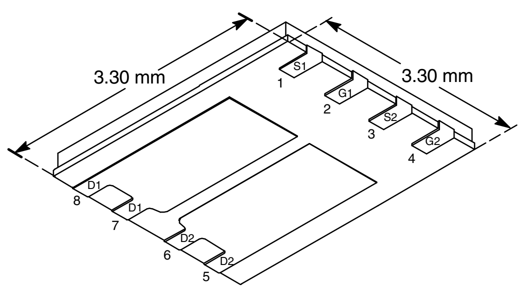
SiS9122DN-VB Datasheet

Dual N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[f]	Q_g (Typ.)
100	0.071 at V_{GS} = 10 V	12.1	3.3 nC
	0.076 at V_{GS} = 7.5 V	11.8	
	0.086 at V_{GS} = 6 V	10.9	

DFN 3x3 EP



Bottom View

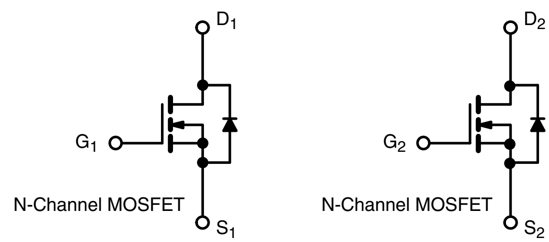
FEATURES

- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- DC/DC Conversion
- Primary side switch
- Synchronous Rectification
- Industrial
- 48 V Battery Monitoring
- LED Driver



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	12.1	A
	T_C = 70 °C		9.7	
	T_A = 25 °C		4.1[a, b]	
	T_A = 70 °C		3.2[a, b]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	20	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	20	
	T_A = 25 °C		2.3[a, b]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	7	
Single Pulse Avalanche Energy		E_{AS}	2.5	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	25	W
	T_C = 70 °C		16	
	T_A = 25 °C		2.8[a, b]	
	T_A = 70 °C		1.8[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[c, d]			260	

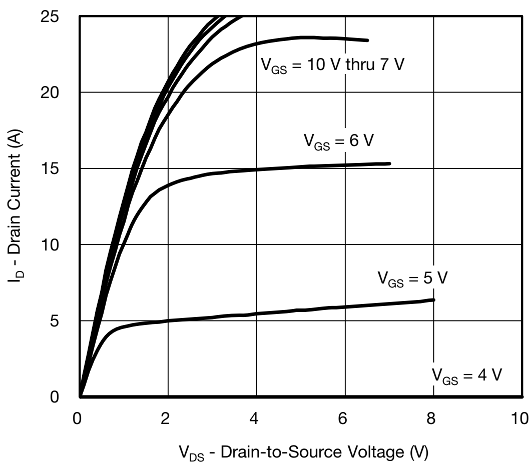
THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, e]	t ≤ 10 s	R_{thJA}	35	44	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4	5	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Maximum under steady state conditions is 94 °C/W.
f. Based on T_C = 25 °C.

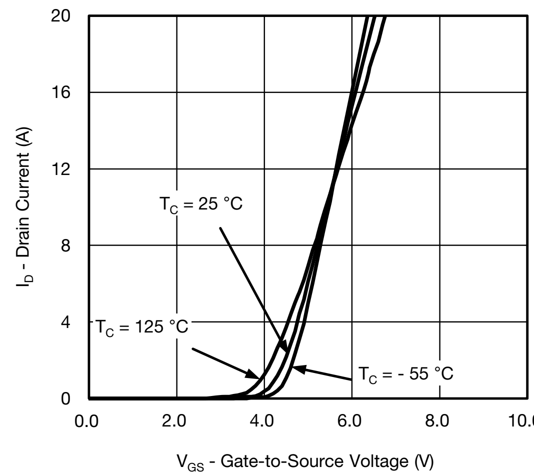
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		61		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.2		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250 µA	2.5		4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	8			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 8 A		0.071		Ω
		V_{GS} = 7.5 V, I_D = 6 A		0.076		
		V_{GS} = 6 V, I_D = 4 A		0.086		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 8 A		11		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		250		pF
Output Capacitance	C_{oss}			73		
Reverse Transfer Capacitance	C_{rss}			7		
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A		5.2	8	nC
		V_{DS} = 50 V, V_{GS} = 7.5 V, I_D = 10 A		4	6	
		V_{DS} = 50 V, V_{GS} = 6 V, I_D = 10 A		3.3	5	
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			1.5		
Output Charge	Q_{oss}	V_{DS} = 50 V, V_{GS} = 0 V		7	11	
Gate Resistance	R_g	f = 1 MHz	1	3.1	5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 5 Ω I_D ≅ 10 A, V_{GEN} = 7.5 V, R_g = 1 Ω		8	16	ns
Rise Time	t_r			8	16	
Turn-Off Delay Time	$t_{d(off)}$			8	16	
Fall Time	t_f			6	12	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 5 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		7	14	
Rise Time	t_r			7	14	
Turn-Off Delay Time	$t_{d(off)}$			8	16	
Fall Time	t_f			5	10	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			20	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	I_S = 4 A, V_{GS} = 0 V		0.87	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 5 A, dI/dt = 100 A/µs, T_J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			27	54	nC
Reverse Recovery Fall Time	t_a			16		ns
Reverse Recovery Rise Time	t_b			14		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

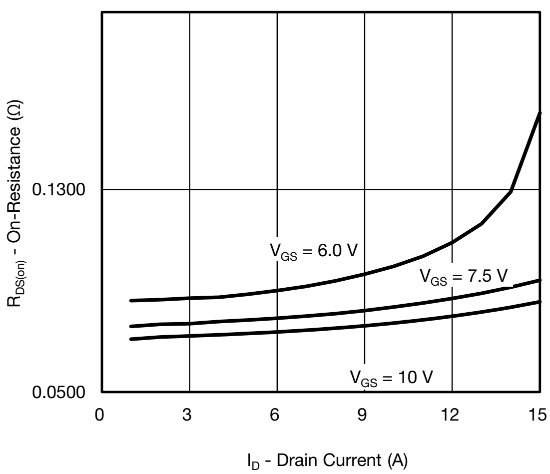
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



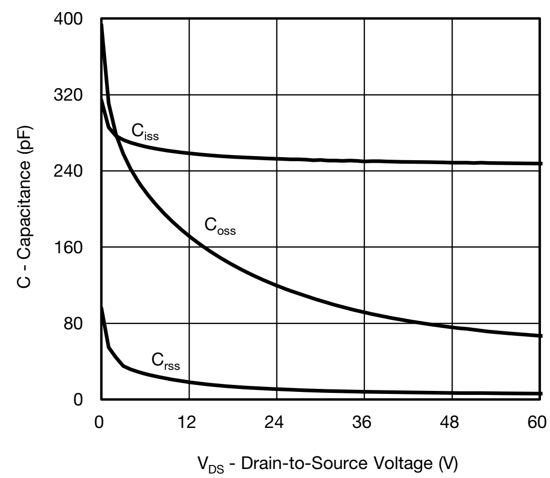
Output Characteristics



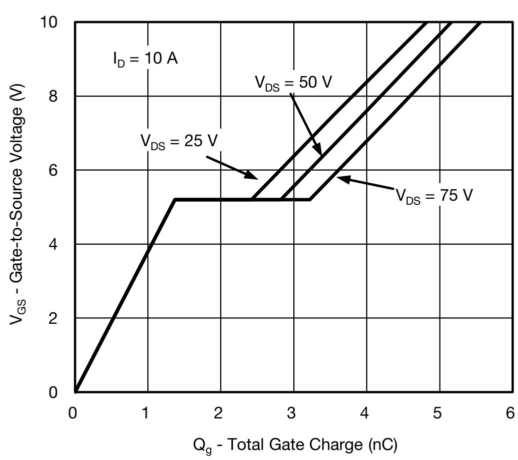
Transfer Characteristics



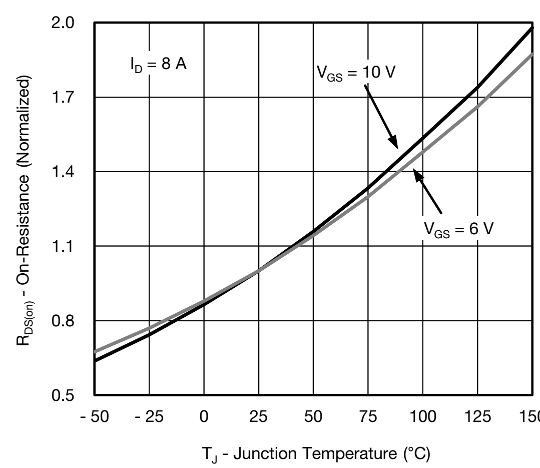
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

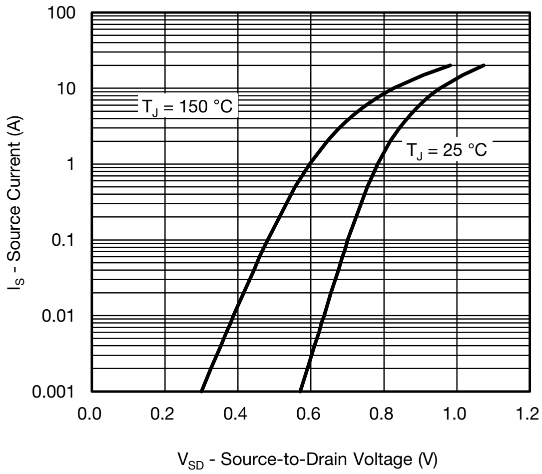


Gate Charge

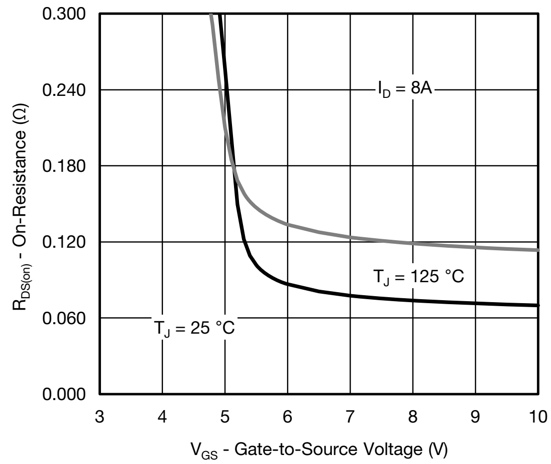


On-Resistance vs. Junction Temperature

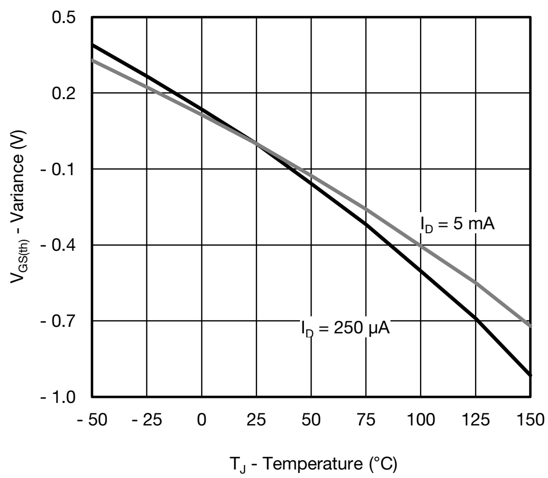
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



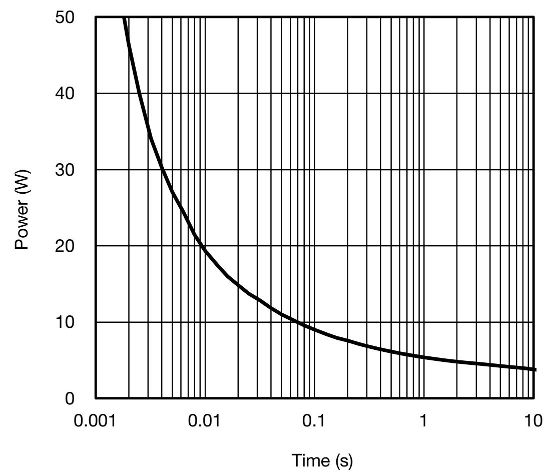
Source-Drain Diode Forward Voltage



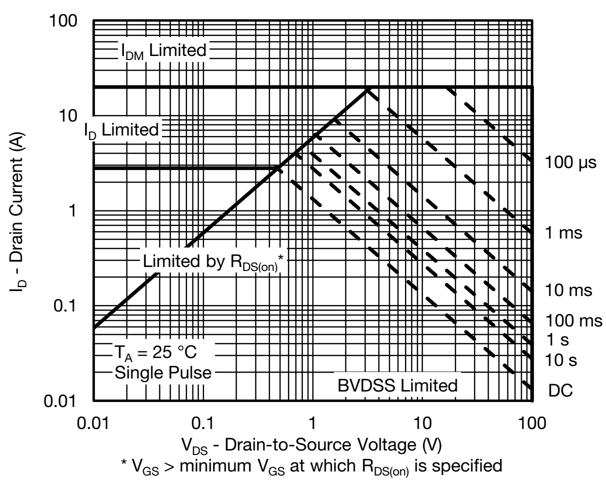
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

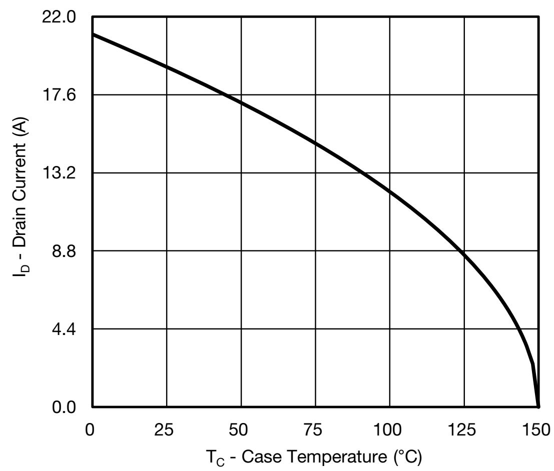


Single Pulse Power, Junction-to-Ambient

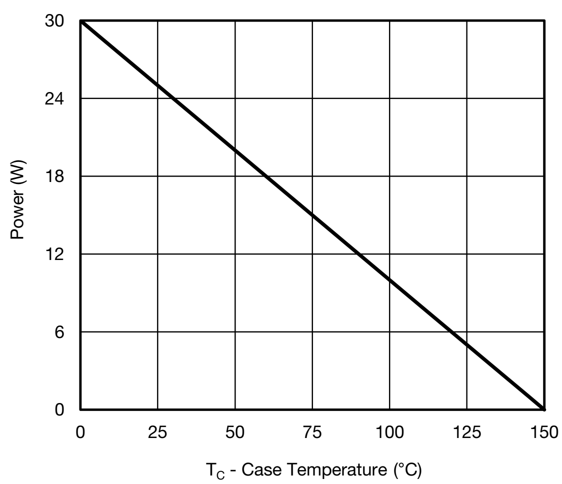


Safe Operating Area, Junction-to-Ambient

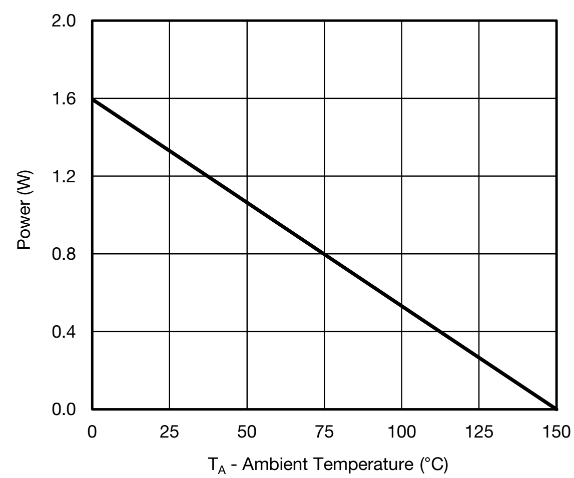
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



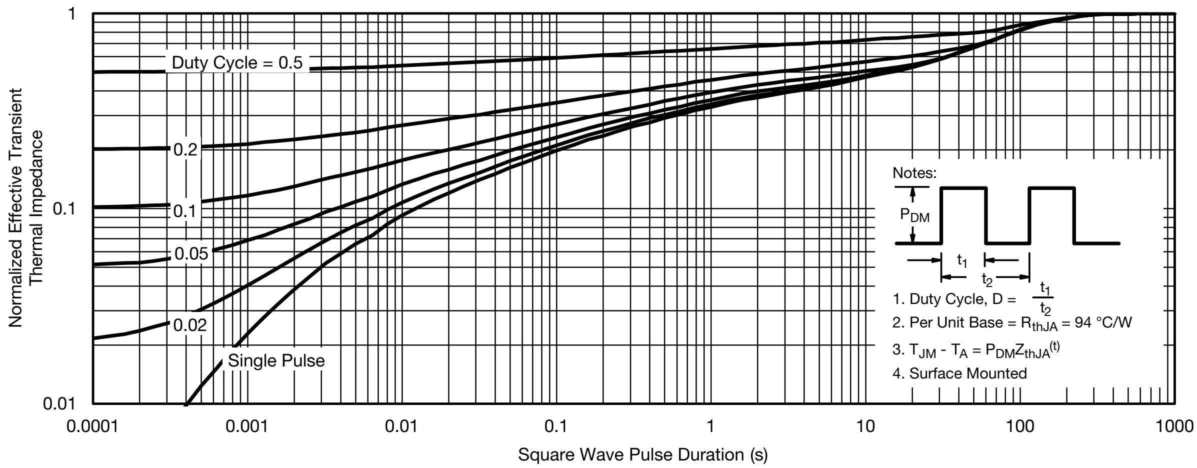
Power, Junction-to-Case



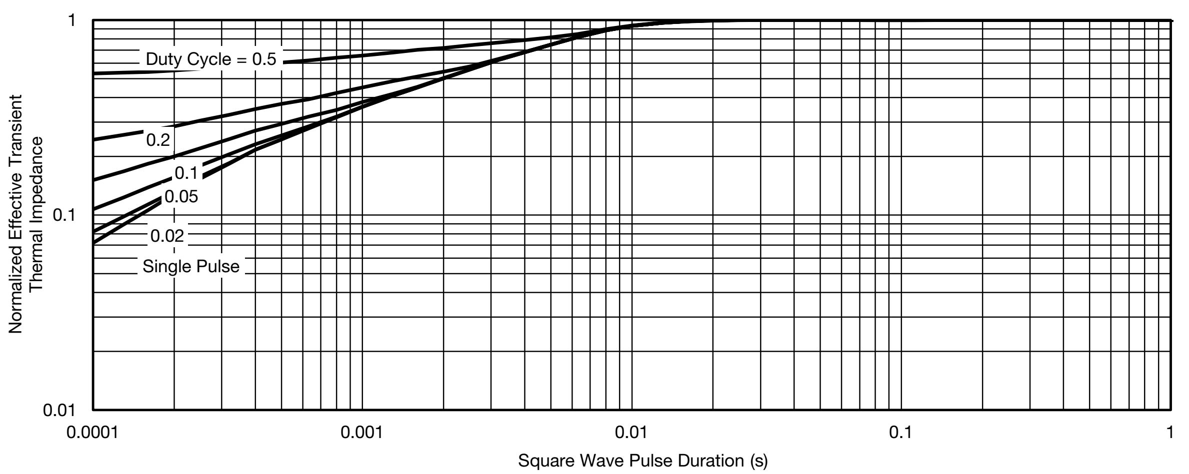
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

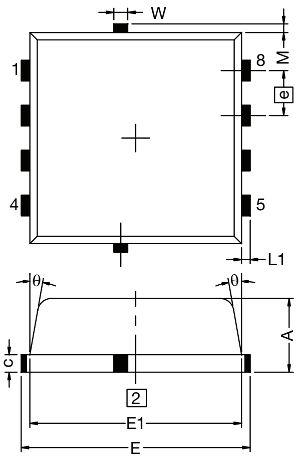


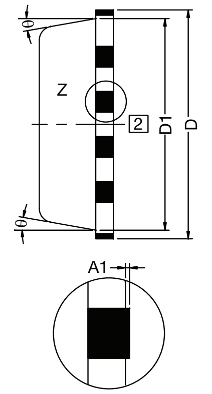
Normalized Thermal Transient Impedance, Junction-to-Ambient



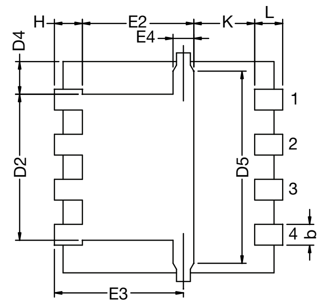
Normalized Thermal Transient Impedance, Junction-to-Case

DFN3x3, (Single / Dual)

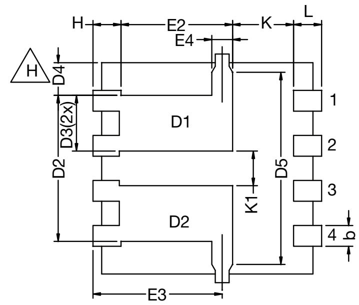




Detail Z



Backside view of single pad



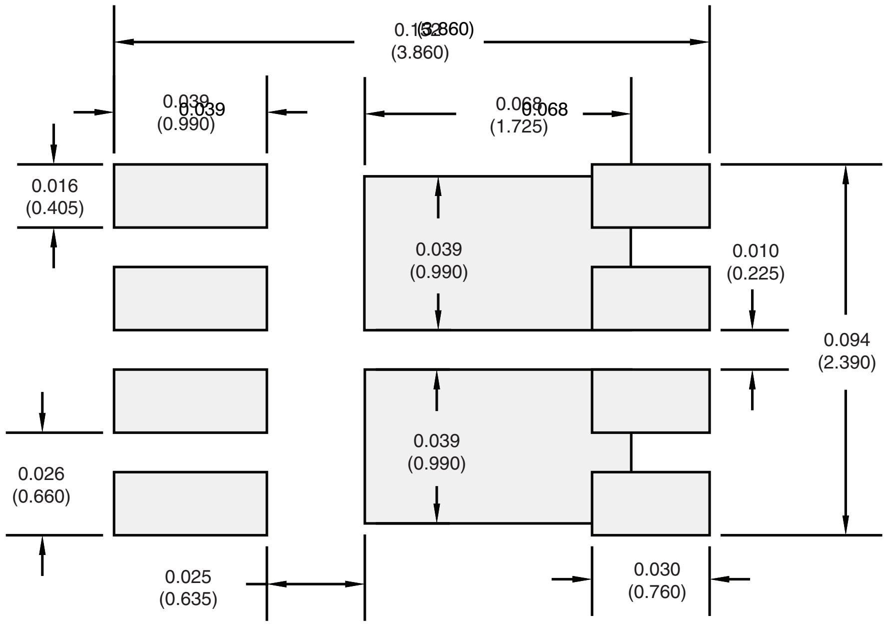
Backside view of dual pad

Notes
1. Inch will govern
2 Dimensions exclusive of mold gate burrs
3. Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 typ.			0.0185 typ		
D5	2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.034 typ.			0.013 typ.		
e	0.65 BSC			0.026 BSC		
K	0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S16-2667-Rev. M, 09-Jan-17
DWG: 5882

RECOMMENDED MINIMUM PADS FOR DFN 3x3 Dual



Recommended Minimum PADs for PowerPAK 1212-8 Dual
Dimensions in Inches/(mm)

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