PESD5V0U1UT-Q

Ultra low capacitance ESD protection diode

16 November 2022 Product data sheet

1. General description

Ultra low capacitance ElectroStatic Discharge (ESD) protection diode in a SOT23 (TO-236AB) small SMD plastic package, designed to protect one high-speed data line from the damage caused by ESD and other transients

2. Features and benefits

- Unidirectional ESD protection of one line
- Ultra low diode capacitance: C_d = 0.6 pF
- Max. peak pulse power: P_{PPM} = 80 W
- Low clamping voltage
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5; (surge)
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Application information

- 10/100/1000 Ethernet
- FireWire
- Communication systems
- Local Area Network (LAN) equipment
- Computers and peripherals
- High-speed data lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	-	0.6	1.5	pF

[1] Measured from pin 1 to 2

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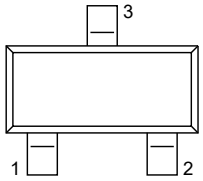
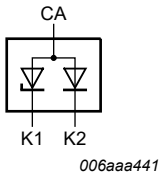
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode ESD protection diode	 SOT23	
2	K2	cathode compensation diode		
3	CA	common anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U1UT-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD5V0U1UT-Q	%AQ

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PPM}	rated peak pulse power	t_p = 8/20 µs	[1]	-	80	W
I_{PPM}	rated peak pulse current		[1]	-	5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	30	kV
		IEC 61000-4-2; air discharge		-	15	kV
		MIL-STD-883; human body model (HBM)		-	10	kV

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.
[3] Measured from pin 1 to 2.

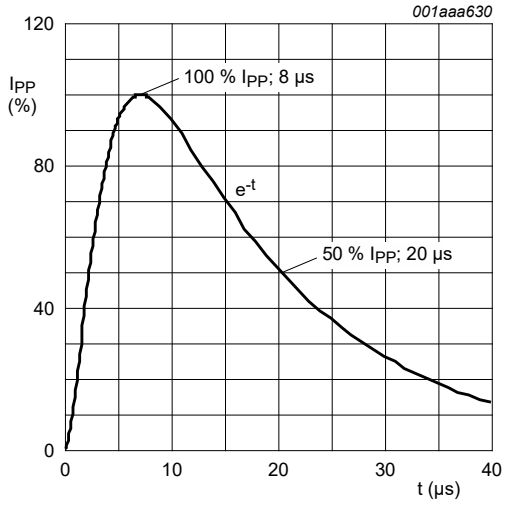


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

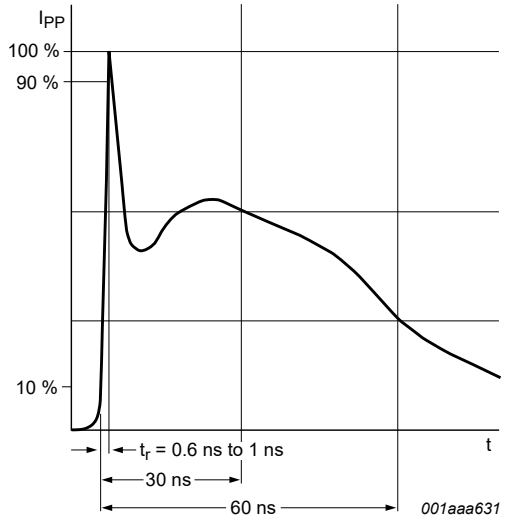


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
V_{BR}	breakdown voltage	I_R = 5 mA; T_{amb} = 25 °C	[1]	7	7.6	8.2	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V; T_{amb} = 25 °C		-	0.03	1	µA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	-	0.6	1.5	pF
V_{CL}	clamping voltage	I_{PP} = 1 A; T_{amb} = 25 °C	[1] [2]	-	-	12	V
		I_{PPM} = 5 A; T_{amb} = 25 °C	[1] [2]	-	-	21	V
R_{diff}	differential resistance	I_R = 1 mA; T_{amb} = 25 °C		-	-	80	Ω

[1] Measured from pin 1 to 2
[2] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.

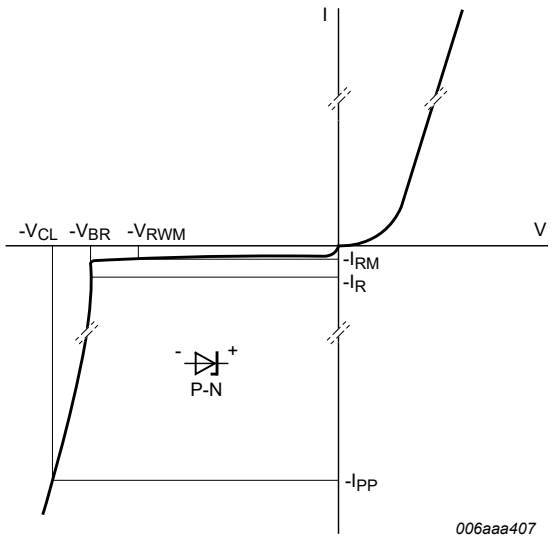


Fig. 3. V-I characteristics for a unidirectional ESD protection diode

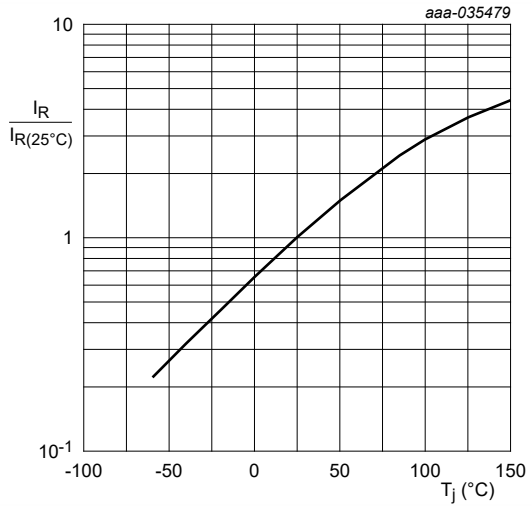


Fig. 4. Relative variation of reverse leakage current as a function of junction temperature; typical values

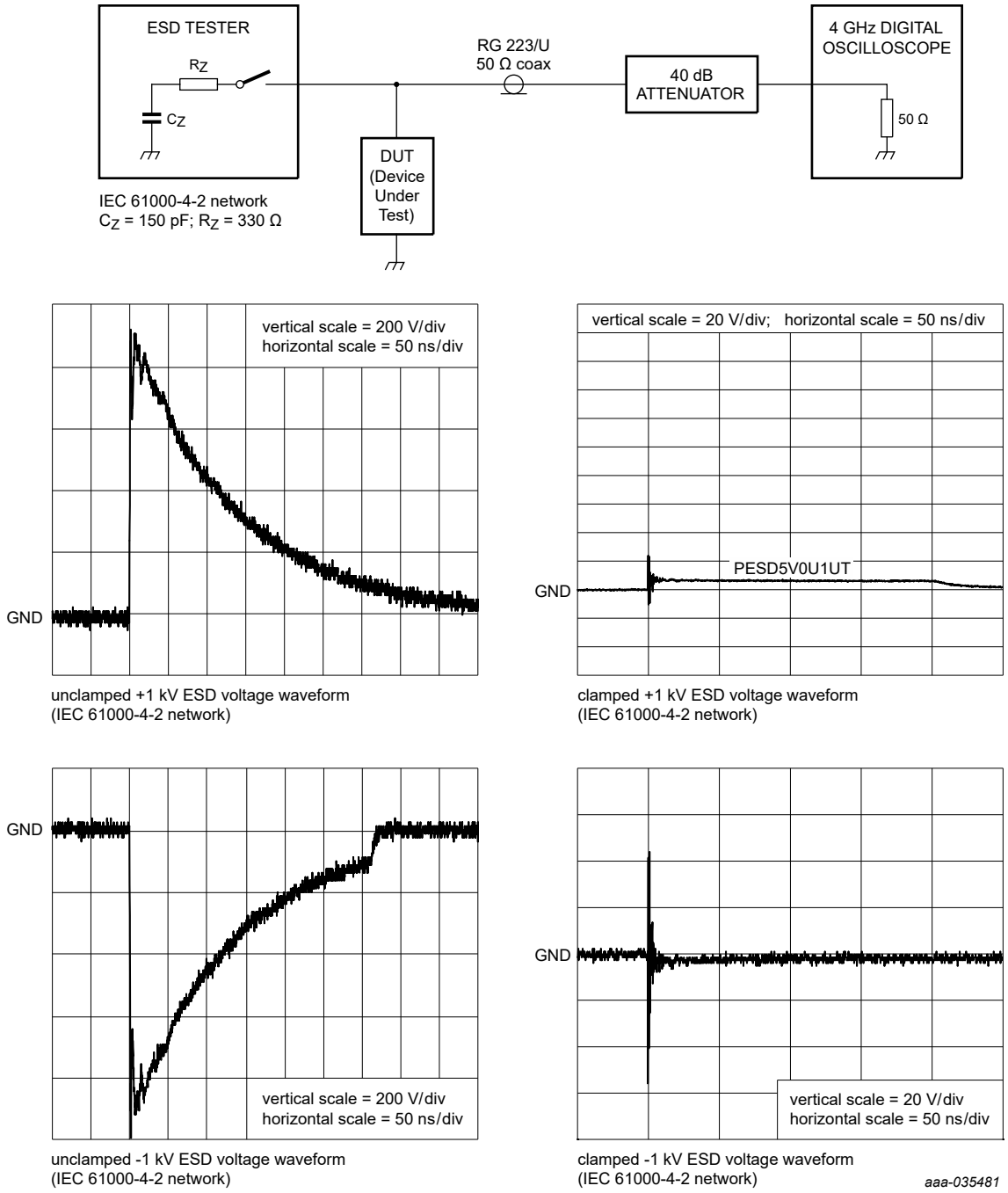
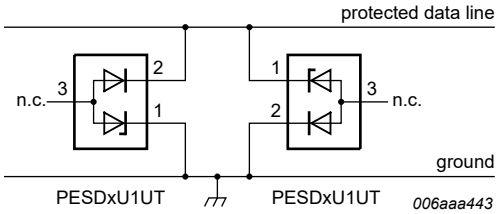


Fig. 5. ESD clamping test setup and waveforms

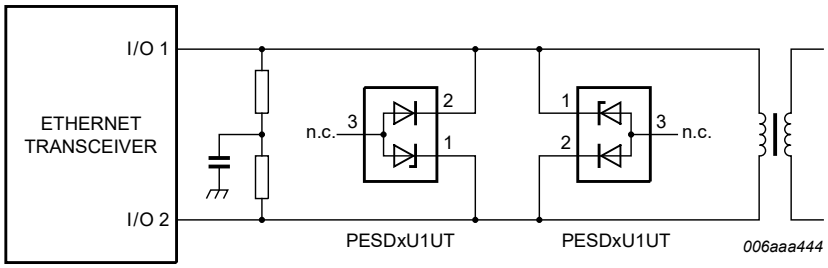
10. Application information

The device is designed for protection of high-speed data lines from damage caused by ESD and surge pulses. The device combines an ESD protection diode and an ultra low capacitance compensation diode to ensure a low device capacitance.



Two PESDxU1UT devices in anti-parallel configuration provide ESD protection in a common-mode application.
The two PESDxU1UT devices should be connected as follows:
protected data line is connected to
device 1 / pin 2
device 2 / pin 1
Ground is connected to
device 1 / pin 1
device 2 / pin 2
pin 3 is not connected for both devices

Fig. 6. Bidirectional ESD protection of one line, common mode



Two PESDxU1UT devices in anti-parallel configuration provide ESD protection in a differential-mode configuration as e.g. for Ethernet applications.
The two PESDxU1UT should be connected as follows:
I/O line 1 is connected to
device 1 / pin 2
device 2 / pin 1
I/O line 2 is connected to
device 1 / pin 1
device 2 / pin 2
pin 3 is not connected for both devices

Fig. 7. Differential mode Ethernet protection

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

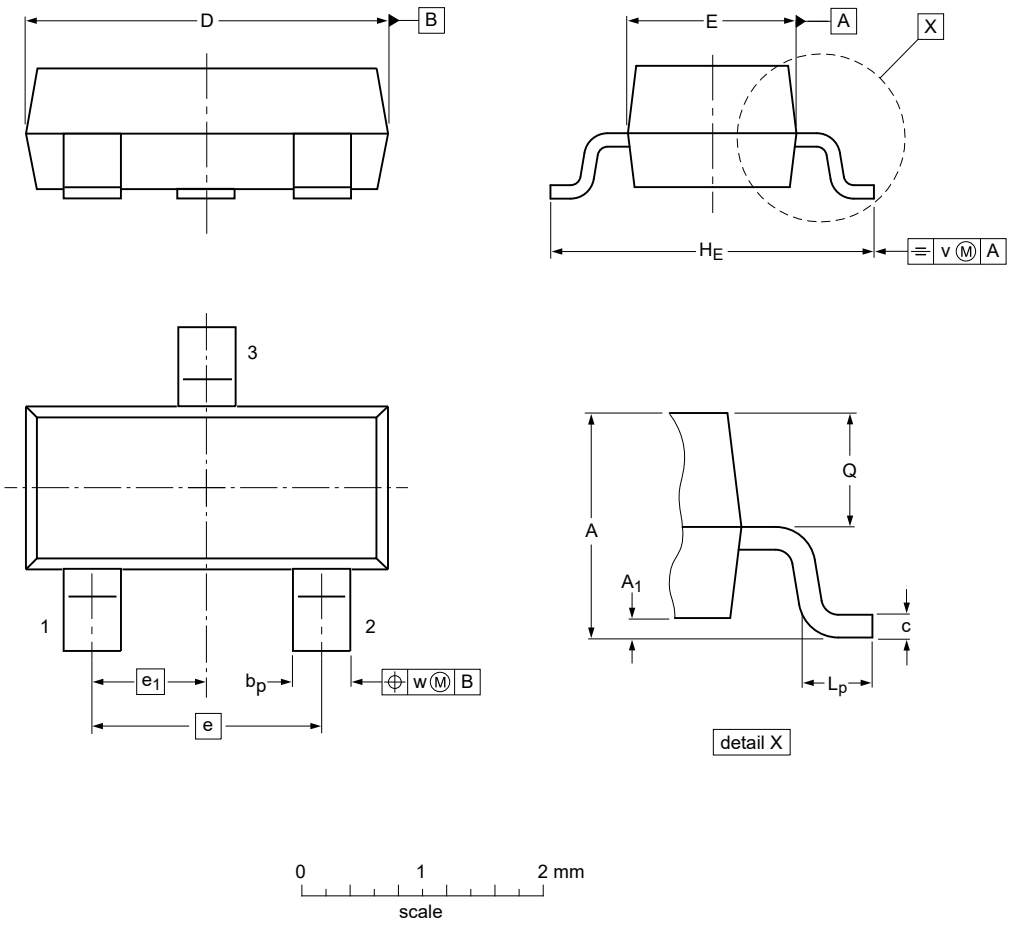
11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	max	1.1	0.1	0.48	0.15	3.0	1.4			2.5	0.45	0.55		
	nom							1.9	0.95				0.2	0.1
	min	0.9		0.38	0.09	2.8	1.2			2.1	0.15	0.45		

sot023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~14-06-19~~ 14-09-22

Fig. 8. Package outline SOT23

13. Soldering

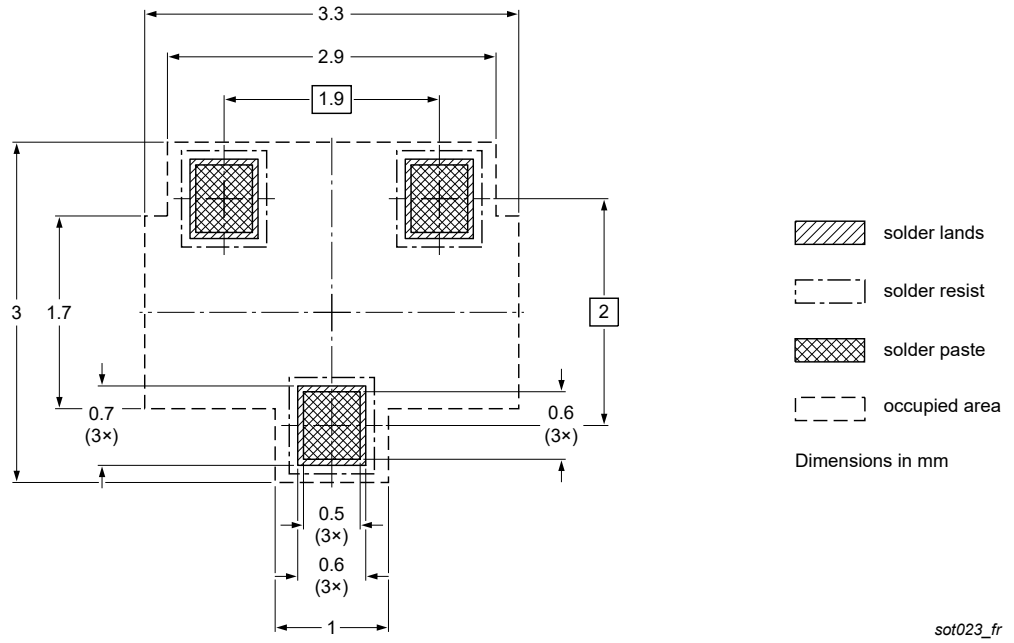


Fig. 9. Reflow soldering footprint for SOT23

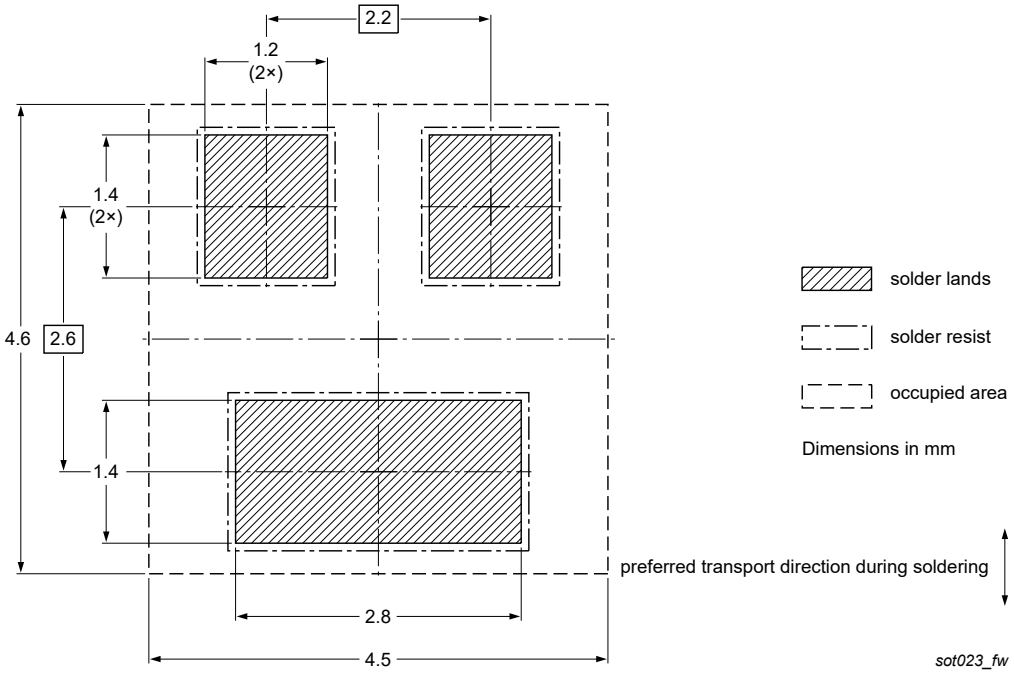


Fig. 10. Wave soldering footprint for SOT23

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U1UT-Q v.1	20221116	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 16 November 2022