

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	EV7N65F-T3
▶ Overseas	Part Number	7N65F
▶ Equivalent	Part Number	7N65F

"T3" means TO-220

EV is the abbreviation of name EVVO

N-Channel Enhancement Mode Power MOSFET

Description

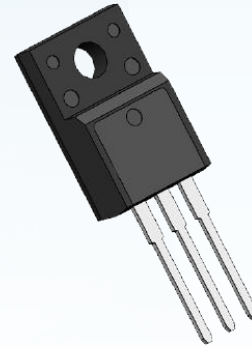
The 7N65F uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate Charge It can be used in a wide variety of applications.

Application

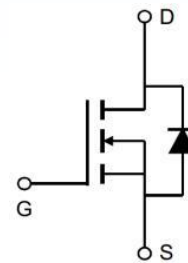
- ☐ Power switching application.
- ☐ Hard switched and high frequency circuits.
- ☐ Uninterruptible power supply.

Features

- ☐ $V_{DS} = 650V$, $I_D = 7A$
- ☐ $R_{DS(ON)} : 1.1\Omega @ V_{GS}=10V$
- ☐ Low gate charge.
- ☐ Green device available.
- ☐ Advanced high cell density trench technology for ultra low on-resistance.
- ☐ Excellent package for good heat dissipation.



Marking and pin assignment



N-Channel MOSFET

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain- Source Voltage	650	V
V_{GS}	Gate Source Voltage	± 30	V
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current ¹	7	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current ¹	4.5	A
I_{DM}	Pulsed Drain Current ³	28	A
E_{AS}, E_{AR}	Avalanche Energy ⁵	49	mJ
I_{AS}, I_{AR}	Avalanche Current ⁵	14	A
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation ⁴	28	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction-to- Case ²	3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ²	62	$^\circ\text{C}/\text{W}$

Electrical Characteristics (TC=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=3.5A$	---	1.1	1.2	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2	3	4	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	μA
		$V_{DS}=520V, V_{GS}=0V, T_J=100^\circ C$	---	---	10	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 30V, V_{DS}=0V$	---	---	± 100	nA
g_{FS}	Forward Transconductance	$V_{DS}=10V, I_D=3.5A$	---	7	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=520V, V_{GS}=10V, I_D=4A$	---	32	48	nC
Q_{gs}	Gate-Source Charge		---	6.4	10	
Q_{gd}	Gate-Drain Charge		---	11.8	18	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=300V, I_{DS}=4A,$ $V_{GEN}=10V, R_G=25\Omega$	---	30	60	nS
T_r	Rise Time		---	34	68	
$T_{d(off)}$	Turn-Off Delay Time		---	72	144	
T_f	Fall Time		---	28	56	
C_{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1MHz$	---	1676	2995	pF
C_{oss}	Output Capacitance		---	135	180	
C_{rss}	Reverse Transfer Capacitance		---	27	50	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$	---	---	7	A
I_{SM}	Pulsed Source Current		---	---	14	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_{SD}=3.5A, T_J=25^\circ C$	---	---	0.8	V
T_{rr}	Reverse Recovery Time	$I_S=3.5A, V_{GS}=10V,$ $di/dt=100A/\mu s, T_J=25^\circ C$	---	210	---	nS
Q_{rr}	Reverse Recovery Charge		---	0.85	---	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.
5. The EAS test condition is $V_{DD}=30V, V_{GS}=10V, L=0.5mH, I_{AS}=14A$

N-Ch 650V Fast Switching MOSFETs

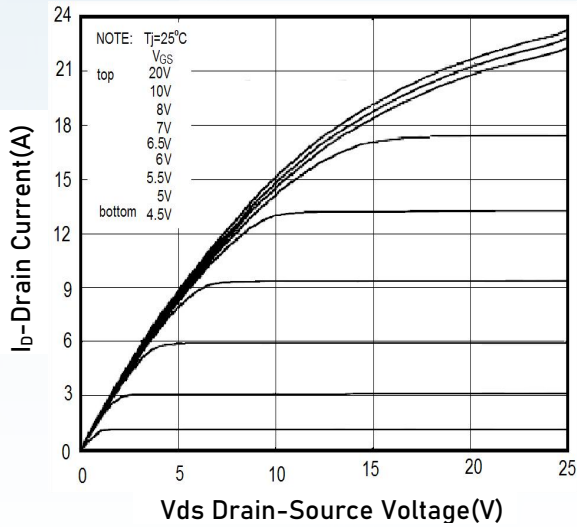


Fig.1 Typical Output Characteristics

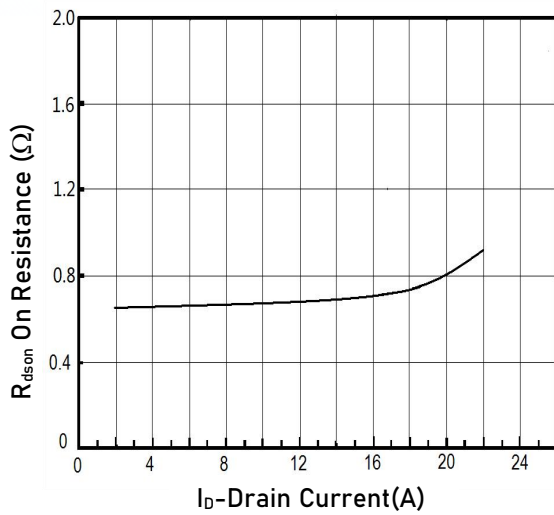


Fig.3 Drain-Source On Resistance

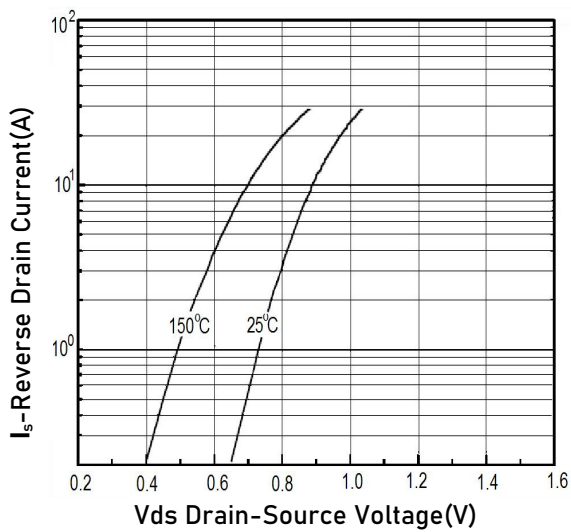


Fig.5 Forward Characteristics Of Reverse

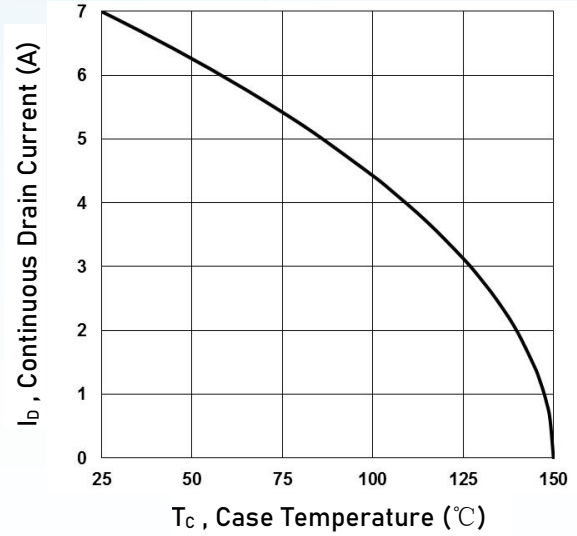


Fig.2 Drain Current

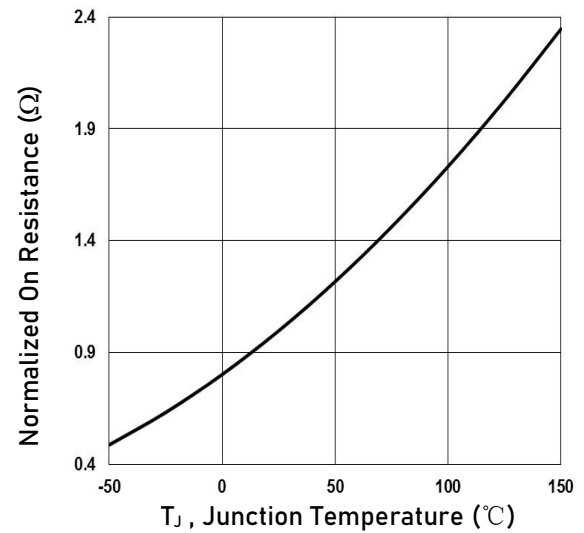


Fig.4 Normalized RDSON vs. T_J

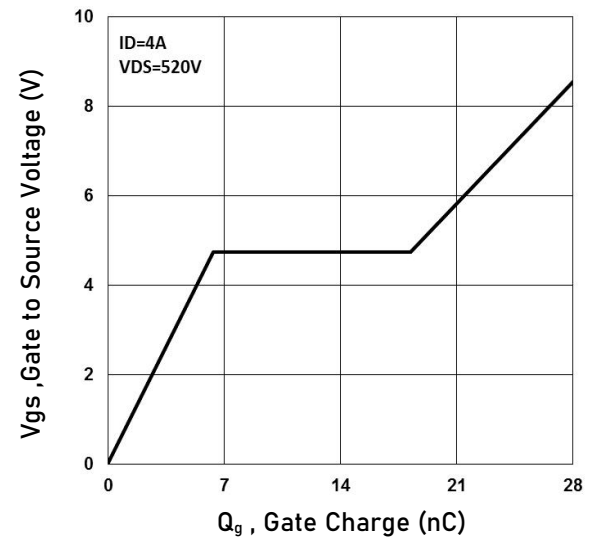


Fig.6 Gate-Charge Characteristics

N-Ch 650V Fast Switching MOSFETs

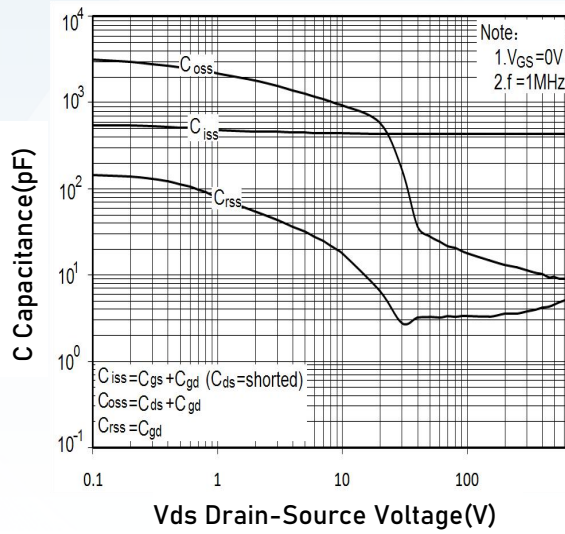


Fig.7 Capacitance

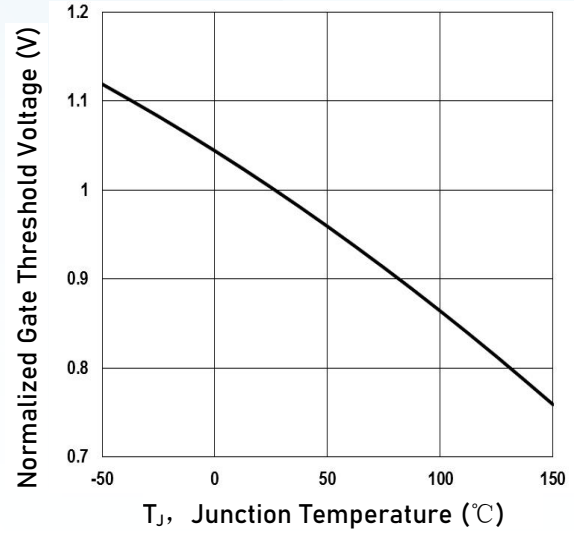


Fig.8 Normalized V_{th} vs. T_J

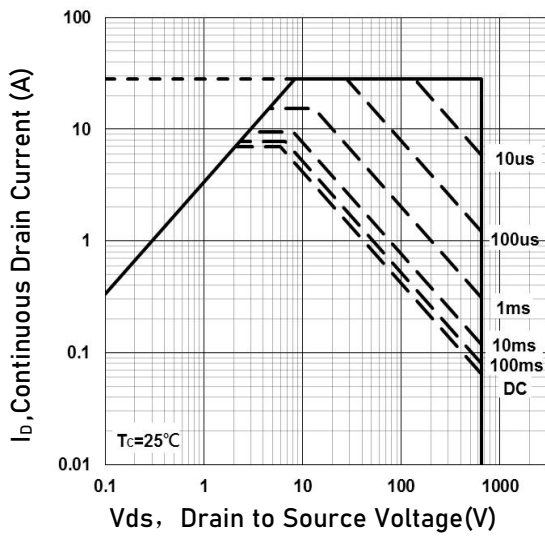


Fig.9 Safe Operating Area

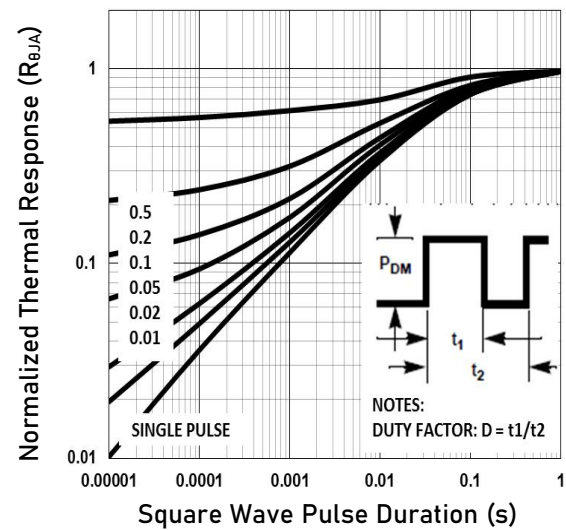
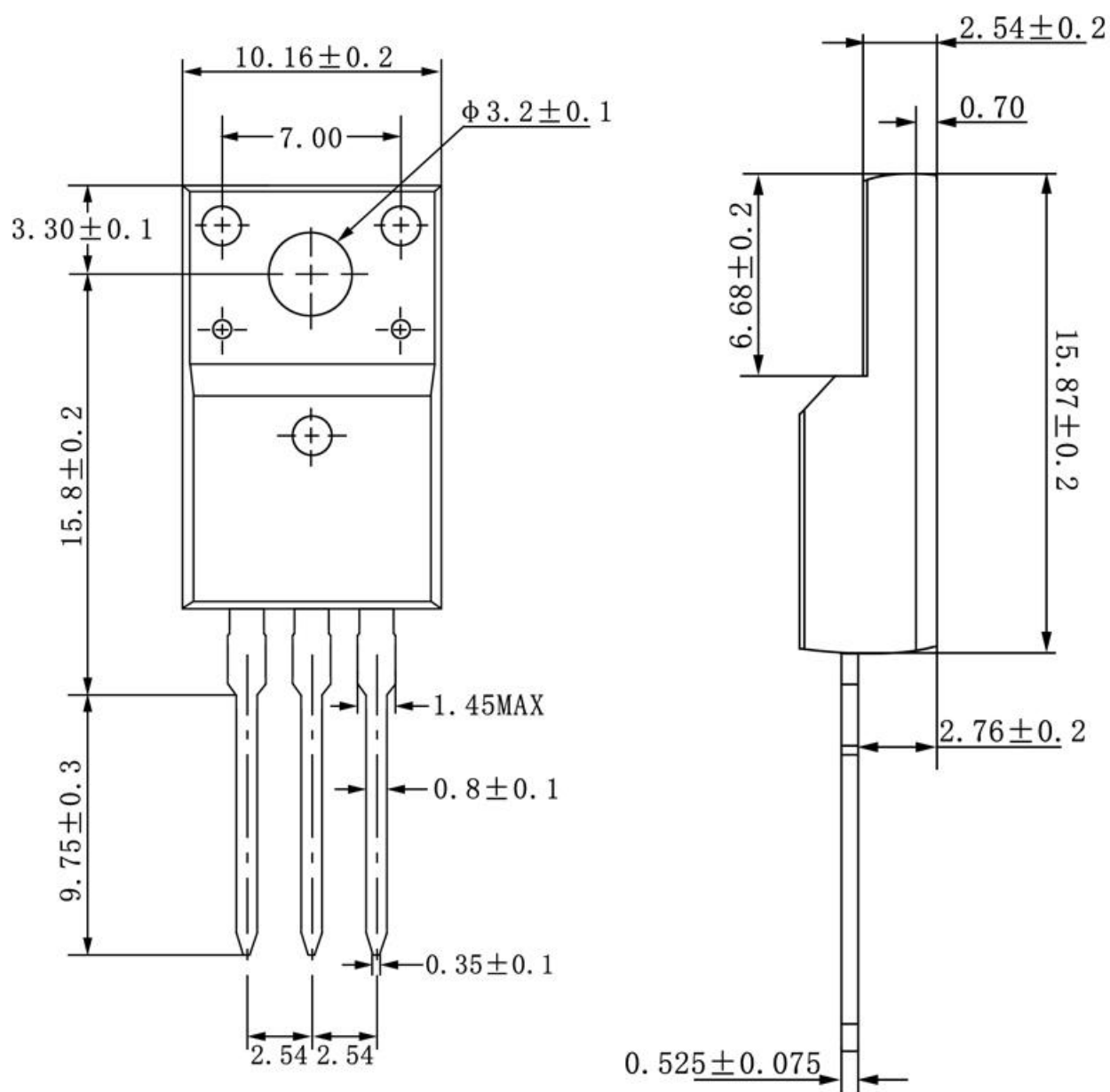


Fig.10 Transient Thermal Impedance

TO-220F Package Information



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