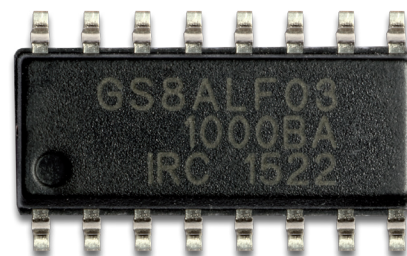


SOIC Thin Film on Ceramic Resistor Networks

SOIC-C Series

Features

- Tested for COTS applications
- Both narrow and wide body versions available
- Standard JEDEC 8, 14, 16, and 20 pin packages
- Ultra-stable TaN resistors on ceramic substrate
- Lower crosstalk than silicon substrate types



 All parts are Pb-free and comply with EU Directive 2011/65/EU amended by (EU) 2015/863 (RoHS3)

SOIC-C resistor networks are high density, low crosstalk networks which combine high precision with the stability and reliability associated with the self-passivating tantalum nitride film system.

Electrical Data

Resistance Range	100R – 200K
Absolute Tolerance	To $\pm 0.1\%$
Ratio Tolerance to R1	To $\pm 0.05\%$
Absolute TCR	To $\pm 25\text{ppm}/^\circ\text{C}$
Tracking TCR	To $\pm 5\text{ppm}/^\circ\text{C}$
Element Power Rating @ 70°C Isolated Schematic Bussed Schematic	100mW 50mW
Power Rating @ 70°C SOIC-N Package	8-Pin 400mW 14-Pin 700mW 16-Pin 800mW
Power Rating @ 70°C SOIC-W Package	16-Pin 1.2W 20-Pin 1.5W
Rated Operating Voltage (not to exceed $\sqrt{\text{Power} \times \text{Resistance}}$)	100 Volts
Operating Temperature	-55°C to $\pm 125^\circ\text{C}$
Noise	<-25dB

Environmental Data

Test Per MIL-PRF-83401	Typical Delta R	Max Delta R
Thermal Shock	$\pm 0.02\%$	$\pm 0.1\%$
Power Conditioning	$\pm 0.03\%$	$\pm 0.1\%$
High Temperature Exposure	$\pm 0.03\%$	$\pm 0.05\%$
Short-time Overload	$\pm 0.02\%$	$\pm 0.05\%$
Low Temperature Storage	$\pm 0.03\%$	$\pm 0.05\%$
Life	$\pm 0.05\%$	$\pm 0.1\%$

General Note

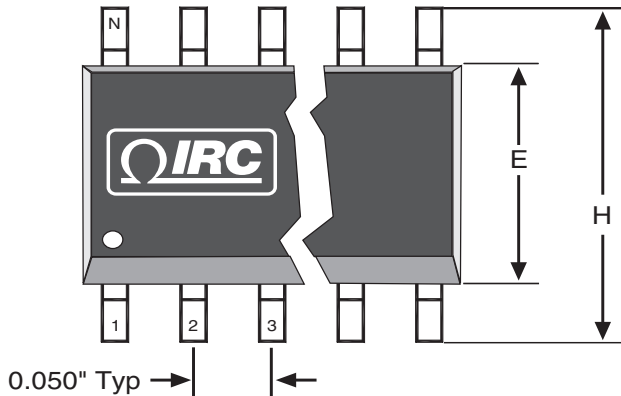
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All information is subject to TT Electronics' own data and is considered accurate at time of going to print.

BI Technologies IRC Welwyn

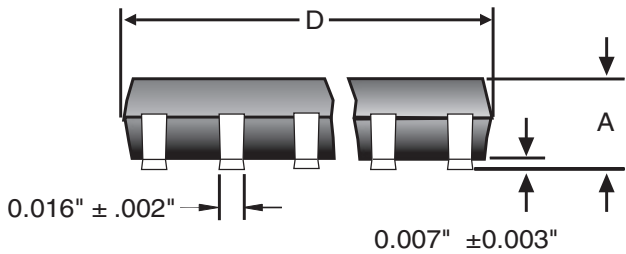
www.ttelectronics.com/resistors

SOIC-C Series

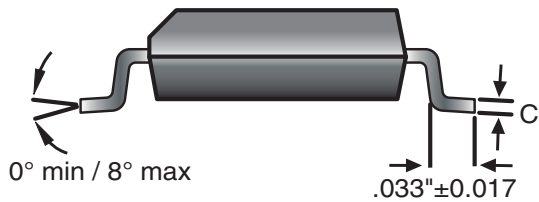
Physical and Schematic Data



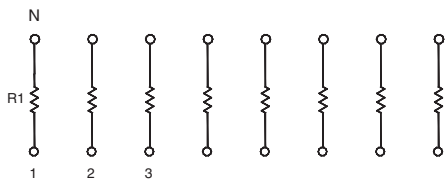
	SOIC-N			SOIC-W	
	8-Pin	14-Pin	16-Pin	16-Pin	20-Pin
D	0.193"±0.004 (4.902 ± 0.102)	0.341"±0.004 (8.661 ± 0.102)	0.390"±0.004 (9.906 ± 0.102)	0.402"±0.004 (10.211 ± 0.102)	0.502"±0.004 (12.751 ± 0.102)
H		0.236"±0.008 (5.994 ± 0.203)		0.406"±0.008 (10.312 ± 0.203)	
E		0.153"±0.004 (3.886 ± 0.102)		0.295"±0.004 (7.493 ± 0.102)	
A		0.064"±0.004 (1.626 ± 0.102)		0.100"±0.004 (2.540 ± 0.102)	
C		0.0075" - 0.010" (0.191 ± 0.254)		0.011"±0.002 (0.279 ± 0.051)	



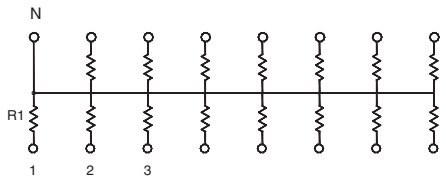
Note: All dimesions exclude mold flash and end flash which shall not exceed 0.006" per side.



Note: Lead Coplanarity 0.004" Max.

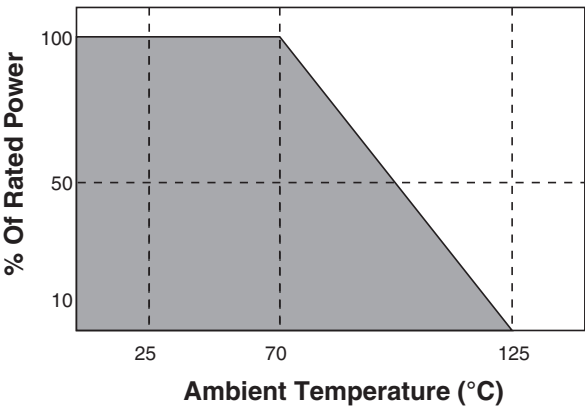


Schematic A
Isolated



Schematic B
Bussed

Power Derating Curve



For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.

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SOIC-C Series

Ordering Procedure

Example: **GS4ALF021002BATHR** (8 pin narrow SOIC, isolated elements, 50ppm/°C, 10 kilohms, absolute tolerance ±0.1%, ratio tolerance ±0.05%, tube packed, variant HR, Pb-free)

G	S	4	A	L	F	0	2	1	0	0	2	B	A	T	H	R	
1	2	3	4	5	6	7	8	9	10								

1	2	3	4	5	6	7	8	9	10
Type	Size	Schematic	Termination	TCR	Value	Absolute Tolerance	Ratio Tolerance	Packing	Variant
GS = Narrow SOIC	4=8 pin	A=Isolated	LF=Pb-free	01=±100ppm/°C	3 digits + multiplier R = ohms for values < 100 ohms	B=±0.1%	A=±0.05%	T=Tube	Optional code - see below
	7=14 pin	B=Bussed		02=±50ppm/°C		C=±0.25	B=±0.1%	R=Reel	
	8=16 pin			03=±25ppm/°C		D=±0.5%	C=±0.25%		
GL = Wide SOIC	0=20 pin					F=±1%	D=±0.5%		
						G=±2%	F=±1%		
						J=±5%	G=±2%		

Variant codes	
Blank	Standard
HR	High reliability screened (50 cycles, thermal shock)

Note: The Variant code may be placed between Schematic and Termination.
Type may be preceded by the optional prefix **GUL-**, e.g. **GUL-GS4ALF021002BATHR**