# DSC1001/3/4

## 1.8V-3.3V Low-Power Precision CMOS Oscillators

### Features

- Frequency Range: 1 MHz to 150 MHz
- Exceptional Stability over Temperature
  - ±10 ppm, ±20 ppm, ±25 ppm, ±50 ppm
- Operating Voltage
  - 1.7 to 3.6V
- Operating Temperature Range
  - Ext. Industrial –40°C to 105°C
  - Industrial –40°C to 85°C
  - Commercial –20°C to 70°C
- Low Operating and Standby Current
  - 6 mA Operating (1 MHz)
  - 15 µA Standby (Max.)
- Ultra Miniature Footprint
  - 2.5 mm x 2.0 mm x 0.85 mm
  - 3.2 mm x 2.5 mm x 0.85 mm
  - 5.0 mm x 3.2 mm x 0.85 mm
  - 7.0 mm x 5.0 mm x 0.85 mm
- MIL-STD 883 Shock and Vibration Resistant
- Pb Free, RoHS, Reach SVHC Compliant
- AEC-Q100 Reliability Qualified

### Applications

- Mobile Applications
- Consumer Electronics
- Portable Electronics
- DVR, CCTV, Surveillance Cameras
- Low Profile Applications
- Industrial Applications

### Benefits

- Pin for Pin “Drop-In” Replacement for Industry Standard Oscillators
- Semiconductor Level Reliability, Significantly Higher than Quartz
- Short Mass Production Lead Times
- Longer Battery Life/Reduced Power Consumption
- Compact Plastic Package
- Cost Effective

### General Description

The DSC1001/3/4 is a silicon MEMS based CMOS family of oscillators that offers excellent jitter and stability performance over a wide range of supply voltages and temperatures. The device operates from 1 MHz to 150 MHz with supply voltages between 1.8 to 3.3 volts and temperature ranges up to –40°C to 105°C.

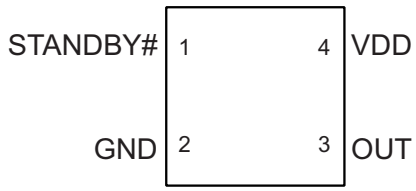
The DSC1001/3/4 incorporate an all silicon resonator that is extremely robust and nearly immune to stress related fractures, common to crystal based oscillators. Without sacrificing the performance and stability required of today’s systems, a crystal-less design allows for a higher level of reliability, making the DSC1001/3/4 ideal for rugged, industrial, and portable applications where stress, shock, and vibration can damage quartz crystal based systems.

Available in industry standard packages, the DSC1001/3/4 can be “dropped-in” to the same PCB footprint as standard crystal oscillators.

The DSC1003 and DSC1004 have the same functionality and performance as the DSC1001, but feature higher output drives of 25 pF and 40 pF, respectively.

### Package Types

**DSC1001/3/4**
CDFN/DFN
(Top View)

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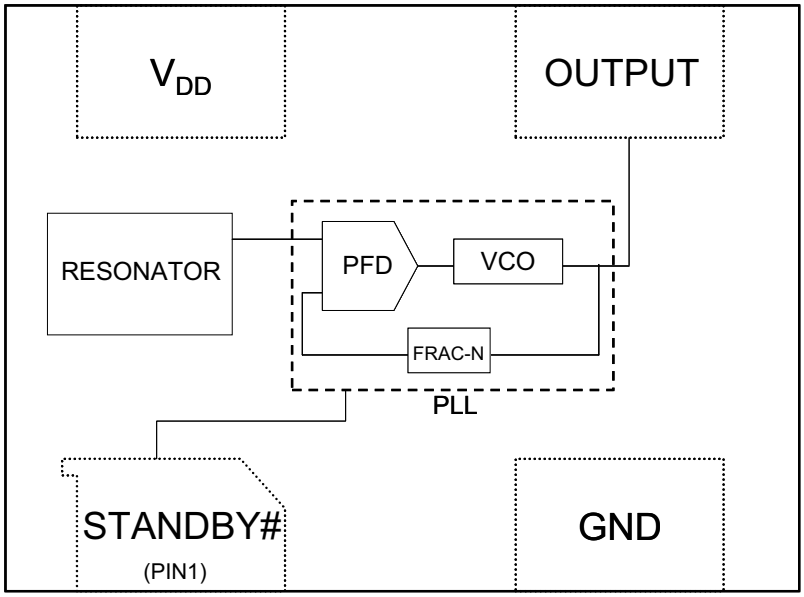
## Block Diagram





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## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Input Voltage ($V_{IN}$) .....–0.3V to $V_{DD}$ + 0.3V
ESD Protection ..... 4 kV HBM, ±200V MM, 1.5 kV CDM

### Recommended Operating Conditions

Supply Voltage ($V_{DD}$) ..... +1.7V to +3.6V
Output Load ($Z_L$) ..... R > 10 kΩ, C ≤ 15 pF

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

**Electrical Characteristics:** $V_{DD}$ = 1.8 to 3.3V; $T_A$ = +85°C unless otherwise specified.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| Frequency | $F_0$ | 1 | — | 150 | MHz | Single Frequency | |
| Frequency Tolerance | Δf | — | — | ±10 | ppm | Includes frequency variations due to initial tolerance, temperature and power supply voltage | |
| | | — | — | ±20 | | | |
| | | — | — | ±25 | | | |
| | | — | — | ±50 | | | |
| Aging | Δf | — | — | ±5 | ppm | 1 year @ +25°C | |
| Supply Current, Standby | $I_{DD}$ | — | — | 15 | µA | T = +25°C | |
| Output Startup Time (Note 1) | $t_{SU}$ | — | 1.0 | 1.3 | ms | T = +25°C | |
| Output Disable Time | $t_{DA}$ | — | 20 | 100 | ns | — | |
| Output Duty Cycle | SYM | 45 | — | 55 | % | — | |
| Input Logic Level High | $V_{IH}$ | 0.75 x $V_{DD}$ | — | — | V | — | |
| Input Logic Level Low | $V_{IL}$ | — | — | 0.25 x $V_{DD}$ | V | — | |
| **$V_{DD}$ = 1.8V** | | | | | | | |
| Supply Current, No Load | $I_{DD}$ | — | 6.0 | 6.3 | mA | 1 MHz | $C_L$ = 0 pF, $R_L$ = ∞, T = +25°C |
| | | — | 6.5 | 7.1 | | 27 MHz | |
| | | — | 7.2 | 8.5 | | 70 MHz | |
| | | — | 8.3 | 11.9 | | 150 MHz | |
| Output Logic Level High | $V_{OH}$ | 0.8 x $V_{DD}$ | — | — | V | –6 mA, DSC1004, $C_L$ = 40 pF | |
| | | 0.8 x $V_{DD}$ | — | — | | –6 mA, DSC1003, $C_L$ = 25 pF | |
| | | 0.8 x $V_{DD}$ | — | — | | –4 mA, DSC1001, $C_L$ = 15 pF | |
| Output Logic Level Low | $V_{OL}$ | — | — | 0.2 x $V_{DD}$ | V | 6 mA, DSC1004, $C_L$ = 40 pF | |
| | | — | — | 0.2 x $V_{DD}$ | | 6 mA, DSC1003, $C_L$ = 25 pF | |
| | | — | — | 0.2 x $V_{DD}$ | | 4 mA, DSC1001, $C_L$ = 15 pF | |

**Note 1:** $t_{SU}$ is time to stable output frequency after $V_{DD}$ is applied. $t_{SU}$ and $t_{EN}$ (after EN is asserted) are identical values.

**2:** Measured over 50k clock cycles.

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**TABLE 1-1: DC CHARACTERISTICS (CONTINUED)**

**Electrical Characteristics:** $V_{DD}$ = 1.8 to 3.3V; $T_A$ = +85°C unless otherwise specified.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| Output Transition Rise Time | $t_R$ | — | 1.4 | 3.0 | ns | DSC1001, $C_L$ = 15 pF | T = +25°C, 20% to 80% |
| | | — | 1.5 | 3.0 | | DSC1003, $C_L$ = 25 pF | |
| | | — | 1.8 | 3.0 | | DSC1004, $C_2$ = 40 pF | |
| Output Transition Fall Time | $t_F$ | — | 1.0 | 3.0 | ns | DSC1001, $C_L$ = 15 pF | T = +25°C, 20% to 80% |
| | | — | 1.1 | 3.0 | | DSC1003, $C_L$ = 25 pF | |
| | | — | 1.2 | 3.0 | | DSC1004, $C_2$ = 40 pF | |
| Jitter, Max. Cycle-to-Cycle | $J_{CC}$ | — | 60 | — | ps | f = 100 MHz (Note 2) | |
| Period Jitter | $J_P$ | — | 10 | 15 | $ps_{RMS}$ | f = 100 MHz (Note 2) | |
| **$V_{DD}$ = 2.5V** | | | | | | | |
| Supply Current, No Load | $I_{DD}$ | — | 6.0 | 6.4 | mA | 1 MHz | $C_L$ = 0 pF, $R_L$ = ∞, T = +25°C |
| | | — | 6.7 | 7.5 | | 27 MHz | |
| | | — | 7.7 | 9.4 | | 70 MHz | |
| | | — | 9.6 | 13.9 | | 150 MHz | |
| Output Logic Level High | $V_{OH}$ | 0.9 x $V_{DD}$ | — | — | V | –6 mA, DSC1004, $C_L$ = 40 pF | |
| | | 0.8 x $V_{DD}$ | — | — | | –6 mA, DSC1003, $C_L$ = 25 pF | |
| | | 0.8 x $V_{DD}$ | — | — | | –4 mA, DSC1001, $C_L$ = 15 pF | |
| Output Logic Level Low | $V_{OL}$ | — | — | 0.1 x $V_{DD}$ | V | 6 mA, DSC1004, $C_L$ = 40 pF | |
| | | — | — | 0.2 x $V_{DD}$ | | 6 mA, DSC1003, $C_L$ = 25 pF | |
| | | — | — | 0.2 x $V_{DD}$ | | 4 mA, DSC1001, $C_L$ = 15 pF | |
| Output Transition Rise Time | $t_R$ | — | 1.0 | 2.0 | ns | DSC1001, $C_L$ = 15 pF | T = +25°C, 20% to 80% |
| | | — | 1.1 | 2.0 | | DSC1003, $C_L$ = 25 pF | |
| | | — | 1.2 | 2.0 | | DSC1004, $C_2$ = 40 pF | |
| Output Transition Fall Time | $t_F$ | — | 0.9 | 2.0 | ns | DSC1001, $C_L$ = 15 pF | T = +25°C, 20% to 80% |
| | | — | 1.0 | 2.0 | | DSC1003, $C_L$ = 25 pF | |
| | | — | 1.1 | 2.0 | | DSC1004, $C_2$ = 40 pF | |

**Note 1:** $t_{SU}$ is time to stable output frequency after $V_{DD}$ is applied. $t_{SU}$ and $t_{EN}$ (after EN is asserted) are identical values.

**2:** Measured over 50k clock cycles.


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**TABLE 1-1: DC CHARACTERISTICS (CONTINUED)**

**Electrical Characteristics:** $V_{DD}$ = 1.8 to 3.3V; $T_A$ = +85°C unless otherwise specified.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---|---|---|---|---|---|---|
| Jitter, Max. Cycle-to-Cycle | $J_{CC}$ | — | 50 | — | ps | f = 100 MHz (Note 2) | |
| Period Jitter | $J_P$ | — | 5 | 10 | $ps_{RMS}$ | f = 100 MHz (Note 2) | |
| **$V_{DD}$ = 3.3V** | | | | | | | |
| Supply Current, No Load | $I_{DD}$ | — | 6.0 | 6.5 | mA | 1 MHz | $C_L$ = 0 pF, $R_L$ = ∞, T = +25°C |
| | | — | 6.8 | 8.0 | | 27 MHz | |
| | | — | 8.2 | 10.5 | | 70 MHz | |
| | | — | 10.8 | 16.6 | | 150 MHz | |
| Output Logic Level High | $V_{OH}$ | 0.9 x $V_{DD}$ | — | — | V | –8 mA, DSC1004, $C_L$ = 40 pF | |
| | | 0.9 x $V_{DD}$ | — | — | | –6 mA, DSC1003, $C_L$ = 25 pF | |
| | | 0.8 x $V_{DD}$ | — | — | | –4 mA, DSC1001, $C_L$ = 15 pF | |
| Output Logic Level Low | $V_{OL}$ | — | — | 0.1 x $V_{DD}$ | V | 8 mA, DSC1004, $C_L$ = 40 pF | |
| | | — | — | 0.1 x $V_{DD}$ | | 6 mA, DSC1003, $C_L$ = 25 pF | |
| | | — | — | 0.2 x $V_{DD}$ | | 4 mA, DSC1001, $C_L$ = 15 pF | |
| Output Transition Rise Time | $t_R$ | — | 1.0 | 2.0 | ns | DSC1001, $C_L$ = 15 pF | T = +25°C, 20% to 80% |
| | | — | 1.1 | 2.0 | | DSC1003, $C_L$ = 25 pF | |
| | | — | 1.2 | 2.0 | | DSC1004, $C_2$ = 40 pF | |
| Output Transition Fall Time | $t_F$ | — | 0.9 | 2.0 | ns | DSC1001, $C_L$ = 15 pF | T = +25°C, 20% to 80% |
| | | — | 1.0 | 2.0 | | DSC1003, $C_L$ = 25 pF | |
| | | — | 1.1 | 2.0 | | DSC1004, $C_2$ = 40 pF | |
| Jitter, Max. Cycle-to-Cycle | $J_{CC}$ | — | 50 | — | ps | f = 100 MHz (Note 2) | |
| Period Jitter | $J_P$ | — | 5 | 10 | $ps_{RMS}$ | f = 100 MHz (Note 2) | |

**Note 1:** $t_{SU}$ is time to stable output frequency after $V_{DD}$ is applied. $t_{SU}$ and $t_{EN}$ (after EN is asserted) are identical values.

**2:** Measured over 50k clock cycles.

## TEMPERATURE SPECIFICATIONS (Note 1)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Operating Temperature Range (T) | $T_A$ | –40 | — | +105 | °C | Ordering Option L |
| | | –40 | — | +85 | °C | Ordering Option I |
| | | –20 | — | +70 | °C | Ordering Option E |
| Junction Operating Temperature | $T_J$ | — | — | +150 | °C | — |
| Storage Temperature Range | $T_A$ | –55 | — | +150 | °C | — |
| Soldering Temperature Range | $T_S$ | — | — | +260 | °C | 40 sec. max |

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.


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## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and Table 2-2.

**TABLE 2-1: CDFN PACKAGE PIN FUNCTION TABLE**

| Pin Number | Symbol | Description |
|---|---|---|
| 1 | STANDBY# | Standby input (**Section 4.1 “Standby Function”**) |
| 2 | GND | Power supply ground |
| 3 | OUT | Oscillator output |
| 4 | VDD | Positive power supply |

**TABLE 2-2: DFN PACKAGE PIN FUNCTION TABLE**

| Pin Number | Symbol | Description |
|---|---|---|
| 1 | STANDBY# | Standby input (**Section 4.1 “Standby Function”**) |
| 2 | GND | Power supply ground |
| 3 | OUT | Oscillator output |
| 4 | VDD | Positive power supply |
| Center Pad | NC | Tie to GND or do not connect. |

## 3.0 NOMINAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

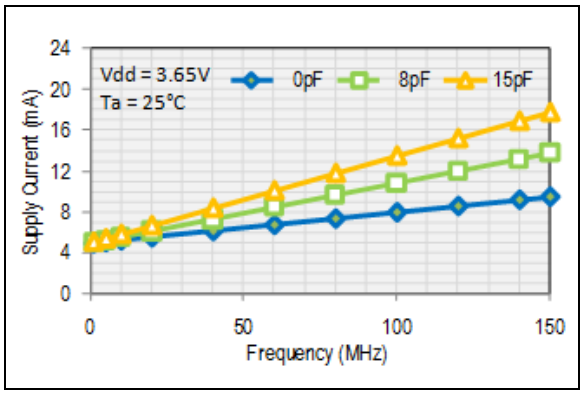


***FIGURE 3-1:*** *Supply Current.*

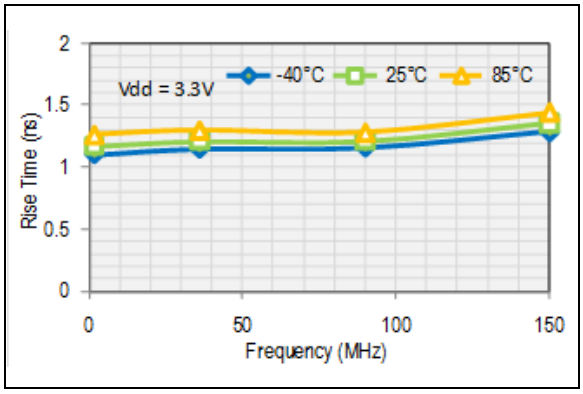


***FIGURE 3-2:*** *Rise Time.*

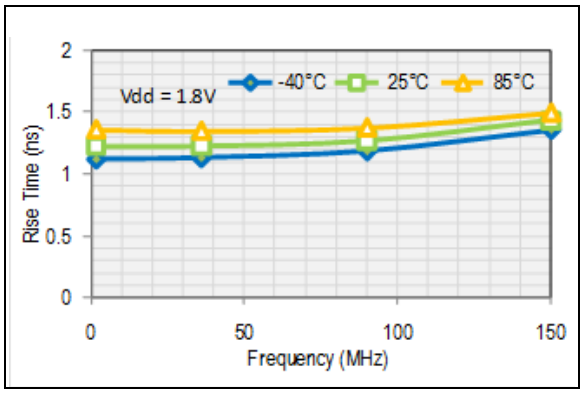


***FIGURE 3-3:*** *Rise Time.*

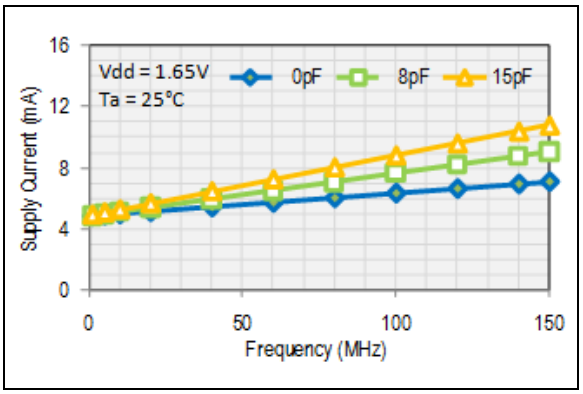


***FIGURE 3-4:*** *Supply Current.*

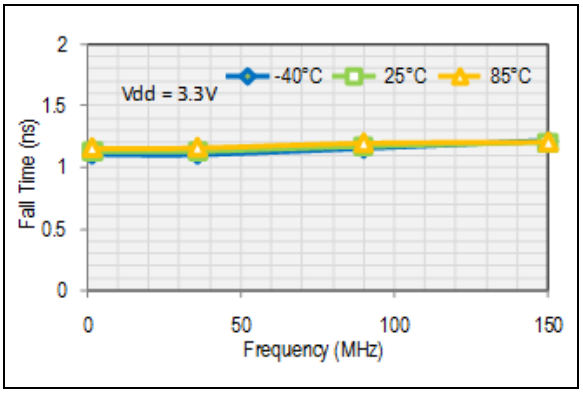


***FIGURE 3-5:*** *Fall Time.*

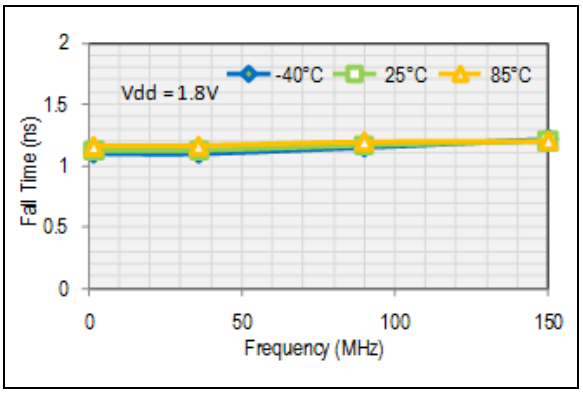


***FIGURE 3-6:*** *Fall Time.*


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## 4.0 OUTPUT WAVEFORM

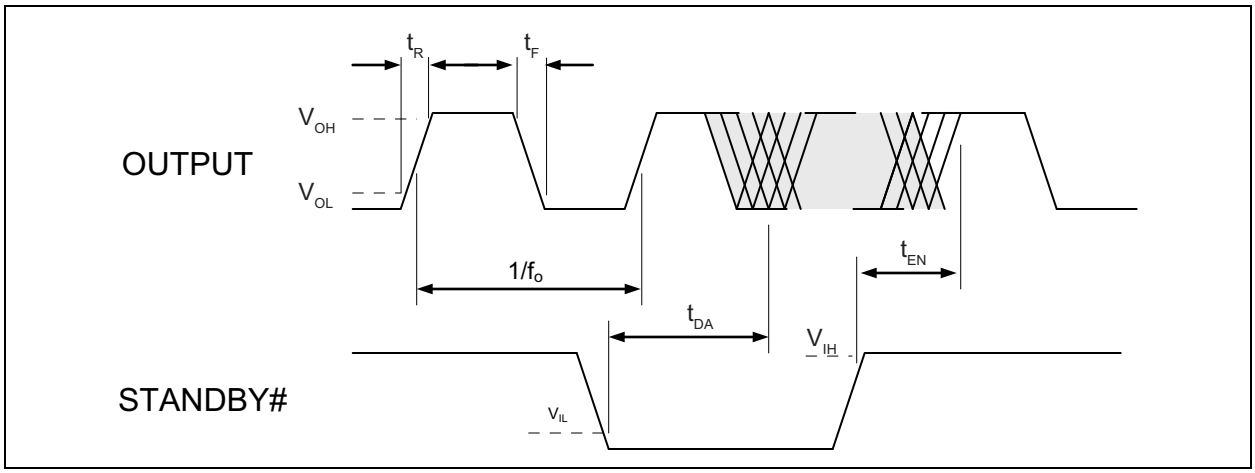


***FIGURE 4-1:*** *Output Waveform.*

### 4.1 Standby Function

| Standby# (Pin 1) | Output (Pin 3) |
|---|---|
| High Level | Output ON |
| Open (no connect) | Output ON |
| Low Level | High Impedance |

## 5.0 TEST CIRCUIT

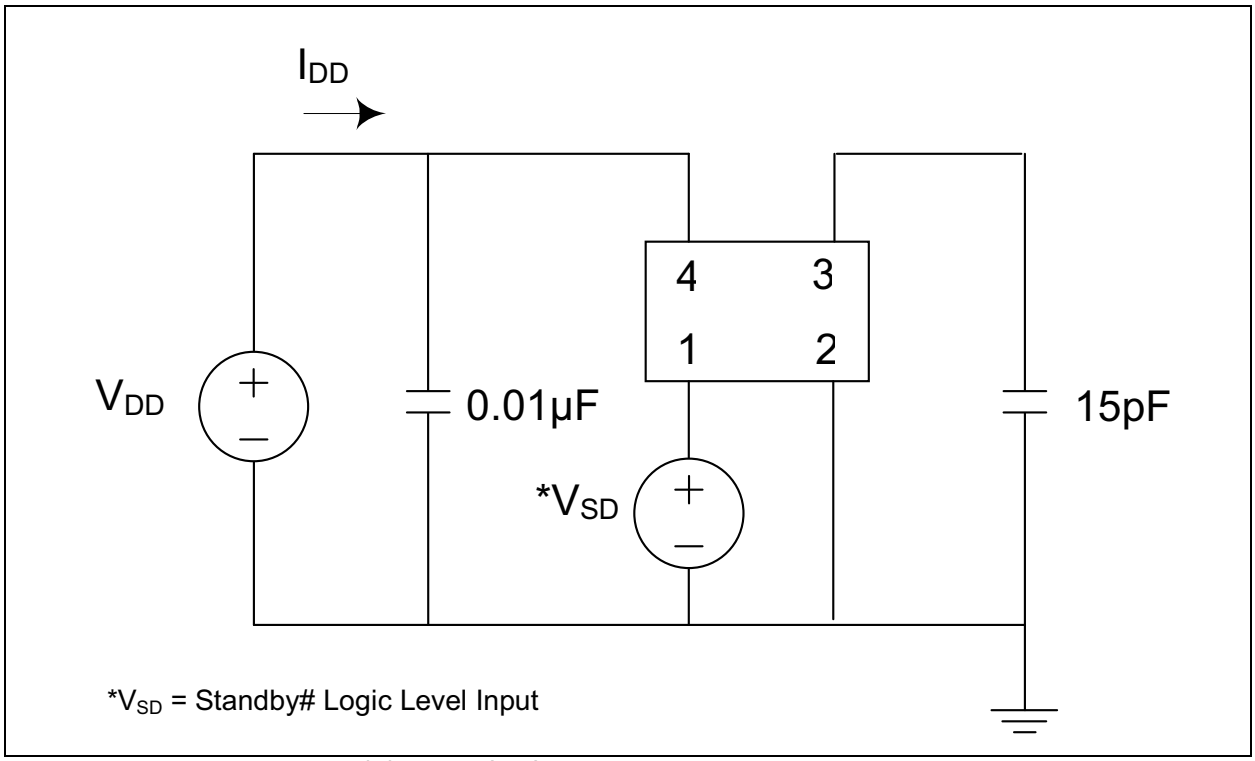


***FIGURE 5-1:*** *DSC1001/3/4 Test Circuit.*


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## 6.0 BOARD LAYOUT (RECOMMENDED)

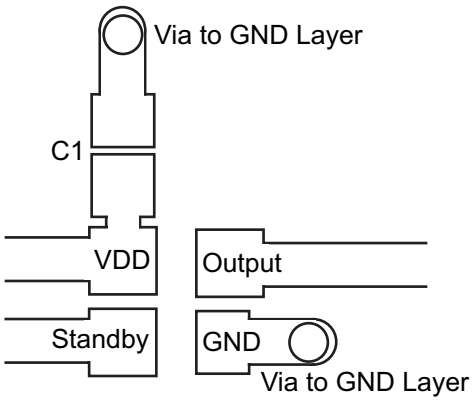


***FIGURE 6-1:*** *Recommended Board Layout for DSC1001/3/4.*

## 7.0 SOLDER REFLOW PROFILE

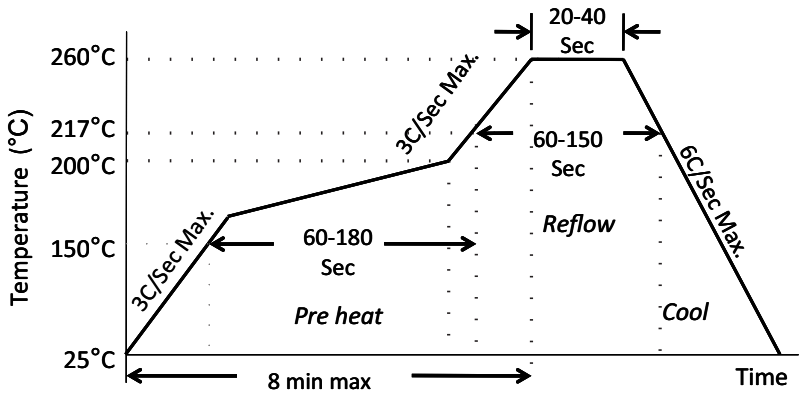


***FIGURE 7-1:*** *Solder Reflow Profile.*

| MSL 1 @ 260°C refer to JSTD-020C | |
|---|---|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/sec. max. |
| Preheat Time 150°C to 200°C | 60 to 180 sec. |
| Time maintained above 217°C | 60 to 150 sec. |
| Peak Temperature | 255°C to 260°C |
| Time within 5°C of Actual Peak | 20 to 40 sec. |
| Ramp-Down Rate | 6°C/sec. max. |
| Time 25°C to Peak Temperature | 8 minutes max. |


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# 8.0 PACKAGING INFORMATION

## 8.1 Package Marking Information

| 4-Lead CDFN/DFN* | Example |
|---|---|
| XXXXXX<br>DCPYYWW<br>0SSS<br>● | 0400000<br>DCP1121<br>0603<br>● |

| | | |
|---|---|---|
| **Legend:** | XX...X | Product code, customer-specific information, or frequency in MHz without printed decimal point |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |

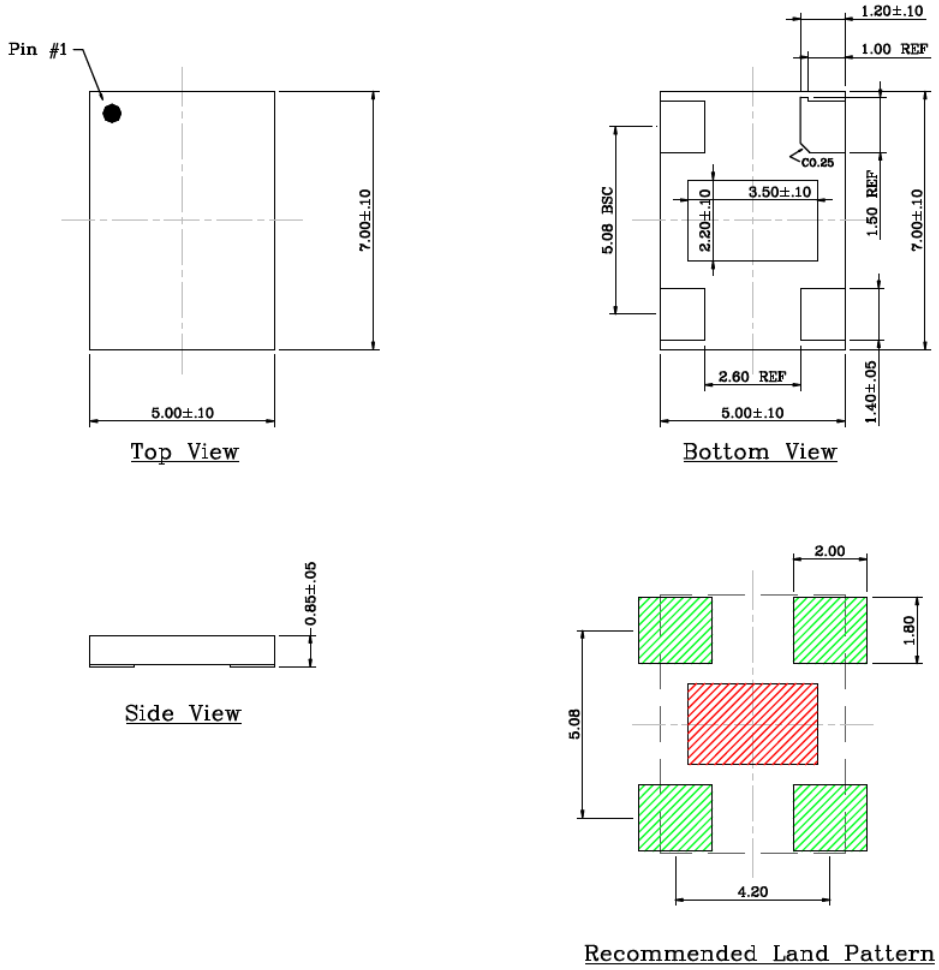
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

## 4-Lead DFN 7.0 mm x 5.0 mm Package Outline & Recommended Land Pattern

**TITLE**
4 LEAD DFN 7.0x5.0mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | DFN75-4LD-PL-1 | UNIT | MM |
|---|---|---|---|




NOTE:
1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep out area.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.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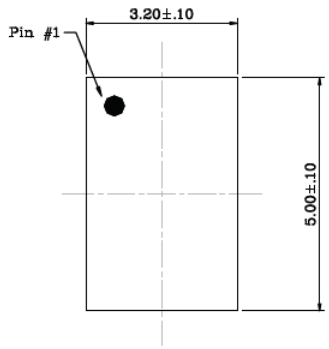
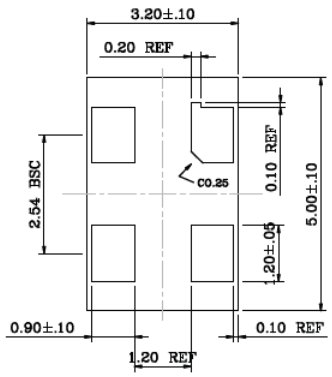
## 4-Lead CDFN 5.0 mm x 3.2 mm Package Outline & Recommended Land Pattern

**TITLE**
4 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

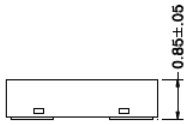
| DRAWING # | CDFN5032-4LD-PL-1 | UNIT | MM |
|---|---|---|---|



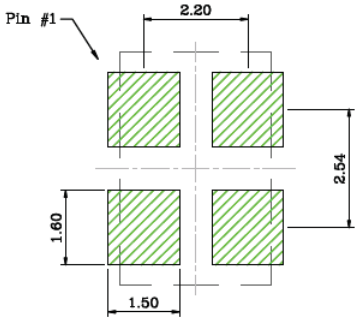

Top View




Bottom View




Side View




Recommended Land Pattern

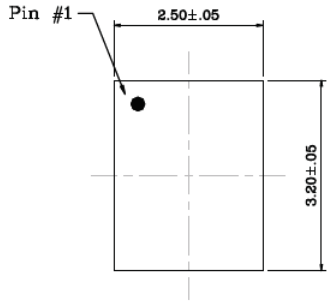
NOTE:
1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

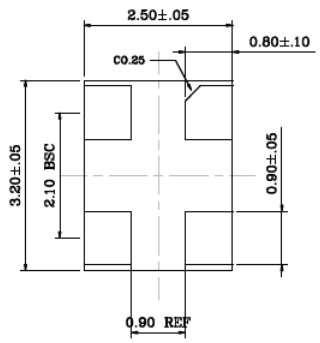
## 4-Lead CDFN 3.2 mm x 2.5 mm Package Outline & Recommended Land Pattern

**TITLE**
4 LEAD CDFN 3.2x2.5mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

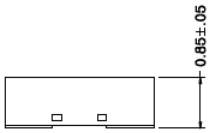
| DRAWING # | CDFN3225-4LD-PL-1 | UNIT | MM |
|---|---|---|---|



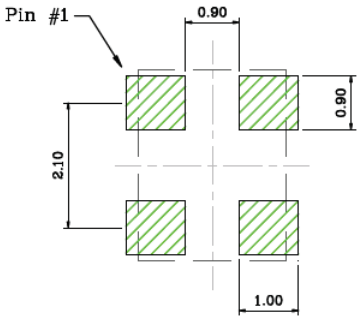

Top View




Bottom View




Side View




Recommended Land Pattern

NOTE:
1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.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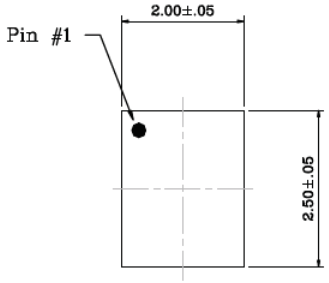
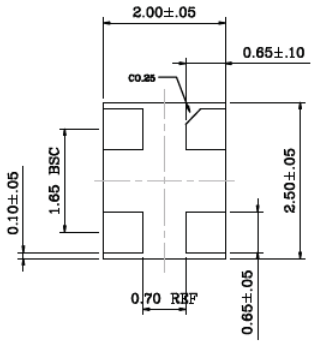
## 4-Lead CDFN 2.5 mm x 2.0 mm Package Outline & Recommended Land Pattern

**TITLE**
4 LEAD CDFN 2.5x2.0mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | CDFN2520-4LD-PL-1 | UNIT | MM |
|---|---|---|---|

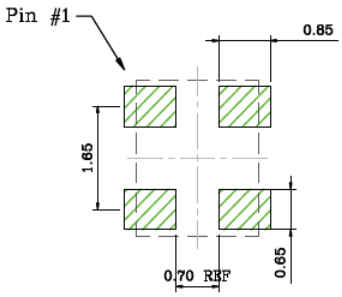



Top View




Bottom View

Side View




Recommended Land Pattern

NOTE:
1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

**NOTES:**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# APPENDIX A: REVISION HISTORY

## Revision A (September 2017)

- Converted Micrel data sheet DSC1001 to Microchip format data sheet DS20005529A.
- Minor text changes throughout.
- Added Table 2-2 for DFN package.
- Combined Micrel data sheet DSC1003 and DSC1004 into this data sheet.
  - Updated **Section 1.0 "Electrical Characteristics"** to reflect this change.
  - Updated General Description and Features to reflect this change.

## Revision B (November 2017)

- Updated $V_{OH}$ and $V_{OL}$ values in Table 1-1.

**NOTES:**


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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | X | X | X | -XXX.XXXX | X |
|---|---|---|---|---|---|
| Device | Package | Temperature Range | Stability | Frequency | Package |

| | | | |
|---|---|---|---|
| **Device:** | DSC1001/3/4: 1.8V - 3.3V Low-Power Precision CMOS Oscillator | | |
| **Package:** | A | = | 4-Lead 7.0 mm x 5.0 mm DFN |
| | B | = | 4-Lead 5.0 mm x 3.2 mm CDFN |
| | C | = | 4-Lead 3.2 mm x 2.5 mm CDFN |
| | D | = | 4-Lead 2.5 mm x 2.0 mm CDFN |
| **Temperature Range:** | E | = | –20°C to +70°C (Extended Commercial) |
| | I | = | –40°C to +85°C (Industrial) |
| | L | = | –40°C to +105°C (Extended Industrial) |
| **Stability:** | 1 | = | ±50ppm |
| | 2 | = | ±25ppm |
| | 3 | = | ±20 ppm |
| | 5 | = | ±10 ppm |
| **Frequency:** | xxx.xxxx | = | 1 MHz to 150 MHz (user-defined) |
| **Packing Option:** | <blank> | = | 110/Tube |
| | T | = | 1,000/Reel |

**Examples:**

a) DSC1001AE1-010.0000T:
1.8V - 3.3V Low-Power Precision CMOS Oscillator, 4-Lead 7.0 mm x 5.0 mm DFN, Ext. Commercial Temperature Range, ±50 ppm, 10 MHz Output Frequency, 1,000/Reel

b) DSC1003BL2-030.0000:
1.8V - 3.3V Low-Power Precision CMOS Oscillator, 4-Lead 5.0 mm x 3.2 mm CDFN, Ext. Industrial Temperature Range, ±25 ppm, 30 MHz Output Frequency, 110/Tube

c) DSC1001DE5-150.0000:
1.8V - 3.3V Low-Power Precision CMOS Oscillator, 4-Lead 2.5 mm x 2.0 mm CDFN, Ext. Commercial Temperature Range, ±10 ppm, 150 MHz Output Frequency, 110/Tube

d) DSC1004AI3-075.0000T:
1.8V - 3.3V Low-Power Precision CMOS Oscillator, 4-Lead 7.0 mm x 5.0 mm DFN, Industrial Temperature Range, ±20 ppm, 75 MHz Output Frequency, 1,000/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**


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