PIC18FXXQ43 Family Programming Specification

Introduction

This programming specification describes a SPI-based programming method for the PIC18FXXQ43 family of microcontrollers. Programming Algorithms describes the programming commands, programming algorithms and electrical specifications used in that particular programming method. APPENDIX B contains individual part numbers, device identification and checksum values, pinout and packaging information, and Configuration Words.

Important:

- This is a SPI-compliant programming method with 8-bit commands.
- The low-voltage entry code is now 32 clocks and MSb first, unlike earlier PIC18 devices, which had 33 clocks and LSb first.

1. Overview

1.1 Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage In-Circuit Serial Programming (ICSP) interface. Data can be programmed into the Program Flash Memory (PFM), Data EEPROM Memory, dedicated “User ID” locations and the Configuration Words.

1.2 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in the table below. For pin locations and packaging information, please refer to Pin Utilization table.

Table 1-1. PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ISCPCLK	ICSPCLK	I	Clock Input - Schmitt Trigger Input
ISCPDAT	ICSPDAT	I/O	Data Input/Output - Schmitt Trigger Input
$\overline{MCLR}/V_{PP}$	Program/Verify mode	I(1)	Program Mode Select
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

Note:

1. The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

1.3 Hardware Requirements

1.3.1 High-Voltage ICSP Programming

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for V_{DD} and one for the $\overline{MCLR}/V_{PP}$ pin.

1.3.2 Low-Voltage ICSP Programming

In Low-Voltage ICSP mode, the device can be programmed using a single V_{DD} source in the device operating range. The $\overline{MCLR}/V_{PP}$ pin does not have to be brought to programming voltage, but can instead be left at the normal operating voltage.

1.3.2.1 Single-Supply ICSP Programming

The device's LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled). The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the $\overline{MCLR}/V_{PP}$ pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and can be used to program the device.

Important:

- The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}/V_{PP}$ pin.
- While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled, regardless of the MCLRE bit. Also, the $\overline{MCLR}$ pin can no longer be used as a general purpose input.

1.4 Write and/or Erase Section

Erasing or writing is selected according to the command used to begin operation (see Table 3-1). The terminologies used in this document, related to erasing/writing to the program memory, are defined in the table below.

Table 1-2. PROGRAMMING TERMS

Term	Definition
Programmed Cell	A memory cell at logic '0'
Erased Cell	A memory cell at logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic erase and/or write

1.4.1 Erasing Memory

Memory is erased by 128-word sectors or in bulk, where 'bulk' includes many subsets of the total memory space. The duration of the data memory erase is determined by the size of data memory. All Bulk ICSP Erase commands have minimum V_{DD} requirements, which are higher than the Sector Erase and Write requirements.

Sector erasing pertains to PFM and User ID memory only. Configuration and data memory should be erased by the Bulk Erase command. For self-write operations, each byte write to data memory includes an automatic erase cycle for the location about to be programmed.

1.4.2 Writing Memory

Memory is written one word at a time. The duration of the write is determined internally.

Note: The size of the word is 16 bits for the Program Flash Memory and is 8 bits for the EEPROM, but the same 24-bit payload is used for both memory regions.

2. Memory Map

This section provides details about how the program memory and EEPROM is organized for this device.

Figure 2-1. Program and Data EEPROM Memory Map

Rev. 40-000101E
4/20/2017

Address	Device			
	PIC18Fx4Q43	PIC18Fx5Q43	PIC18Fx6Q43	PIC18Fx7Q43
00 0000h to 00 3FFFh	Program Flash Memory (8 KW)(1)	Program Flash Memory (16 KW)(1)	Program Flash Memory (32 KW)(1)	Program Flash Memory (64 KW)(1)
00 4000h to 00 7FFFh	Not Present(2)			
00 8000h to 00 FFFFh		Not Present(2)		
01 0000h to 01 FFFFh			Not Present(2)	
02 0000h to 1F FFFFh				Not Present(2)
20 0000h to 20 001Fh	User IDs (32 Words)(3)			
20 0020h to 2B FFFFh	Reserved			
2C 0000h to 2C 00FFh	Device Information Area (DIA)(3)(5)			
2C 0100h to 2F FFFFh	Reserved			
30 0000h to 30 0009h	Configuration Words (3)			
30 0009h to 37 FFFFh	Reserved			
38 0000h to 38 03FFh	Data EEPROM (1024 Bytes)			
38 0400h to 3B FFFFh	Reserved			
3C 0000h to 3C 000Ah	Device Configuration Information(3)(4)(5)			
3C 000Bh to 3F FFFBh	Reserved			
3F FFFCh to 3F FFFDh	Revision ID (1 Word)(3)(4)(5)			
3F FFFEh to 3F FFFFh	Device ID (1 Word)(3)(4)(5)			

Note 1: Storage Area Flash is implemented as the last 128 Words of User Flash, if enabled.

2: The addresses do not roll over. The region is read as '0'.

3: Not code-protected.

4: Hard-coded in silicon.

5: This region cannot be written by the user and it's not affected by a Bulk Erase.

2.1 User ID Location

A user may store identification information (User ID) in 32 designated locations. The User ID locations are mapped to 20 0000h-20 001Fh. Each location is 16 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

2.2 Device/Revision ID

The 16-bit Device ID Word is located at 3F FFFEh and the 16-bit Revision ID is located at 3F FFFCh. These locations are read-only and cannot be erased or modified. See 2.5 DEVICE ID and 2.6 REVISION ID for more details.

2.3 Device Configuration Information (DCI)

The Device Configuration Information (DCI) is a dedicated region in the memory that holds information about the device which is useful for programming and bootloader applications. The data stored in this region is read-only and cannot be modified/erased. Refer to the table below for complete DCI table addresses and description.

Table 2-1. DEVICE CONFIGURATION INFORMATION

Address	Name	Description	Value				Units
			PIC18F24/44/54Q43	PIC18F25/45/55Q43	PIC18F26/46/56Q43	PIC18F27/47/57Q43	
3C 0000h	ERSIZ	Erase Row Size	128				Words
3C 0002h	WLSIZ	Number of write latches per row	0				Bytes
3C 0004h	URSIZ	Number of user erasable pages	64	128	256	512	Rows
3C 0006h	EESIZ	Data EEPROM memory size	1024				Bytes
3C 000h	PCNT	Pin Count	28/40(1)/48	28/40(1)/48	28/40(1)/48	28/40(1)/48	Pins

Note:

1. Pin Count value of 40 is used for 44-pin parts as well.

2.4 Configuration Words

The devices have five Configuration Words, starting at address, 30 0000h. Configuration bits enable or disable specific features, placing these controls outside the normal software process, and they establish configured values prior to the execution of any software.

In terms of programming, these important Configuration bits should be considered:

1. **LVP: Low-Voltage Programming Enable bit**
   - 1 = ON: Low-Voltage Programming is enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
   - 0 = OFF: High voltage on $\overline{MCLR}/V_{PP}$ must be used for programming.

   It is important to note that the LVP bit cannot be written (to '0') while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the configuration state. For more information, see 3.1.2 LOW-VOLTAGE Programming (LVP) Mode.
2. **MCLRE: Master Clear ($\overline{MCLR}$) Enable bit**
   - If LVP = 1: RE3 pin function is $\overline{MCLR}$
   - If LVP = 0
     - 1 = $\overline{MCLR}$ pin is $\overline{MCLR}$
     - 0 = $\overline{MCLR}$ pin function is a port-defined function
3. **$\overline{CP}$: User NVM Program Memory Code Protection bit**
   - 1 = OFF: User NVM code protection is disabled
   - 0 = ON: User NVM code protection is enabled

For more information on code protection, see 3.3 Code Protection.

2.5 DEVICE ID

Name: DEVICE ID

Device ID Register

Bit	15	14	13	12	11	10	9	8
	DEV[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	q	q	q	q	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	q	q	q	q	q	q	q	q

Bits 15:0 – DEV[15:0]
Device ID bits

Device	Device ID
PIC18F24Q43	7360h
PIC18F25Q43	73C0h
PIC18F26Q43	7420h
PIC18F27Q43	7480h
PIC18F44Q43	7380h
PIC18F45Q43	73E0h
PIC18F46Q43	7440h
PIC18F47Q43	74A0h
PIC18F54Q43	73A0h
PIC18F55Q43	7400h
PIC18F56Q43	7460h
PIC18F57Q43	74C0h

2.6 REVISION ID

Name: REVISION ID

Revision ID Register

Bit	15	14	13	12	11	10	9	8
	1010[3:0]				MJRREV[5:2]			
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	0	1	0	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	MJRREV[1:0]		MNRREV[5:0]					
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	q	q	q	q	q	q	q	q

Bits 15:12 – 1010[3:0] Read as ‘1010’
These bits are fixed with value ‘`1010`’ for all devices in this family.

Bits 11:6 – MJRREV[5:0] Major Revision ID bits
These bits are used to identify a major revision. (A0, B0, C0, etc.).
Revision A = `b'00 0000'`

Bits 5:0 – MNRREV[5:0] Minor Revision ID bits
These bits are used to identify a minor revision.
Revision A0 = `b'00 0000'`

3. Programming Algorithms

3.1 Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK pins are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state, all I/Os are automatically configured as high-impedance inputs and the Program Counter (PC) is cleared.

3.1.1 HIGH-VOLTAGE Program/Verify Mode Entry and Exit

There are two different modes of entering Program/Verify mode via high voltage:

- V_{PP}-First Entry mode
- V_{DD}-First Entry mode

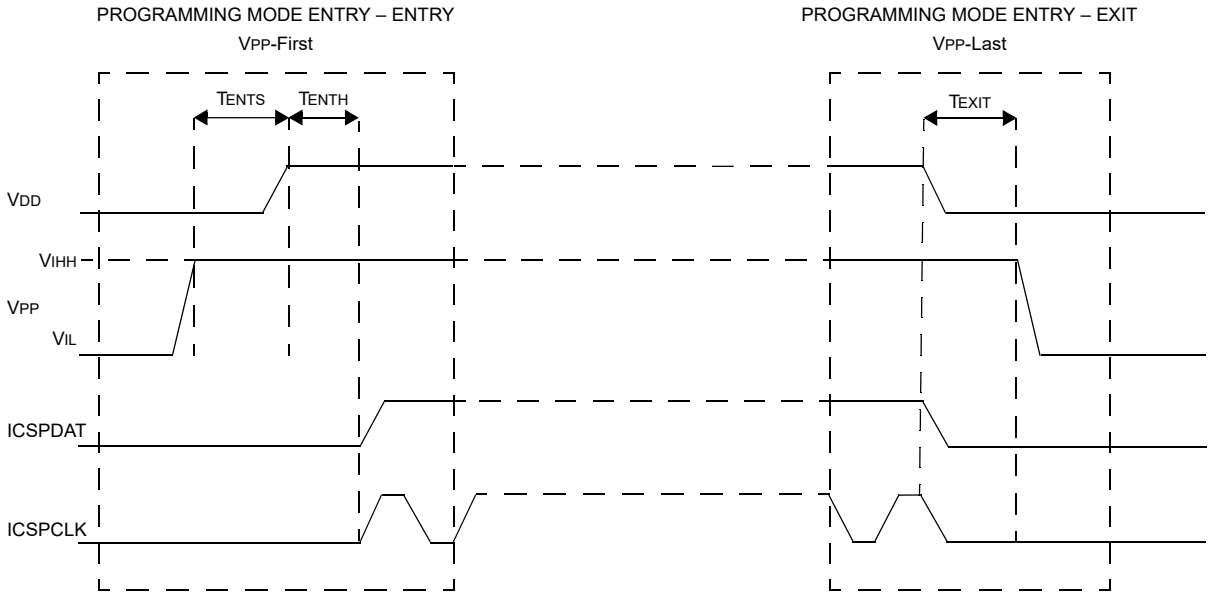
3.1.1.1 V_{PP}-First Entry Mode

To enter Program/Verify mode via the V_{PP}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V_{IHH}.
3. Raise the voltage on V_{DD} from 0V to the desired operating voltage.

The V_{PP}-First Entry mode prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has already been programmed to have $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer disabled ($\overline{PWRTE}$ = 0) and the internal oscillator selected, the device will execute code immediately. V_{PP}-First Entry mode is strongly recommended as it prevents user code from executing. See the timing diagram in Figure 3-1.

Figure 3-1. PROGRAMMING ENTRY AND EXIT MODES – V_{PP}-First and Last



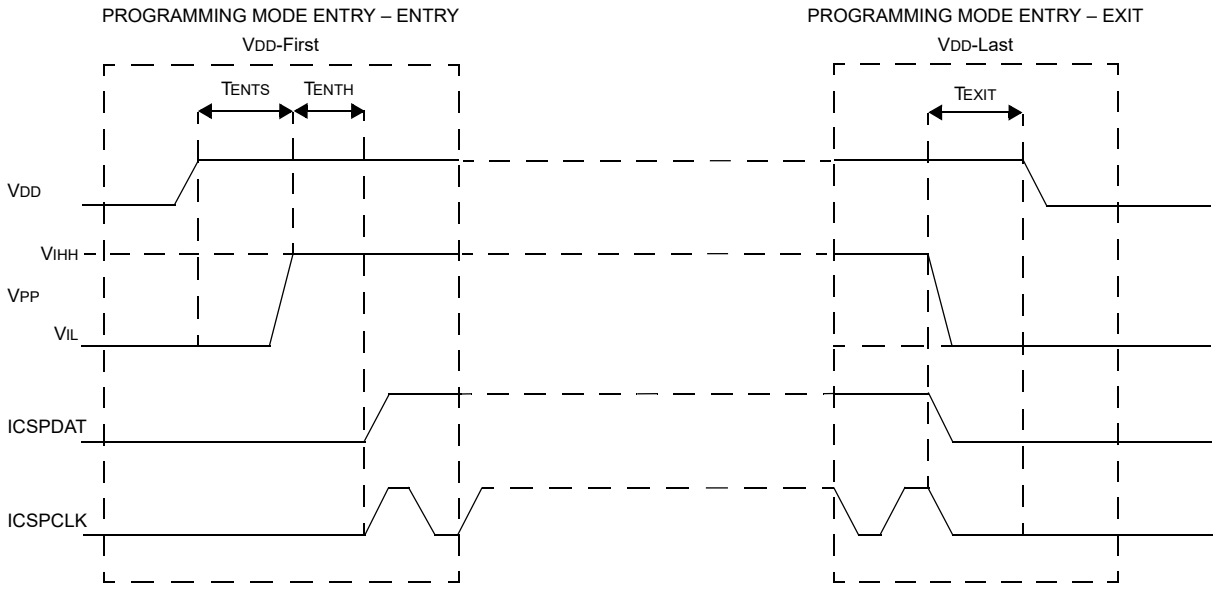
3.1.1.2 V_{DD}- First Entry Mode

To enter Program/Verify mode via the V_{DD}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on V_{DD} from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V_{DD} or below to V_{IHH}.

The V_{DD}-First Entry mode is useful for programming the device when V_{DD} is already applied, for it is not necessary to disconnect V_{DD} to enter Program/Verify mode. See the timing diagram in Figure 3-2.

Figure 3-2. PROGRAMMING ENTRY AND EXIT MODES – VDD-First and Last



3.1.1.3 Program/Verify Mode Exit

To exit Program/Verify mode, lower $\overline{MCLR}$ from V_{IHH} to V_{IL}. V_{PP}-First Entry mode should use V_{PP}-Last Exit mode (see Figure 3-1). V_{DD}-First Entry mode should use V_{DD}-Last Exit mode (see Figure 3-2).

3.1.2 LOW-VOLTAGE Programming (LVP) Mode

The Low-Voltage Programming mode allows the devices to be programmed using V_{DD} only, without high voltage. When the LVP bit in the Configuration Word register is set to '1', the Low-Voltage ICSP Programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A **32-bit key sequence** is presented on ICSPDAT, clocked by ICSPCLK. The LSb of the pattern is a "don't care `x`". The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required before the pattern detect goes active.

The key sequence is a specific 32-bit pattern, '`32'h4d434850`' (more easily remembered as **MCHP** in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the Most Significant Byte must be shifted in first. Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained. For Low-Voltage Programming timing, see Figure 3-3 and Figure 3-4.

Figure 3-3. LVP Entry (Powering Up)

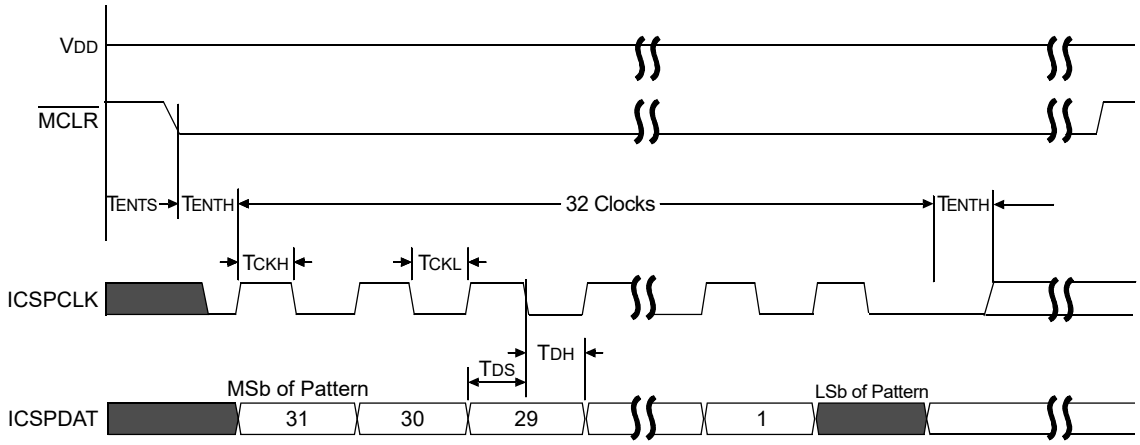
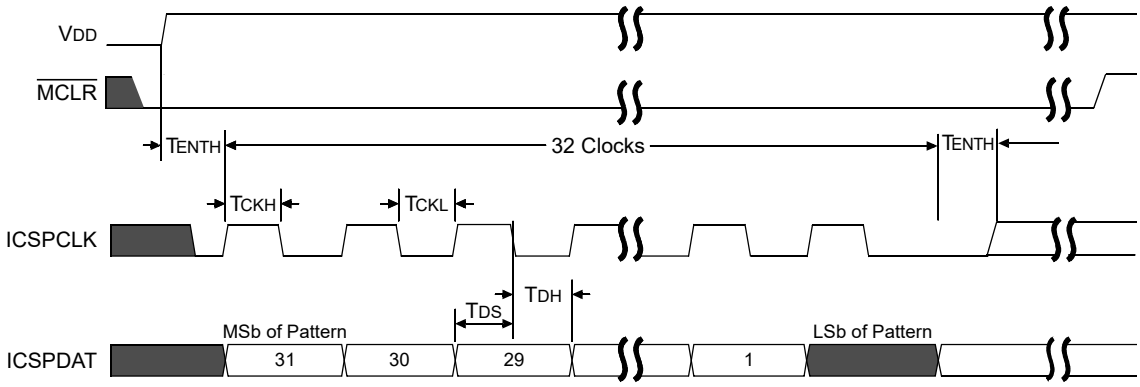


Figure 3-4. LVP Entry (Powered)



Exiting Program/Verify mode is done by raising $\overline{MCLR}$ from below V_{IL} to V_{IH} level (or higher, up to V_{DD}).

Important:
To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

3.1.3 Program/Verify Commands

Once a device has entered ICSP Program/Verify mode (using either high-voltage or LVP entry), the programming host device may issue six commands to the microcontroller, each eight bits in length. The commands are summarized in Table 3-1. The commands are used to erase or program the device based on the location of the Program Counter (PC).

Some of the 8-bit commands also have an associated data payload (such as Load PC Address and Read Data from NVM).

If the host device issues an 8-bit command byte that has an associated data payload, the host device is responsible for sending an additional 24 clock pulses (for example, three 8-bit bytes) in order to send or receive the payload data associated with the command.

The payload field size is used so as to be compatible with many 8-bit SPI-based systems. Within each 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad

bits, followed by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted, Most Significant bit (MSb) first.

When the programming device issues a command that involves a host to microcontroller payload (for example, Load PC Address), the Start, Stop and Pad bits should all be driven by the programmer to '0'. When the programming host device issues a command that involves microcontroller to host payload data (for example, Read Data from NVM), the Start, Stop and Pad bits should be treated as "don't care" bits and the values should be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host should wait a specified minimum amount of delay (which is command-specific) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

Table 3-1. ICSP™ COMMAND SET SUMMARY(1)

Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb … LSb)	Hex			
Load PC address	1000 0000	80	Yes	T_{DLY}	Payload Value = PC
Bulk Erase	0001 1000	18	Yes	T_{ERAB}	The payload carries the information of the regions that need to be bulk-erased.
Sector Erase Program Memory	1111 0000	F0	No	T_{ERAS}	The sector addressed by the MSbs of the PC is erased; LSbs are ignored
Read Data from NVM	1111 11J0	FC/FE	Yes	T_{DLY}	Data output '0' if code-protect is enabled:J = 0: PC is unchangedJ = 1: PC = PC + n(2) after reading
Increment Address	1111 1000	F8	No	T_{DLY}	PC = PC + n(2)

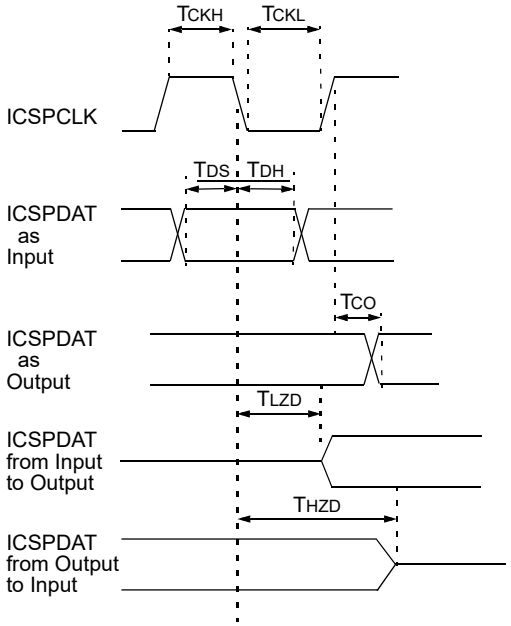
.....continued

Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb … LSb)	Hex			
Program Data	11J0 0000	C0/E0	Yes	T_{PROG}	Payload value = Data WordJ = 0: PC is unchangedJ = 1: PC = PC + n after writing

Important:

1. All clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller should latch received ICSPDAT values on the falling edge of the ICSPCLK line. When the microcontroller receives ICSPDAT line values from the host programmer, the ICSPDAT values must be valid a minimum of T_{DS} before the falling edges of ICSPCLK and should remain valid for a minimum of TDH after the falling edge of ICSPDAT. See Figure 3-5.
2. PC is incremented by n = 1 for data memory, Configuration Words and n = 2 for all other regions.

Figure 3-5. Clock and Data Timing



3.1.3.1 Program Data

The Program Data command is used to program one NVM word (for example, one 16-bit instruction word for program memory/configuration memory/User ID memory or one 8-bit data for a Data EEPROM Memory address). The payload data is written into program or EEPROM memory immediately after the Programming Data command is issued (see 3.2 Programming Algorithms). Depending on the value of bit 5 of the command, the PC may or may not be incremented (see Table 3-1).

Figure 3-6. PROGRAM DATA (PROGRAM MEMORY, USER ID AND CONFIGURATION)

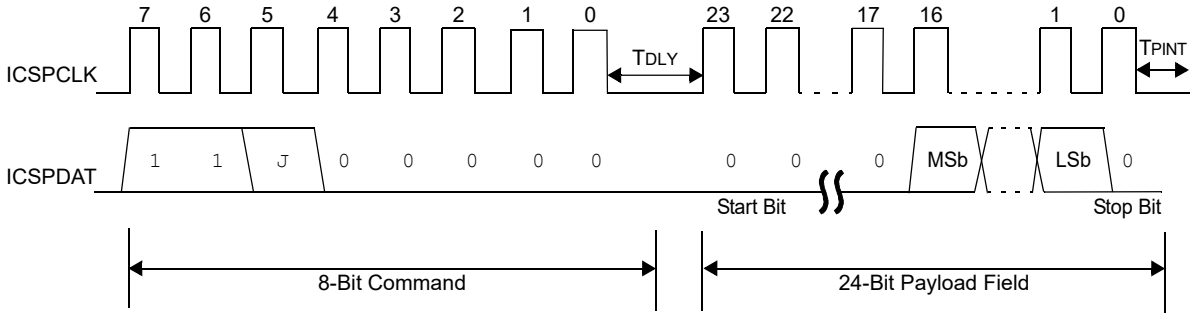
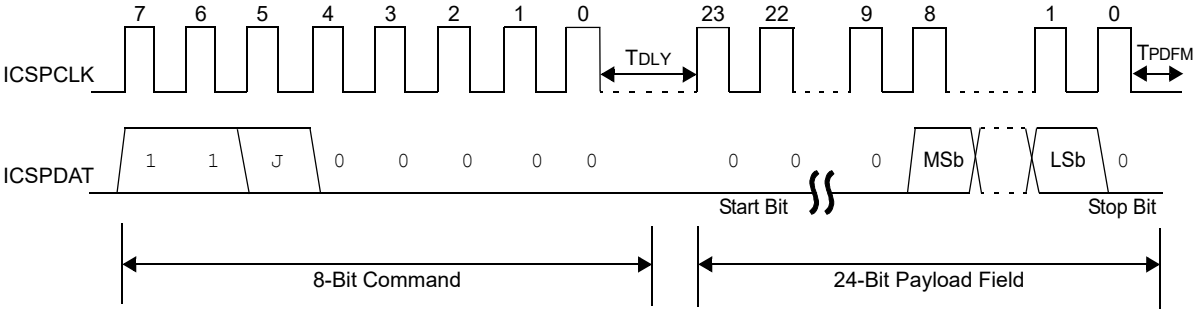


Figure 3-7. PROGRAM DATA (DATA EEPROM)



3.1.3.2 Read Data from NVM

The Read Data from NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of the ICSP data payload clock and it will revert to Input mode (high-impedance) after the 24th falling edge of the ICSP data payload clock. The Start and Stop bits are only one-half of a bit time wide; therefore, they should be ignored by the host programmer device, since the latched value may be indeterminate. Additionally, the host programmer device should only consider the MSb to LSb payload bits as valid and should ignore the values of the Pad bits. If the memory region is code-protected ($\overline{CP}$ or $\overline{DP}$), the data will be read as zeros (see Figure 3-8 and Figure 3-9). Depending on the value of bit 1 of the command, the PC may or may not be incremented (see Table 3-1). The Read Data from NVM command can be used to read data for Program Flash Memory (see Figure 3-8) or the Data EEPROM Memory (see Figure 3-9).

Figure 3-8. READ DATA FROM NVM (PFM)

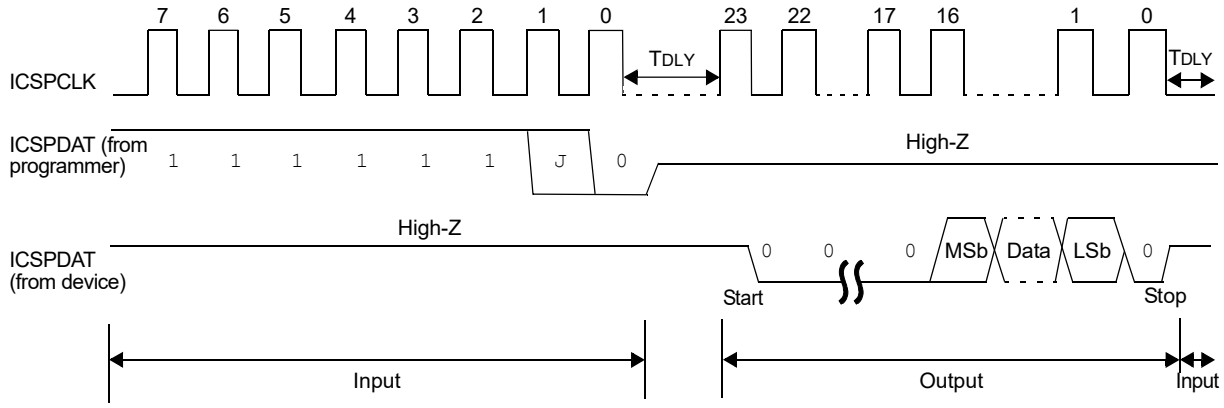
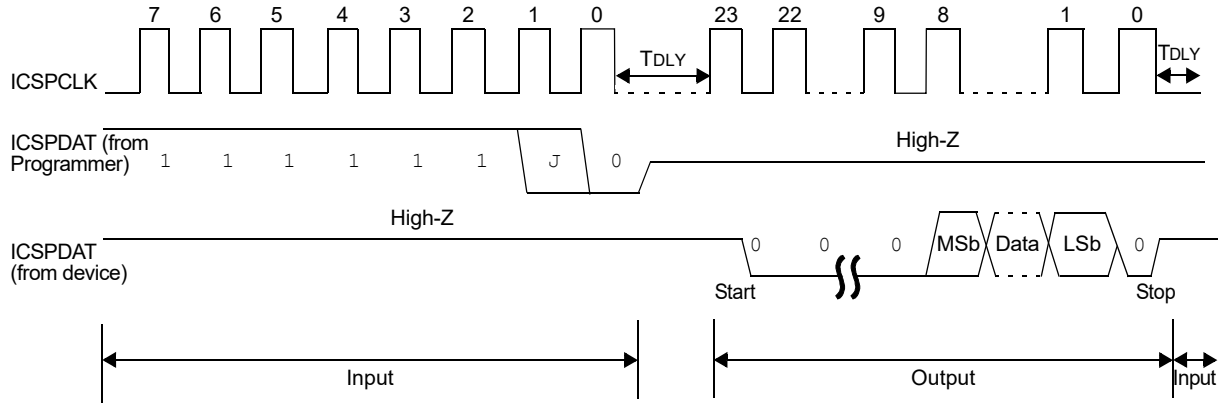


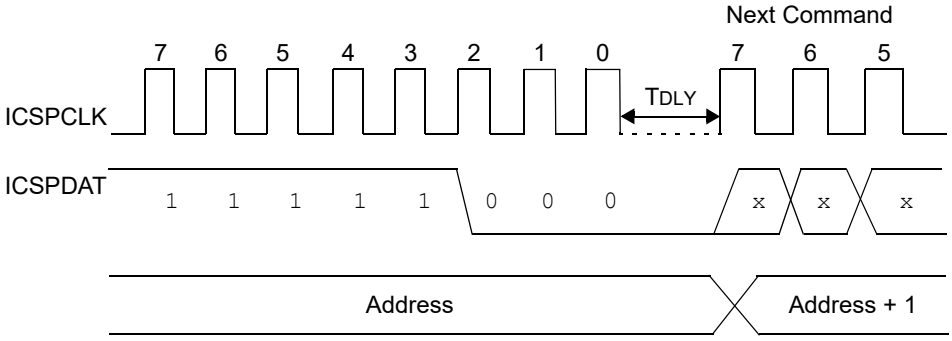
Figure 3-9. READ DATA FROM NVM (DATA EEPROM)



3.1.3.3 Increment Address

The address is incremented when this command is received. Depending on the current value of the Program Counter, the increment varies. If the PC points to PFM, then the PC is incremented by 2; if the PC points to data EEPROM, then it is incremented by 1. It is not possible to decrement the address. To reset the Program Counter, the user must use the Load PC Address command.

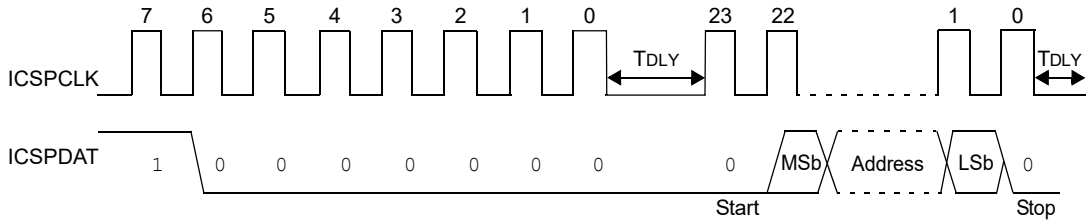
Figure 3-10. INCREMENT ADDRESS



3.1.3.4 Load PC Address

The PC value is set using the supplied data. The address implies the memory panel (PFM or Data EEPROM Memory or Configuration memory) to be accessed (see Figure 3-11).

Figure 3-11. LOAD PC ADDRESS



3.1.3.5 Bulk Erase

The Bulk Erase command is used to completely erase different memory regions. The area selection is a bit-field in the payload.

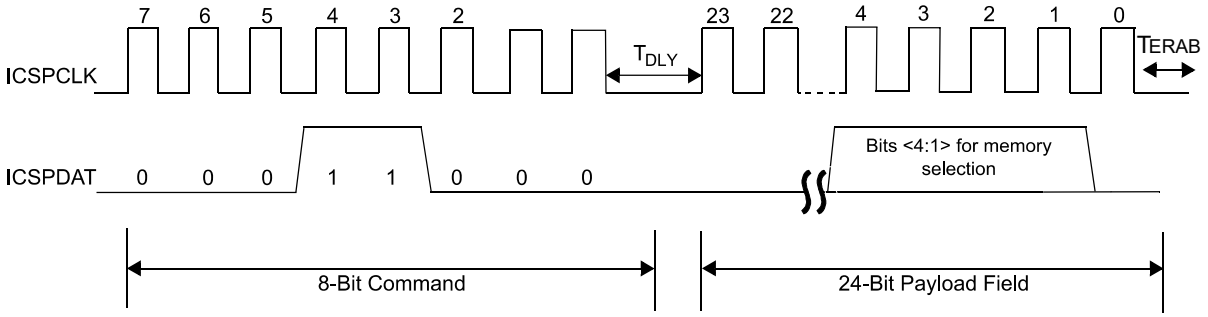
By setting the following bits of the payload, the corresponding memory regions can be bulk erased. Setting multiple bits is valid.

1. Bit 1: Data EEPROM
2. Bit 2: Flash memory
3. Bit 3: User ID memory
4. Bit 4: Configuration memory

Important: If the device is code-protected and a Bulk Erase command for the configuration memory is issued, all other regions are also bulk erased.

After receiving the Bulk Erase command, the erase will complete after the time interval T_{ERAB}. See Figure 3-12 for Bulk Erase command structure.

Figure 3-12. BULK ERASE MEMORY

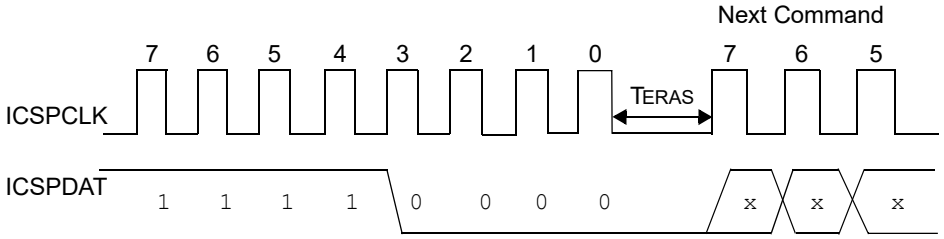


3.1.3.6 Sector Erase Program Memory

The Sector Erase Program Memory command will erase an individual sector based on the current address of the Program Counter. If the program memory is code-protected, the Sector Erase Memory command will be ignored. The Bulk Erase command must be used to erase code-protected memory.

The Flash memory sector defined by the current PC will be erased. The user must wait T_{ERAS} for erasing to be complete (see Figure 3-13). Sector Erase may be used for program memory and User ID regions only. Configuration and data regions must be erased with the Bulk Erase method.

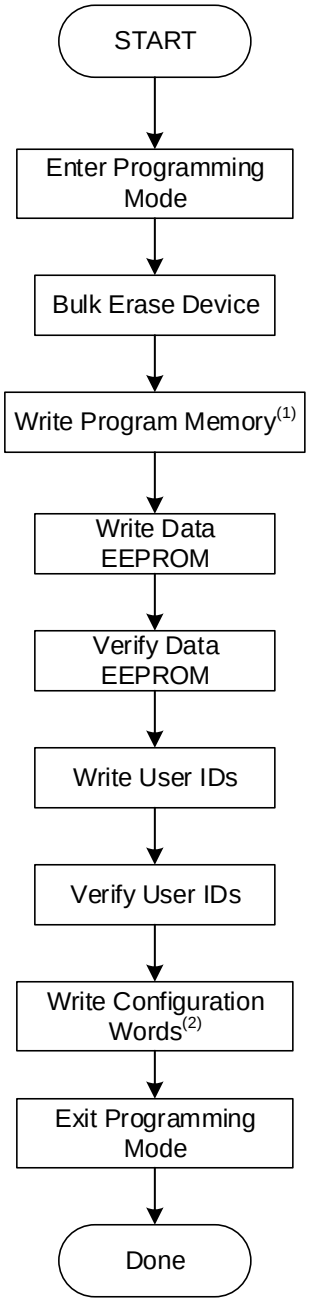
Figure 3-13. SECTOR ERASE MEMORY



3.2 Programming Algorithms

The Program Flash Memory, User ID and Configuration regions are programmed one word at a time. The EEPROM memory is programmed one byte at a time.

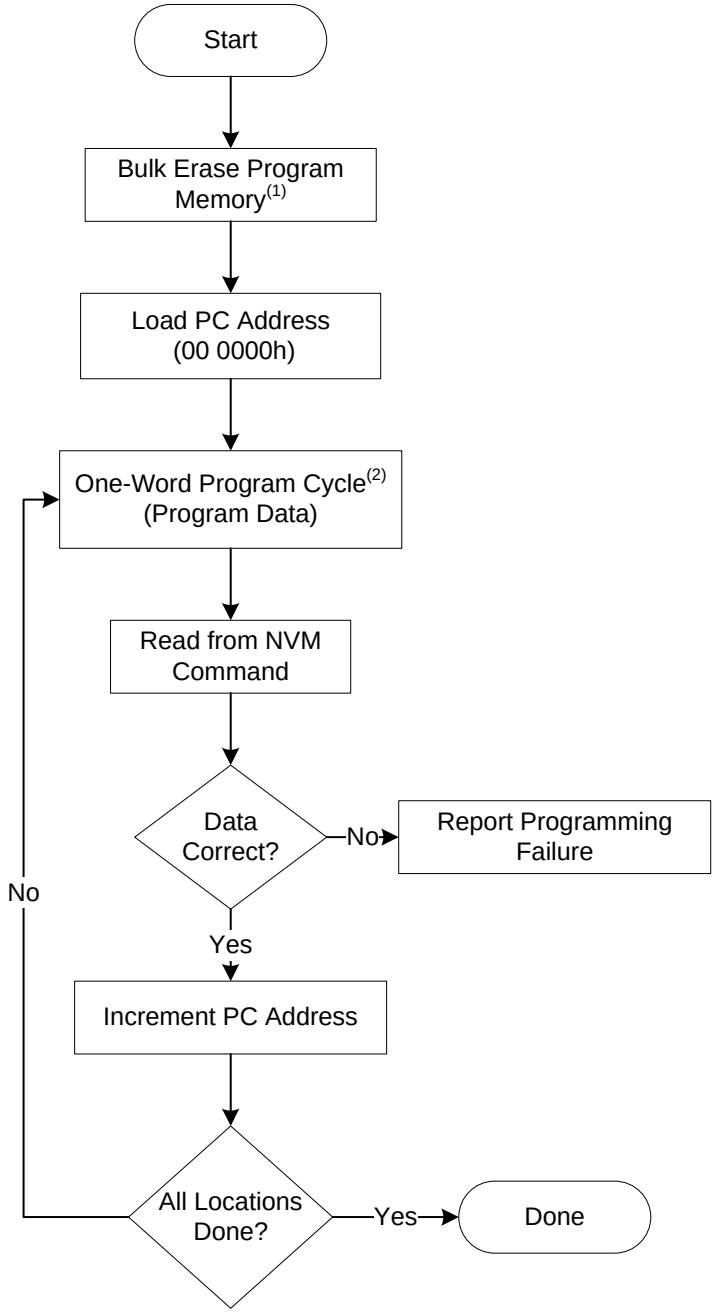
Figure 3-14. DEVICE PROGRAM/VERIFY FLOWCHART



Note:

1. See Figure 3-15.
2. See Figure 3-17.

Figure 3-15. PROGRAM MEMORY FLOWCHART



Note:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 3-18.

Figure 3-16. ONE-WORD PROGRAM CYCLE

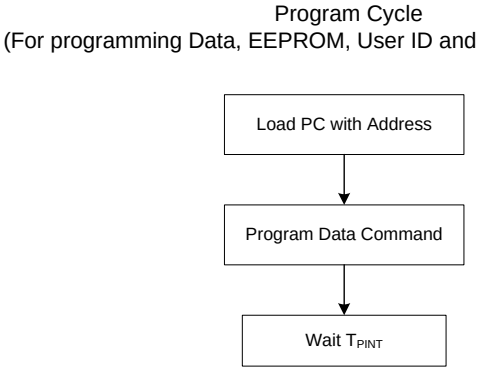
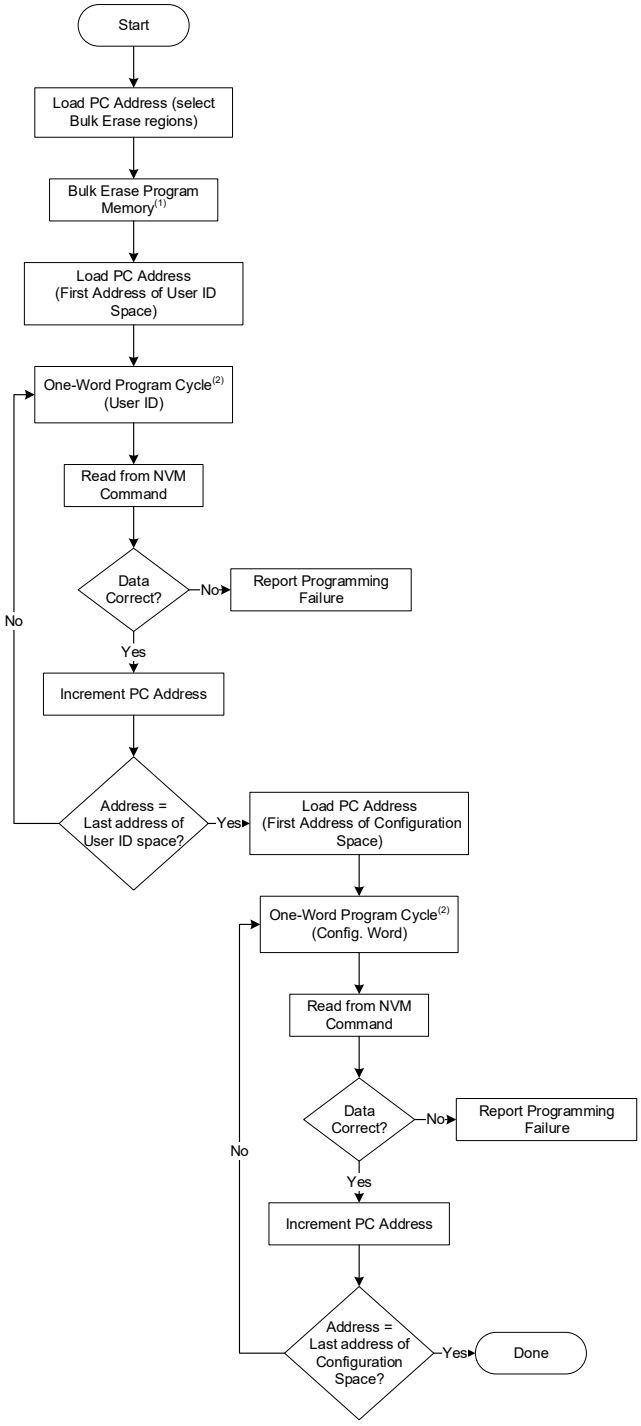


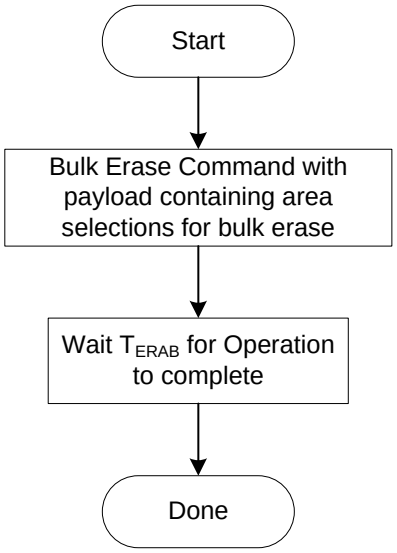
Figure 3-17. USER ID AND CONFIGURATION MEMORY PROGRAM FLOWCHART



Note:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. See Figure 3-16.

Figure 3-18. BULK ERASE FLOWCHART



3.3 Code Protection

Code protection is controlled using the $\overline{CP}$ bit. When code protection is enabled, all program memory and Data EEPROM locations read as '0'. Further programming is disabled for the program memory and Data EEPROM until a Bulk Erase operation is performed on the configuration memory region. Program memory and Data EEPROM can still be programmed and read during program execution.

The User ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

The only way to disable code protection is to use the Bulk Erase Program Memory command with bit 4 of the payload set to '1'. This will clear the disable code protection and also erase all the memory locations.

3.4 Hex File Usage

3.4.1 Embedding Configuration Information in the HEX File

To allow portability of code, a programmer is required to read the Configuration Word locations from the Hex file. If Configuration Word information is not present in the Hex file, then a simple warning message should be issued. Similarly, when saving a Hex file, all Configuration Word information must be included. An option to not include the Configuration Word information may be provided. When embedding Configuration Word information in the Hex file, it should start at address 30 0000h.

Important:
Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

3.4.2 Embedding Data EEPROM Information in the HEX File

To allow portability of code, a programmer is required to read the data EEPROM information from the Hex file. If data EEPROM information is not present, a simple warning message should be issued. Similarly,

when saving a Hex file, all data EEPROM information must be included. An option to not include the data EEPROM information may be provided. When embedding data EEPROM information in the Hex file, it should start at address 38 0000h.

Important:
Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

3.5 Checksum Computation

The checksum is calculated by two different methods, dependent on the setting of the $\overline{CP}$ Configuration bit. Refer to 6. APPENDIX B for checksum computation examples.

3.5.1 Program Code Protection Disabled

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data, starting at address 00 0000h, up to the maximum user-addressable location. Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

3.5.2 Program Code Protection Enabled

When the MPLAB® IDE check box for "Configure → ID Memory... → Use Unprotected Checksum" is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the User ID. The unprotected checksum is distributed, one nibble per ID location. Each nibble is right justified.

The checksum of a code-protected device is computed in the following manner:

- All of the User ID locations are added to create the sum ID
- The sum ID is then added to the Configuration bits
- All unimplemented Configuration bits are masked to '0'

Important:
The checksum calculation differs depending on the code-protect setting. Since the code memory locations read out differently, depending on the code-protect setting, the examples in 6. APPENDIX B describe how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Word and ID locations can always be read.

4. Electrical Specifications

Refer to the device specific data sheet for absolute maximum ratings.

Table 4-1. AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at +25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/ Comments**
Programming Supply Voltages and Currents						
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	1.80	—	5.50	V	**(Note 1)**
V_{PEW}	Read/Write and Sector Erase Operations	V_{DDMIN}	—	V_{DDMAX}	V	
V_{BE}	Bulk Erase Operations	V_{BORMAX}	—	V_{DDMAX}	V	**(Note 2)**
I_{DDI}	Current on V_{DD}, Idle	—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming	—	—	10	mA	
I_{PP}	**V_{PP}**					
	Current on $\overline{MCLR}/V_{PP}$	—	—	600	µA	
V_{IHH}	High Voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify Mode Entry	7.9	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ Rise Time (V_{IL} to V_{IHH}) for Program/Verify Mode Entry	—	—	1.0	µs	
V_{IH}	**I/O Pins**					
	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input High Level	0.8 V_{DD}	—	V_{DD}	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input Low Level	V_{SS}	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT Output High Level	V_{DD}-0.7	—	—	V	I_{OH} = 3 mA, V_{DD} = 3.0V
V_{OL}	ICSPDAT Output Low Level	—	—	V_{SS} + 0.6	V	I_{OL} = 6 mA, V_{DD} = 3.0V
Programming Mode Entry and Exit						
T_{ENTS}	Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time before V_{DD} or $\overline{MCLR}$↑	100	—	—	ns	
T_{ENTH}	Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time before V_{DD} or $\overline{MCLR}$↑	1	—	—	ms	
Serial Program/Verify						

.....continued

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at +25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/ Comments
T_{CKL}	Clock Low Pulse Width	100	—	—	ns	
T_{CKH}	Clock High Pulse Width	100	—	—	ns	
T_{DS}	Data in Setup Time before Clock↓	100	—	—	ns	
T_{DH}	Data in Hold Time after Clock↓	100	—	—	ns	
T_{CO}	Clock↑ to Data Out Valid (during a Read Data command)	0	—	80	ns	
T_{LZD}	Clock↓ to Data Low-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{HZD}	Clock↓ to Data High-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{DLY}	Data Input not Driven to Next Clock Input (delay required between command/data or command/command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase Cycle Time	—	—	11	ms	Program, Config and ID
T_{ERAS}	Sector Erase Cycle Time	—	—	11	ms	
T_{PDFM}	Internally Timed DFM (EEPROM) Programming Operation Time	—	—	11	ms	EEPROM memory and Configuration Words
T_{PINT}	Internally Timed Programming Operation Time	—	—	50	µs	Program Memory and Configuration Words
T_{EXIT}	Time Delay when Exiting Program/ Verify Mode	1	—	—	µs	

Note:

1. Bulk Erased devices default to Brown-out Reset enabled with BORV = `11` (low trip point). V_{DDMIN} is the V_{BOR} threshold (with BORV = `1`) when performing Low-Voltage Programming on a Bulk Erased device to ensure that the device is not held in Brown-out Reset.
2. The hardware requires V_{DD} to be above the BOR threshold, at the ~2.85V nominal setting, in order to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit settings. Refer to the microcontroller device data sheet specifications for min./typ./max. limits of the V_{BOR} level.

5. APPENDIX A: Revision History

Doc Rev.	Date	Comments
A	01/2019	Initial document release.

6. APPENDIX B

This section provides information about the Device ID, Checksums and Pinout Descriptions

Table 6-1. Configuration Word and Mask

Device	Device ID	Config. 1L		Config. 1H		Config. 2L		Config. 2H		Config. 3L		Config. 3H		Config. 4L		Config. 4H		Config. 5L		Config. 5H		
		Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Word (Hex)	Mask (Hex)	Unprotected (Hex)	Protected (Hex)	Mask (Hex)
PIC18F 24Q43	7360h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 25Q43	73C0h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 26Q43	7420h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 27Q43	7480h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 44Q43	7380h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 45Q43	73E0h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 46Q43	7440h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 47Q43	74A0h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 54Q43	73A0h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 55Q43	7400h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 56Q43	7460h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01
PIC18F 57Q43	74C0h	FF	77	FF	29	FF	FF	FF	BF	FF	7F	FF	3F	FF	3F	FF	8F	FF	00	FF	FE	01

Table 6-2. Checksum Values

Device	Checksum			
	Unprotected		Code-Protected	
	Blank	00AAh at First and Last Address	Blank	00AAh at First and Last Address
PIC18F24Q43	C3EBh	C341h	0413h	03FFh
PIC18F25Q43	83EBh	784Ch	040Fh	040Ah
PIC18F26Q43	03EBh	0341h	0407h	03F3h
PIC18F27Q43	03EBh	0341h	0407h	03F3h
PIC18F44Q43	C3EBh	C341h	0413h	03FFh
PIC18F45Q43	83EBh	784Ch	040Fh	040Ah
PIC18F46Q43	03EBh	0341h	0407h	03F3h
PIC18F47Q43	03EBh	0341h	0407h	03F3h
PIC18F54Q43	C3EBh	C341h	0413h	03FFh
PIC18F55Q43	83EBh	784Ch	040Fh	040Ah
PIC18F56Q43	03EBh	0341h	0407h	03F3h
PIC18F57Q43	03EBh	0341h	0407h	03F3h

Table 6-3.

Checksum Computed With Code Protection Disabled: PIC18F24Q43, Blank Device

Sum of Memory Addresses from 0000h to 3FFFh	C000h (4000h * 00FFh)
Configuration Word 1L	FFh
Configuration Word 1L Mask	77h
Configuration Word 1H	FFh
Configuration Word 1H Mask	29h
Configuration Word 2L	FFh
Configuration Word 2L Mask	FFh
Configuration Word 2H	FFh
Configuration Word 2H Mask	BFh
Configuration Word 3L	FFh
Configuration Word 3L Mask	7Fh
Configuration Word 3H	FFh
Configuration Word 3H Mask	3Fh
Configuration Word 4L	FFh
Configuration Word 4L Mask	3Fh
Configuration Word 4H	FFh
Configuration Word 4H Mask	8Fh
Configuration Word 5L	FFh
Configuration Word 5L Mask	00h
Configuration Word 5H	FFh
Configuration Word 5H Mask	01h
Checksum = C000h + (FFh AND 77h) + (FFh AND 29h) + (FFh AND FFh) + (FFh AND BFh) + (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 3Fh) + (FFh AND 8Fh) + (FFh AND 00h) + (FFh AND 01h) = C000h + 77h + 29h + FFh + BFh + 7Fh + 3Fh + 3Fh + 8Fh + 00h + 01h = C3EBh	

Table 6-4.

Checksum Computed With Code Protection Disabled: PIC18F24Q43, 00AAh at First and Last Address

Sum of Memory Addresses from 0000h to 3FFFh	BF56h (AAh + (3FFEh * 00FFh) + AAh)
Configuration Word 1L	FFh
Configuration Word 1L Mask	77h
Configuration Word 1H	FFh
Configuration Word 1H Mask	29h
Configuration Word 2L	FFh
Configuration Word 2L Mask	FFh
Configuration Word 2H	FFh
Configuration Word 2H Mask	BFh
Configuration Word 3L	FFh
Configuration Word 3L Mask	7Fh
Configuration Word 3H	FFh
Configuration Word 3H Mask	3Fh
Configuration Word 4L	FFh
Configuration Word 4L Mask	3Fh
Configuration Word 4H	FFh
Configuration Word 4H Mask	8Fh
Configuration Word 5L	FFh
Configuration Word 5L Mask	00h
Configuration Word 5H	FFh
Configuration Word 5H Mask	01h
Checksum = BF56h + (FFh AND 77h) + (FFh AND 29h) + (FFh AND FFh) + (FFh AND BFh) + (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 3Fh) + (FFh AND 8Fh) + (FFh AND 00h) + (FFh AND 01h) = BF56h + 77h + 29h + FFh + BFh + 7Fh + 3Fh + 3Fh + 8Fh + 00h + 01h = C341h	

Table 6-5.

Checksum Computed With Code Protection Enabled: PIC18F24Q43, Blank Device

Configuration Word 1L	FFh
Configuration Word 1L Mask	77h
Configuration Word 1H	FFh
Configuration Word 1H Mask	29h
Configuration Word 2L	FFh
Configuration Word 2L Mask	FFh
Configuration Word 2H	FFh
Configuration Word 2H Mask	BFh
Configuration Word 3L	FFh
Configuration Word 3L Mask	7Fh
Configuration Word 3H	FFh
Configuration Word 3H Mask	3Fh
Configuration Word 4L	FFh
Configuration Word 4L Mask	3Fh
Configuration Word 4H	FFh
Configuration Word 4H Mask	8Fh
Configuration Word 5L	FFh
Configuration Word 5L Mask	00h
Configuration Word 5H	FFh
Configuration Word 5H Mask	01h
Checksum = (FFh AND 77h) + (FFh AND 29h) + (FFh AND FFh) + (FFh AND BFh) + (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 3Fh) + (FFh AND 8Fh) + (FFh AND 00h) + (FFh AND 01h) + SUM_ID = 77h + 29h + FFh + BFh + 7Fh + 3Fh + 3Fh + 8Fh + 00h + 01h + 28h = 0413h	
SUM_ID = Bytewise sum of lower four bits of all User ID Locations SUM_ID = 000Ch + 0003h + 000Eh + 000Bh + 0000h + 0000h + 0000h + 0000h = 0028h	

Table 6-6.

Checksum Computed With Code Protection Enabled: PIC18F24Q43, 00AAh at First and Last Address

Configuration Word 1L	FFh
Configuration Word 1L Mask	77h
Configuration Word 1H	FFh
Configuration Word 1H Mask	29h
Configuration Word 2L	FFh
Configuration Word 2L Mask	FFh
Configuration Word 2H	FFh
Configuration Word 2H Mask	BFh
Configuration Word 3L	FFh
Configuration Word 3L Mask	7Fh
Configuration Word 3H	FFh
Configuration Word 3H Mask	3Fh
Configuration Word 4L	FFh
Configuration Word 4L Mask	3Fh
Configuration Word 4H	FFh
Configuration Word 4H Mask	8Fh
Configuration Word 5L	FFh
Configuration Word 5L Mask	00h
Configuration Word 5H	FFh
Configuration Word 5H Mask	01h
Checksum = (FFh AND 77h) + (FFh AND 29h) + (FFh AND FFh) + (FFh AND BFh) + (FFh AND 7Fh) + (FFh AND 3Fh) + (FFh AND 3Fh) + (FFh AND 8Fh) + (FFh AND 00h) + (FFh AND 01h) + SUM_ID = 77h + 29h + FFh + BFh + 7Fh + 3Fh + 3Fh + 8Fh + 00h + 01h + 14h = 03FFh	
SUM_ID = Bytewise sum of lower four bits of all User ID Locations SUM_ID = 000Ch + 0003h + 0004h + 0001h + 0000h + 0000h + 0000h + 0000h = 0014h	

Table 6-7. Programming Pin Locations By Package Type

Device	Package	Package Code	V_{DD}	V_{SS}	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
			PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC18F 24Q43 PIC18F 25Q43 PIC18F 26Q43 PIC18F 27Q43	28-Pin SPDIP	(SP)	20	19, 8	1	RE3	27	RB6	28	RB7
	28-Pin SOIC	(SO)	20	19, 8	1	RE3	27	RB6	28	RB7
	28-Pin SSOP	(SS)	20	19, 8	1	RE3	27	RB6	28	RB7
	28-Pin VQFN	(STX)	17	16, 5	26	RE3	24	RB6	25	RB7
PIC18F 44Q43 PIC18F 45Q43 PIC18F 46Q43 PIC18F 47Q43	40-Pin PDIP	(P)	32, 11	31, 12	1	RE3	39	RB6	40	RB7
	40-Pin VQFN	(NHX)	26, 7	27, 6	16	RE3	14	RB6	15	RB7
	44-Pin TQFP	(PT)	28, 7	29, 6	18	RE3	16	RB6	17	RB7
PIC18F 54Q43 PIC18F 55Q43 PIC18F 56Q43 PIC18F 57Q43	48-Pin TQFP	(PT)	30, 7	31 , 6	20	RE3	18	RB6	19	RB7
	48-Pin VQFN	(6LX)	30, 7	31, 6	20	RE3	18	RB6	19	RB7

Note:
The most current package drawings are located in the Microchip Packaging Specification, DS00000049 (http://www.microchip.com/packaging). The drawing numbers listed above do not include the current revision designator, which is added at the end of the number.

6.1 Register Summary - Configuration Words

Offset	Name	Bit Pos.								
300000	CONFIG1L	7:0		RSTOSC[2:0]				FEXTOSC[2:0]		
300001	CONFIG1H	7:0			FCMEN		CSWEN		PR1WAY	CLKOUTEN
300002	CONFIG2L	7:0	BOREN[1:0]		LPBOREN	IVT1WAY	MVECEN	PWRTS[1:0]		MCLRE
300003	CONFIG2H	7:0	XINST		LVP	STVREN	PPS1WAY	ZCD	BORV[1:0]	
300004	CONFIG3L	7:0		WDTE[1:0]		WDTCPS[4:0]				
300005	CONFIG3H	7:0			WDTCCS[2:0]			WDTCWS[2:0]		
300006	CONFIG4L	7:0			DEBUG	SAFEN	BBEN	BBSIZE[2:0]		
300007	CONFIG4H	7:0	WRTAPP				WRTSAF	WRTD	WRTC	WRTB
300008	CONFIG5L	7:0								
300009	CONFIG5H	7:0								CP

6.1.1 CONFIG1L

Name: CONFIG1L
Offset: 30 0000h

Configuration Word 1L

Bit	7	6	5	4	3	2	1	0
		RSTOSC[2:0]				FEXTOSC[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	1	1		1	1	1

Bits 6:4 – RSTOSC[2:0] Power-up Default Value for COSC bits
This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

Value	Description
111	EXTOSC operating per FEXTOSC bits
110	HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1. Resets COSC/NOSC to b'110'.
101	LFINTOSC
100	SOSC
011	Reserved
010	EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
001	Reserved
000	HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1. Resets COSC/NOSC to b'110'.

Bits 2:0 – FEXTOSC[2:0] FEXTOSC External Oscillator Mode Selection bits

Value	Description
111	ECH (external clock) above 8 MHz
110	ECM (external clock) for 500 kHz to 8 MHz
101	ECL (external clock) below 500 kHz
100	Oscillator not enabled
011	Reserved (do not use)
010	HS (crystal oscillator) above 4 MHz
001	XT (crystal oscillator) above 500 kHz, below 4 MHz
000	LP (crystal oscillator) optimized for 32.768 kHz

6.1.2 CONFIG1H

Name: CONFIG1H
Offset: 30 0001h

Configuration Word 1H

Bit	7	6	5	4	3	2	1	0
			FCMEN		CSWEN		PR1WAY	$\overline{\text{CLKOUTEN}}$
Access			R/W		R/W		R/W	R/W
Reset			1		1		1	1

Bit 5 – FCMEN Fail-Safe Clock Monitor Enable bit

Value	Description
1	Fail-Safe Clock Monitor enabled
0	Fail-Safe Clock Monitor disabled

Bit 3 – CSWEN Clock Switch Enable bit

Value	Description
1	Writing to NOSC and NDIV is allowed
0	The NOSC and NDIV bits cannot be changed by user software

Bit 1 – PR1WAY PRLOCKED One-Way Set Enable bit

Value	Description
1	PRLOCKED bit can be cleared and set only once; Priority registers remain locked after one clear/set cycle
0	PRLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 0 – $\overline{\text{CLKOUTEN}}$ Clock Out Enable bit
If FEXTOSC = HS, XT, LP, then this bit is ignored.
Otherwise:

Value	Description
1	CLKOUT function is disabled; I/O function on OSC2
0	CLKOUT function is enabled; $F_{OSC}/4$ clock appears at OSC2

6.1.3 CONFIG2L

Name: CONFIG2L
Offset: 30 0002h

Configuration Word 2L

Bit	7	6	5	4	3	2	1	0
	BOREN[1:0]		$\overline{\text{LPBOREN}}$	IVT1WAY	MVECEN	PWRTS[1:0]		MCLRE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	1	1	1

Bits 7:6 – BOREN[1:0] Brown-out Reset Enable bits
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by BORV bit

Value	Description
11	Brown-out Reset enabled, SBOREN bit is ignored
10	Brown-out Reset enabled while running, disabled in Sleep; SBOREN is ignored
01	Brown-out Reset enabled according to SBOREN
00	Brown-out Reset disabled

Bit 5 – $\overline{\text{LPBOREN}}$ Low-Power BOR Enable bit

Value	Description
1	Low-Power Brown-out Reset is disabled
0	Low-Power Brown-out Reset is enabled

Bit 4 – IVT1WAY IVTLOCK One-Way Set Enable bit

Value	Description
1	IVTLOCK bit can be cleared and set only once; IVT registers remain locked after one clear/set cycle
0	IVTLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 3 – MVECEN Multivector Enable bit

Value	Description
1	Multivector is enabled; vector table used for interrupts
0	Legacy interrupt behavior

Bits 2:1 – PWRTS[1:0] Power-up Timer Selection bits

Value	Description
11	PWRT is disabled
10	PWRT is set at 64 ms
01	PWRT is set at 16 ms
00	PWRT is set at 1 ms

Bit 0 – MCLRE Master Clear ($\overline{\text{MCLR}}$) Enable bit

Value	Condition	Description
x	If LVP = 1	RE3 pin function is $\overline{\text{MCLR}}$
1	If LVP = 0	$\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0	If LVP = 0	$\overline{\text{MCLR}}$ pin function is port defined function

6.1.4 CONFIG2H

Name: CONFIG2H
Offset: 30 0003h

Configuration Word 2H

Bit	7	6	5	4	3	2	1	0
	$\overline{XINST}$		LVP	STVREN	PPS1WAY	$\overline{ZCD}$	BORV[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	1		1	1	1	1	1	1

Bit 7 – $\overline{XINST}$ Extended Instruction Set Enable bit

Value	Description
1	Extended Instruction Set and Indexed Addressing mode disabled (Legacy mode)
0	Extended Instruction Set and Indexed Addressing mode enabled

Bit 5 – LVP Low-Voltage Programming Enable bit
The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state.

Value	Description
1	Low-voltage programming enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
0	HV on $\overline{MCLR}/V_{PP}$ must be used for programming

Bit 4 – STVREN Stack Overflow/Underflow Reset Enable bit

Value	Description
1	Stack Overflow or Underflow will cause a Reset
0	Stack Overflow or Underflow will not cause a Reset

Bit 3 – PPS1WAY PPSLOCKED One-Way Set Enable bit

Value	Description
1	The PPSLOCKED bit can only be set once after an unlocking sequence is executed; once PPSLOCK is set, all future changes to PPS registers are prevented
0	The PPSLOCKED bit can be set and cleared as needed (provided an unlocking sequence is executed)

Bit 2 – $\overline{ZCD}$ ZCD Disable bit

Value	Description
1	ZCD disabled. ZCD can be enabled by setting the ZCDSEN bit of ZCDCON
0	ZCD always enabled, PMDx[ZCDMD] bit is ignored

Bits 1:0 – BORV[1:0] Brown-out Reset Voltage Selection bits

Value	Description
1x	Brown-out Reset Voltage (V_{BOR}) set to 2.55 V
01	Brown-out Reset Voltage (V_{BOR}) set to 2.7 V
00	Brown-out Reset Voltage (V_{BOR}) set to 2.85 V

Note: BORV - The higher voltage setting is recommended for operation at or above 16 MHz.

6.1.5 CONFIG3L

Name: CONFIG3L
Offset: 30 0004h

Configuration Word 3L

Bit	7	6	5	4	3	2	1	0
		WDTE[1:0]		WDTCPS[4:0]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	1	1	1	1	1

Bits 6:5 – WDTE[1:0] WDT Operating Mode bits

Value	Description
11	WDT enabled regardless of Sleep; SEN bit in WDTCON0 is ignored
10	WDT enabled while Sleep = 0, suspended when Sleep = 1; SEN bit in WDTCON0 is ignored
01	WDT enabled/disabled by SEN bit in WDTCON0
00	WDT disabled, SEN bit in WDTCON0 is ignored

Bits 4:0 – WDTCPS[4:0] WDT Period Select bits

WDTCPS	WDTCON0[WDTPS] at POR				Software Control of WDTPS?
	Value	Divider Ratio		Typical Time Out (F_{IN} = 31 kHz)	
11111	01011	1:65536	2^{16}	2s	Yes
11110 ... 10011	11110 ... 10011	1:32	2^5	1 ms	No

.....continued

WDTCPS	WDTCON0[WDTPS] at POR				Software Control of WDTPS?
	Value	Divider Ratio		Typical Time Out (F_{IN} = 31 kHz)	
10010	10010	1:8388608	2^{23}	256s	No
10001	10001	1:4194304	2^{22}	128s	
10000	10000	1:2097152	2^{21}	64s	
01111	01111	1:1048576	2^{20}	32s	
01110	01110	1:524288	2^{19}	16s	
01101	01101	1:262144	2^{18}	8s	
01100	01100	1:131072	2^{17}	4s	
01011	01011	1:65536	2^{16}	2s	
01010	01010	1:32768	2^{15}	1s	
01001	01001	1:16384	2^{14}	512 ms	
01000	01000	1:8192	2^{13}	256 ms	
00111	00111	1:4096	2^{12}	128 ms	
00110	00110	1:2048	2^{11}	64 ms	
00101	00101	1:1024	2^{10}	32 ms	
00100	00100	1:512	2^{9}	16 ms	
00011	00011	1:256	2^{8}	8 ms	
00010	00010	1:128	2^{7}	4 ms	
00001	00001	1:64	2^{6}	2 ms	
00000	00000	1:32	2^{5}	1 ms	

6.1.6 CONFIG3H

Name: CONFIG3H
Offset: 30 0005h

Configuration Word 3H

Bit	7	6	5	4	3	2	1	0
			WDTCCS[2:0]			WDTCWS[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 5:3 – WDTCCS[2:0] WDT Input Clock Selector bits

Value	Condition	Description
x	WDTE = 00	These bits have no effect
111	WDTE ≠ 00	Software Control
110 to 011	WDTE ≠ 00	Reserved
010	WDTE ≠ 00	WDT reference clock is the SOSC
001	WDTE ≠ 00	WDT reference clock is the 31.25 kHz MFINTOSC
000	WDTE ≠ 00	WDT reference clock is the 31.0 kHz LFINTOSC

Bits 2:0 – WDTCWS[2:0] WDT Window Select bits

WDTCWS	WDTCON1[WINDOW] at POR			Software control of WINDOW	Keyed access required?
	Value	Window delay Percent of time	Window opening Percent of time		
111	111	n/a	100	Yes	No
110	110	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

6.1.7 CONFIG4L

Name: CONFIG4L
Offset: 30 0006h

Configuration Word 4L

Bit	7	6	5	4	3	2	1	0
			$\overline{\text{DEBUG}}$	$\overline{\text{SAFEN}}$	$\overline{\text{BBEN}}$	BBSIZE[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit 5 – $\overline{\text{DEBUG}}$ Debugger Enable bit

Value	Description
1	Background debugger disabled
0	Background debugger enabled

Bit 4 – $\overline{\text{SAFEN}}$ Storage Area Flash (SAF) Enable bit(1)

Value	Description
1	SAF is disabled
0	SAF is enabled

Bit 3 – $\overline{\text{BBEN}}$ Boot Block Enable bit(1)

Value	Description
1	Boot Block is disabled
0	Boot Block is enabled

Bits 2:0 – BBSIZE[2:0] Boot Block Size Selection bits(2)

Table 6-8. Boot Block Size

$\overline{\text{BBEN}}$	BBSIZE	Boot Block Size (words)	End Address of Boot Block	Device Size		
				16k	32k	64k
1	xxx	0	–	X	X	X
0	111	512	00 03FFh	X	X	X
0	110	1024	00 07FFh	X	X	X
0	101	2048	00 0FFFh	X	X	X
0	100	4096	00 1FFFh	X	X	X
0	011	8192	00 3FFFh	X	X	X
0	010	16384	00 7FFFh	– (3)	X	X
0	001	32768	00 FFFFh	– (3)		X
0	000	Reserved	00 FFFFh	– (3)		

Note:

1. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
2. BBSIZE[2:0] bits can only be changed when BBEN = 1. Once BBEN = 0, BBSIZE[2:0] can only be changed through a Bulk Erase.
3. The maximum Boot Block size is half the user program memory size. All selections higher than the maximum size default to the maximum Boot Block size of half PFM. For example, all settings of BBSIZE[2:0] = 000 through BBSIZE[2:0] = 010, default to a Boot Block size of 16 kW on a 32 kW device.

6.1.8 CONFIG4H

Name: CONFIG4H
Offset: 30 0007h

Configuration Word 4H

Note:

1. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
2. Applicable only if $\overline{\text{SAFEN}}$ = 0.
3. Applicable only if $\overline{\text{BBEN}}$ = 0.

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{WRTAPP}}$				$\overline{\text{WRTSAF}}$	$\overline{\text{WRTD}}$	$\overline{\text{WRTC}}$	$\overline{\text{WRTB}}$
Access	R/W				R/W	R/W	R/W	R/W
Reset	1				1	1	1	1

Bit 7 – $\overline{\text{WRTAPP}}$ Application Block Write Protection bit(1)

Value	Description
1	Application Block is NOT write-protected
0	Application Block is write-protected

Bit 3 – $\overline{\text{WRTSAF}}$ Storage Area Flash (SAF) Write Protection bit(1) (2)

Value	Description
1	SAF is NOT write-protected
0	SAF is write-protected

Bit 2 – $\overline{\text{WRTD}}$ Data EEPROM Write Protection bit(1)

Value	Description
1	Data EEPROM is NOT write-protected
0	Data EEPROM is write-protected

Bit 1 – $\overline{\text{WRTC}}$ Configuration Register Write Protection bit(1)

Value	Description
1	Configuration Registers are NOT write-protected
0	Configuration Registers are write-protected

Bit 0 – $\overline{\text{WRTB}}$ Boot Block Write Protection bit(1) (3)

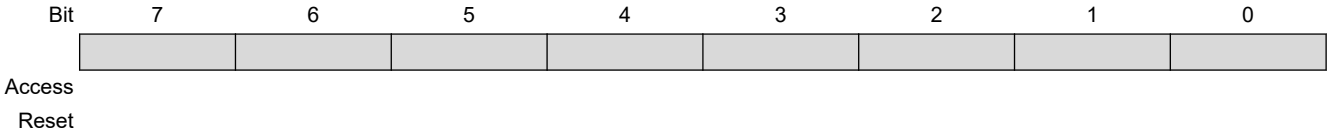
Value	Description
1	Boot Block is NOT write-protected
0	Boot Block is write-protected

6.1.9 CONFIG5L

Name: CONFIG5L
Offset: 30 0008h

Configuration Word 5L

This register is reserved



6.1.10 CONFIG5H

Name: CONFIG5H
Offset: 30 0009h

Configuration Word 5H

Bit	7	6	5	4	3	2	1	0
								$\overline{CP}$
Access								R/W
Reset								1

Bit 0 – $\overline{CP}$ User Program Flash Memory and Data EEPROM Code Protection bit(1)

Value	Description
1	User Program Flash Memory and Data EEPROM code protection are disabled
0	User Program Flash Memory and Data EEPROM code protection are enabled

The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at http://www.microchip.com/. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Trademarks

ISBN: 978-1-5224-4067-3

Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4450-2828 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-67-3636 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

PIC18F27Q43-I/SS PIC18F27Q43-I/STX PIC18F47Q43T-I/MP PIC18F47Q43T-I/PT PIC18F57Q43-E/PT PIC18F57Q43-I/PT PIC18F57Q43T-I/PT PIC18F27Q43-I/SP PIC18F47Q43-E/P PIC18F47Q43-E/PT PIC18F47Q43-I/MP PIC18F47Q43-I/P PIC18F47Q43-I/PT PIC18F27Q43-E/SO PIC18F27Q43-E/SP PIC18F27Q43-E/SS PIC18F27Q43-E/STX PIC18F27Q43-I/SO PIC18F27Q43T-I/SO PIC18F27Q43T-I/SS PIC18F27Q43T-I/STX PIC18F47Q43-E/MP