ATA663331/ATA663354

LIN SBC(1) including LIN Transceiver, Voltage Regulator, Dual Low-side Driver and a High-side Switch

DATASHEET

Features

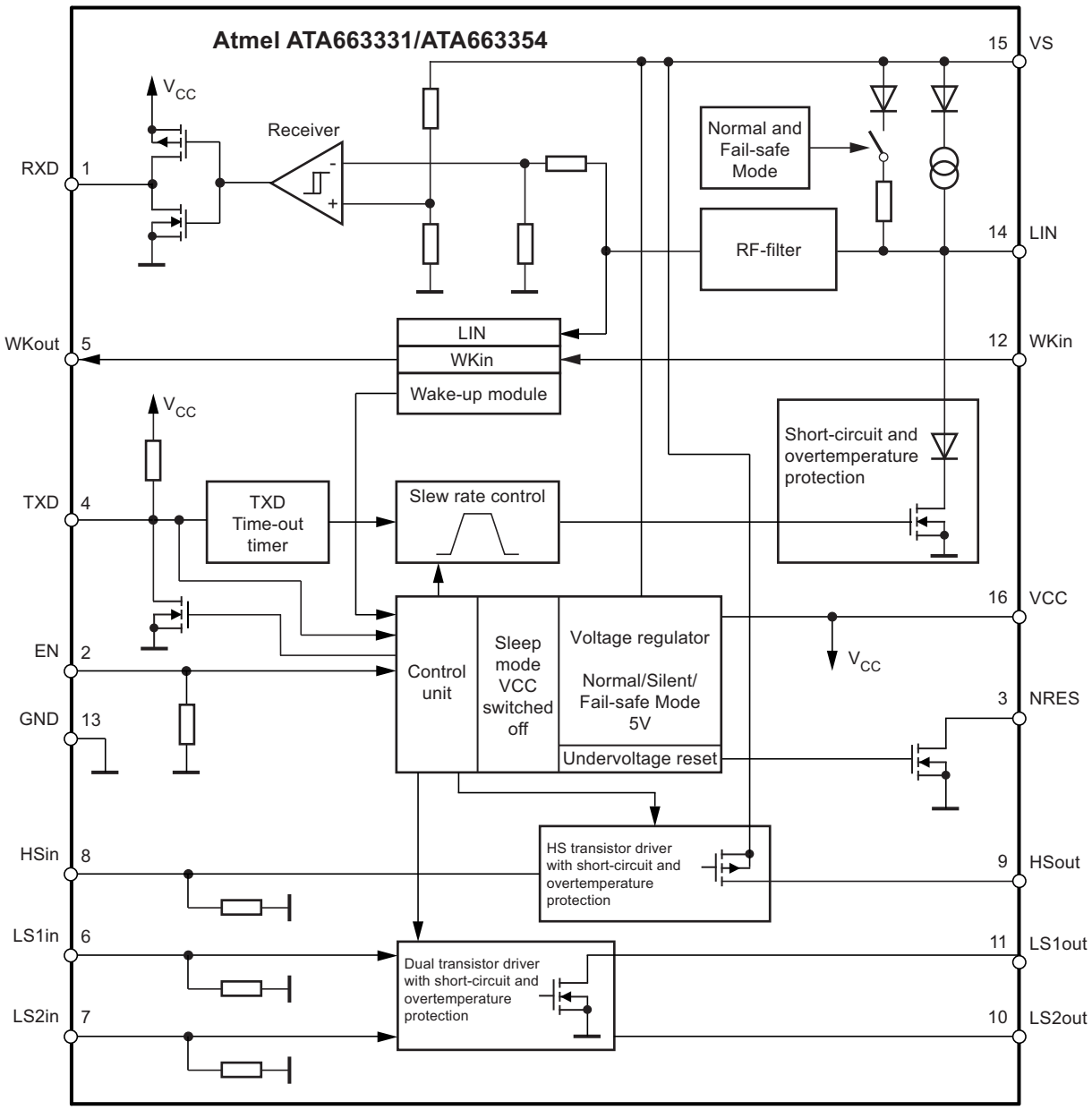
- Supply voltage up to 40V
- Operating voltage V_{VS} = 5V to 28V
- Supply current
  - Sleep mode: typically 10µA
  - Silent mode: typically 47µA
  - Very low current consumption at low supply voltages (2V < V_{VS} < 5.5V): typically 130µA
- Linear low-drop voltage regulator, 85mA current capability:
  - MLC (multi-layer ceramic) capacitor with 0Ω ESR
  - Normal, fail-safe, and silent mode
    - Atmel ATA663354: V_{VCC} = 5.0V ±2%
    - Atmel ATA663331: V_{VCC} = 3.3V ±2%
  - Sleep mode: VCC is switched off
- VCC undervoltage detection with open drain reset output (NRES, 4ms reset time)
- Voltage regulator is short-circuit and over-temperature protected
- LIN physical layer according to LIN 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2
- Bus pin is over-temperature and short-circuit protected versus GND and battery
- Two low-side protected switches and one high-side protected switch
- Wake-up capability via LIN bus (100µs dominant) and WKin pin
- Wake-up source recognition
- TXD time-out timer
- Advanced EMC and ESD performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.3”
- Interference and damage protection according to ISO7637
- Qualified according to AEC-Q100
- Package: DFN16 with wettable flanks (Moisture Sensitivity Level 1)

Note: 1. LIN SBC: LIN system basis chip

1. Description

Designed in compliance with LIN specifications 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, the Atmel® ATA6633xx is a new generation of system basis chips with a fully integrated LIN transceiver, a low-drop voltage regulator (3.3V/5V/85mA), two low-side drivers, and one high-side driver. This combination makes it possible to develop simple, but powerful, slave nodes in LIN bus systems. Atmel ATA6633xx is designed to handle low-speed data communication in vehicles (such as in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20kBaud. The bus output is designed to withstand high voltage. Sleep mode and silent mode guarantee minimized current consumption even in the case of a floating or short-circuited LIN bus.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning DFN16

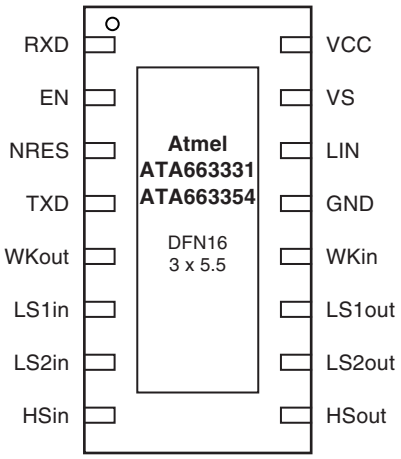


Table 2-1. Pin Description

Pin	Symbol	Function
1	RXD	Receive data output
2	EN	Enables normal mode if the input is high
3	NRES	VCC undervoltage output, open drain, low at reset
4	TXD	Transmit data input
5	WKout	Low-voltage output to indicate local wake-up request
6	LS1in	Low-side 1 control input
7	LS2in	Low-side 2 control input
8	HSin	High-side control input
9	HSout	High-side output
10	LS2out	Low-side 2 output
11	LS1out	Low-side 1 output
12	WKin	High-voltage input for local wake-up request
13	GND	Ground
14	LIN	LIN bus line input/output
15	VS	Supply voltage
16	VCC	Output voltage regulator 3.3V/5V/85mA
Backside		Heat slug, power-ground connection

3. Pin Description

3.1 Supply Pin (VS)

LIN operating voltage is V_{VS} = 5V to 28V. In order to avoid false bus messages, undervoltage detection is implemented to disable transmission if V_{VS} falls below typ. 4.5V. After switching on V_{VS}, the IC starts in fail-safe mode and the voltage regulator is switched on.

The supply current in sleep mode is typically 10µA and 47µA in silent mode.

3.2 Ground Pin (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It can handle ground shifts of up to 11.5% with respect to V_{VS}.

3.3 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85mA, supplying the microcontroller and other ICs on the PCB, and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes a reset signal at the NRES output pin if it drops below a defined threshold $V_{VCC\_th\_uv\_down}$.

3.4 Undervoltage Reset Output Pin (NRES)

If the V_{VCC} voltage falls below the undervoltage detection threshold $V_{VCC\_th\_uv\_down}$, NRES switches to low after t_{res_f}. Even if V_{VCC} = 0V the NRES stays low because it is internally driven from the VS voltage. If VS voltage ramps down, NRES stays low until V_{VS} < 1.5V and then becomes high-impedant.

The undervoltage delay implemented keeps NRES low for t_{Reset} = 4ms after V_{VCC} reaches its nominal value.

3.5 Bus Pin (LIN)

A low-side driver is implemented with internal current limitation and thermal shutdown as well as an internal pull-up resistor in compliance with LIN specification 2.x. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to VS, even in the event of a GND shift or supply disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification.

The fall time (transition from recessive to dominant state) and the rise time (transition from dominant to recessive state) are slope-controlled.

During a short-circuit at the LIN pin to VBAT, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. The VCC regulator works independently during LIN overtemperature switch-off.

During a short circuit from LIN to GND the IC can be switched into sleep or silent mode and even in this case the current consumption is lower than 100µA in sleep mode and lower than 120µA in silent mode. If the short circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2µA at pin LIN during loss of V_{VS}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

3.6 Bus Data Input/Output (TXD)

In normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state. If the TXD pin stays at GND level while switching into normal mode, it must be pulled to high level longer than 10µs before the LIN driver can be activated. This feature prevents the bus line from being unintentionally driven to dominant state after normal mode has been activated (also if a short circuit occurs at TXD to GND). If TXD is short-circuited to GND, it is possible to switch to sleep mode via the EN- pin after $t > t_{dom}$.

In fail-safe mode this pin is used as an output and signals the fail-safe source.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{dom} > 20ms, the LIN bus driver is switched to the recessive state. Nevertheless, when switching to sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, switch TXD to high (> 10µs).

3.7 Bus Data Output Pin (RXD)

In normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured with an external load capacitor of 20pF.

In silent mode the RXD output switches to high.

3.8 Enable Input Pin (EN)

The enable input pin controls the operation mode of the device. If EN is high, the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/85mA output capability.

If EN is switched to low while TXD is still high, the device is forced into silent mode. No data transmission is then possible and the current consumption is reduced to $I_{VSsilent}$ typ. 47µA. The VCC regulator maintains full functionality.

If EN is switched to low while TXD is low, the device is forced into sleep mode. No data transmission is possible and the voltage regulator is switched off.

Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.

3.9 Wake Input Pin (WKin)

The WKin pin is a high-voltage input used to wake up the device from sleep mode or silent mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10µA is implemented. The voltage threshold for a wake-up signal is typically 2V below the VS voltage. If a local wake up is not needed in the application, the WKin pin can be connected directly to the VS pin.

3.10 Wake Output Pin (WKout)

The WKout pin is a low-voltage output used for waking up a microcontroller or other device. It is a push-pull output stage switching between VCC and GND. It is directly controlled by the WKin pin. If $V_{WKin} \geq V_{WKinH}$, WKout is low and no wake-up is detected. If $V_{WKin} < V_{WKinL}$, WKout is high and the device is switched into fail-safe mode if it was previously in a low-power mode such as sleep or silent mode. Please note that during silent, fail-safe and normal mode, the output pin WKout is always showing the state of pin WKin.

If a local wake up is not needed in the application, the WKout pin can be left open.

3.11 Low-side Driver Pins (LS1out, LS2out, LS1in, LS2in)

LS1out and LS2out are the low-side driver outputs. They are only functional in normal mode (see also the “Operating Modes” section). These outputs are both short-circuit protected by means of output voltage monitoring and protected against overheating. They additionally include an active clamping circuitry to provide a freewheeling path needed for inductive loads. The clamping voltage $V_{LSclamp}$ is typically > 44V. Please note that an upper energy limit is defined both for single and for repetitive clamping events. This must be considered when choosing the load, because overheating caused by excessive clamping energy is not covered by the output protection and may therefore cause damage to the device.

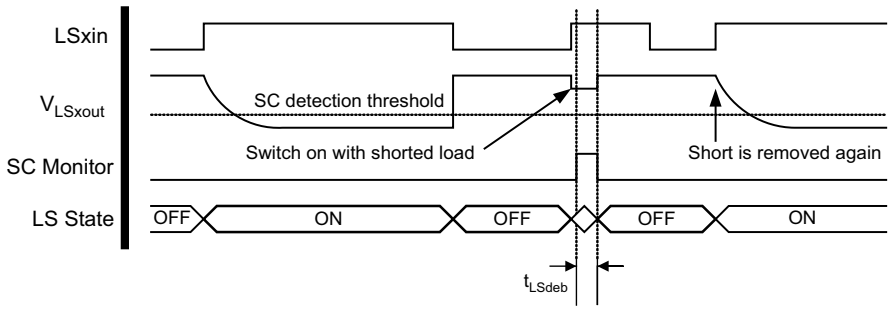
If the LS1in pin or the LS2in pin stay at GND level while switching into normal mode, it must be pulled to high level longer than 10µs before the low-side driver can be activated. This feature prevents the low-side drivers (LS1out pin or LS2out pin respectively) from being unintentionally switched ON after normal mode has been activated. To reactivate the low-side drivers, switch LS1in or LS2in to high (> 10µs).

A disconnection of VS where the low sides are still supplied by VBAT through a load does not have any impact on the clamping feature. That is, voltages above the minimum clamping voltage level $V_{LSclamp}$ activate the energy freewheeling path within the low-side transistor.

The low-side switches are controlled via the low voltage input pins LS1in and LS2in. If the inputs are at high and the IC is in normal mode (i. e., EN is high and there is no undervoltage supply condition), the outputs are switched ON. For fail-safe reasons, both inputs are equipped with a pull-down resistor to GND. This will keep the low-side switches off in case of a missing connection from the controller.

If an overload condition is detected, the appropriate driver stage is shut down. The protective shutdown of the low-side outputs is latched. That is, the corresponding control line LSxin has to go to low first before the output can be restarted again. Because the short-circuit detection is done by means of drain-to-source voltage monitoring, the switch-on event of the transistor is blanked out from the monitoring, so that a capacitor connected to the low-side output does not trigger the protection circuit upon activation of the transistor. Please see also following diagram for illustration:

Figure 3-1. Short-Circuit Detection Timing



As can be seen in Figure 3-1, the output transistor is not switched on again until the control pin “LSxin” is switched off and on again by the microcontroller. As explained above, the short-circuit monitor is only enabled after the transistor reaches full conductivity. That is why the SC monitor line does not show any signal on the first and the last switching-on event in the figure above. Without a short present at the output, the transistor takes much more time to establish its operation point than if there is a short present.

3.12 High-side Driver Pins (HSout, HSin)

This high-side switch is designed for low-power loads such as LEDs, sensors or a voltage divider for measuring the supply voltage. It is functional in all operation modes of the chip but sleep mode. Its structure is connected to the VS supply pin. This pin is protected against short-circuits and also overheating.

The high-side switch is controlled via the low-voltage input pin HSin. If the input is at high, the output is switched on. For fail-safe reasons, the HSin input is equipped with a pull-down resistor to GND. This keeps the high-side switch off in case of a missing connection from the controller.

Please note that in case of a disconnected system ground, the module can be supplied via the connected load on the high-side output and an internal ESD structure. This is the case if the load has a different ground connection than the PCB. See also the “Absolute Maximum Ratings” section for current limits in such cases.

As is the case with low-side switches, the protective shutdown of the high-side output is debounced and latched. In other words, after a protective shutdown of the driver stage, the control line HSin has to go to low first before the output can be restarted.

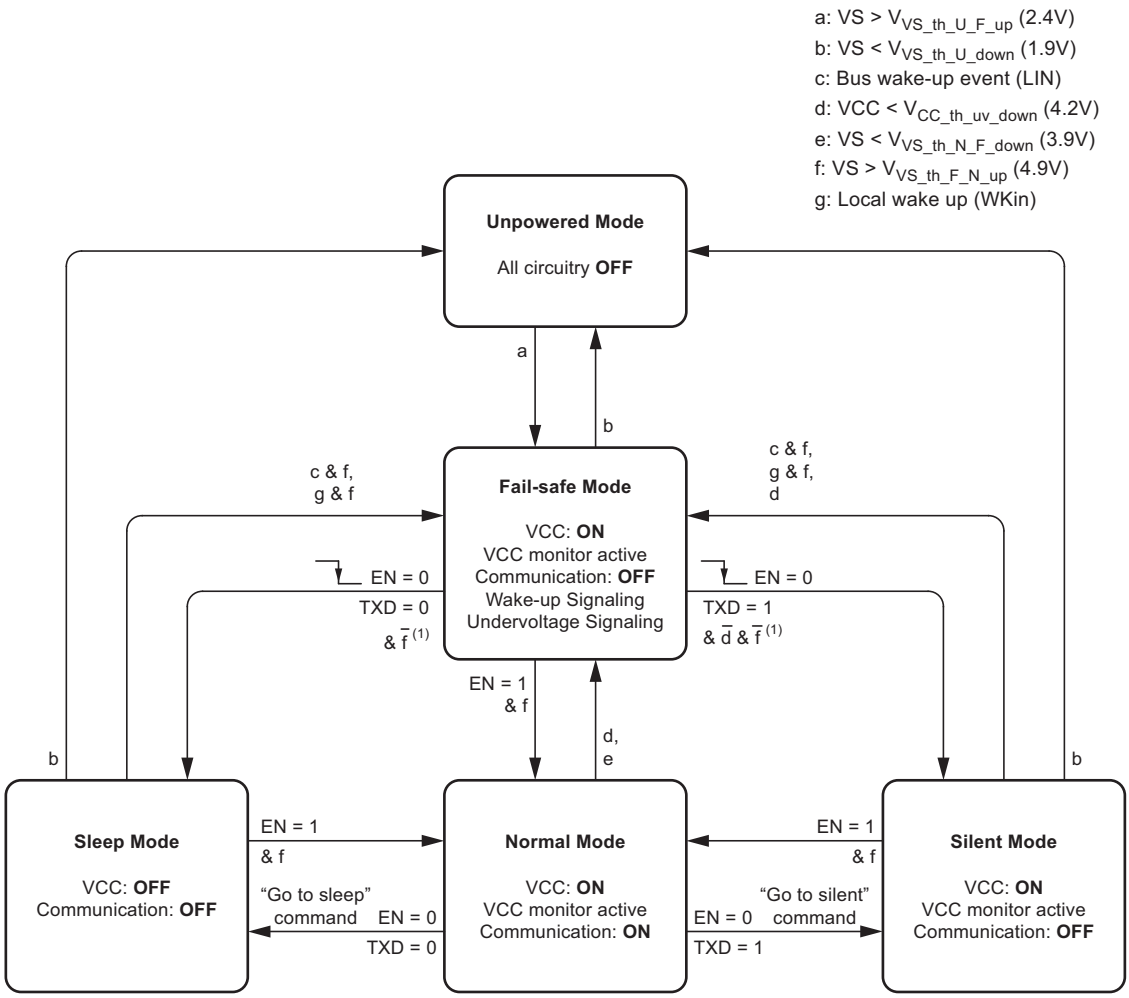
4. Functional Description

4.1 Physical Layer Compatibility

Because the LIN physical layer is independent of higher LIN layers (such as the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes found in older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

4.2 Operating Modes

Figure 4-1. Operating Modes



Note: 1. Condition $\bar{f}$ is valid for VS ramp up; at VS ramp down condition e is valid instead of $\bar{f}$.

Table 4-1. Operating Modes

Operating Modes	Transceiver	Voltage Regulator	Low-side Outputs	High-side Output	LIN	TXD	RXD
Fail-safe	OFF	ON	OFF	HSin-dependent	Recessive	Signaling fail-safe sources (see Table 4-2)	
Normal	ON	ON	LSin-dependent	HSin-dependent	TXD-dependent	Follows data transmission	
Silent	OFF	ON	OFF	HSin-dependent	Recessive	High	High
Sleep/Unpowered	OFF	OFF	OFF	OFF	Recessive	Low	Low

4.2.1 Normal Mode

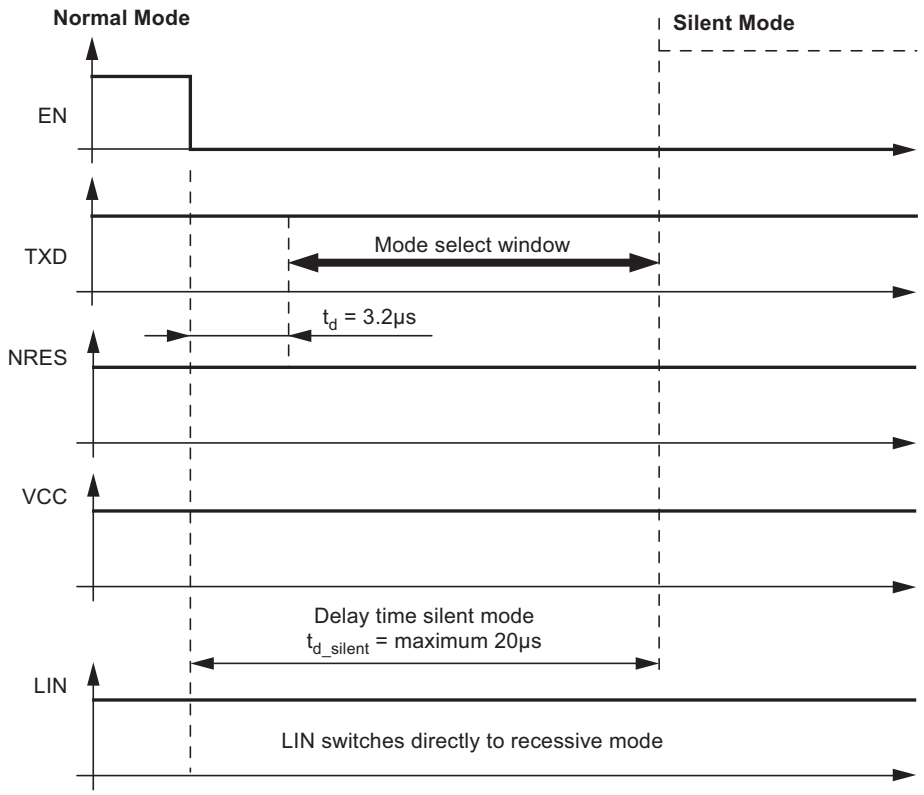
This is the normal transmitting and receiving mode of the LIN interface. Furthermore, the low-side drivers can only be operated in this mode. The VCC voltage regulator works with 3.3V/5V output voltage.

If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to fail-safe mode.

4.2.2 Silent Mode

A falling edge at EN while TXD is high switches the IC into silent mode. The TXD signal has to be logic high during the mode select window. The transmission path is disabled in silent mode. The voltage regulator is active. The overall supply current from VBAT is a combination of the $I_{VSsilent}$ of typ. 47µA plus the VCC regulator output current I_{VCC}.

Figure 4-2. Switching to Silent Mode



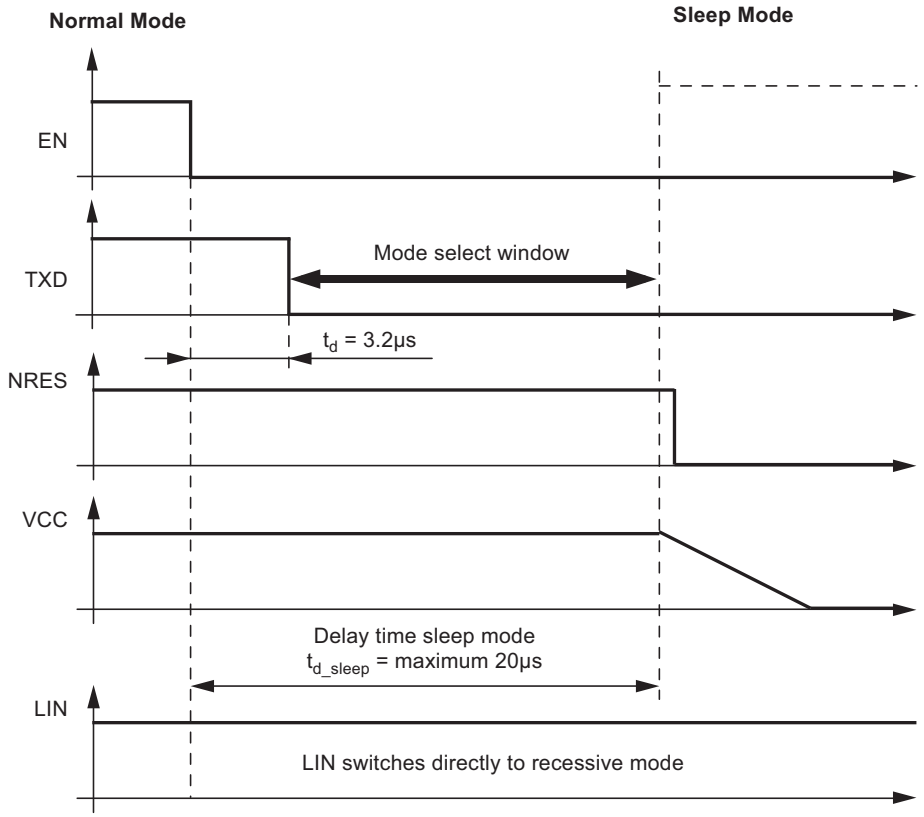
In silent mode the internal slave termination between the LIN pin and VS pin is disabled to minimize the current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10µA) is present between the LIN pin and the VS pin. The silent mode can be activated regardless of the current level on the LIN pin or WKin pin.

If an undervoltage condition occurs, NRES is switched to low and the Atmel® ATA6633xx changes its state to fail-safe mode.

4.2.3 Sleep Mode

A falling edge at EN while TXD is low switches the IC into sleep mode. The TXD signal has to be logic low during the mode select window.

Figure 4-3. Switching to Sleep Mode



In order to avoid any influence on the LIN pin while switching to sleep mode, it is possible to switch the EN to low up to 3.2µs earlier than the TXD. The best and easiest way is to generate two simultaneous falling edges at TXD and EN.

In sleep mode the transmission path is disabled. Supply current from V_{Bat} is typically $I_{VSsleep}$ = 10µA. The VCC regulator is switched off; NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled to minimize the current consumption in case pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10µA) between pin LIN and pin VS is present. The sleep mode can be activated independently from the current level on pin LIN. A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

If TXD is short-circuited to GND, it is possible to switch to sleep mode via EN after $t > t_{dom}$.

4.2.4 Fail-safe Mode

The device automatically switches to fail-safe mode at system power-up. The voltage regulator is switched on. The NRES output remains low for t_{res} = 4ms and resets the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high. The IC then changes to normal mode. A low at NRES switches the IC directly into fail-safe mode. During fail-safe mode the TXD pin is an output and signals together with the RXD output pin the fail-safe source.

If the device enters fail-safe mode coming from the normal mode (EN=1) due to a V_{VS} undervoltage condition ($V_{VS} < V_{VS\_th\_N\_F\_down}$), it is possible to switch into sleep mode or silent mode through a falling edge at the EN input. The current consumption can be reduced further with this feature.

A wake-up event from either silent mode or sleep mode is signaled to the microcontroller using the two pins RXD and TXD. A V_{VS} undervoltage condition is also signaled at these two pins. The coding is shown in Table 4-2.

A wake-up event switches the IC to fail-safe mode.

Table 4-2. Signaling in Fail-safe Mode

Fail-safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
$V_{VS\_th\_N\_F\_down}$ (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

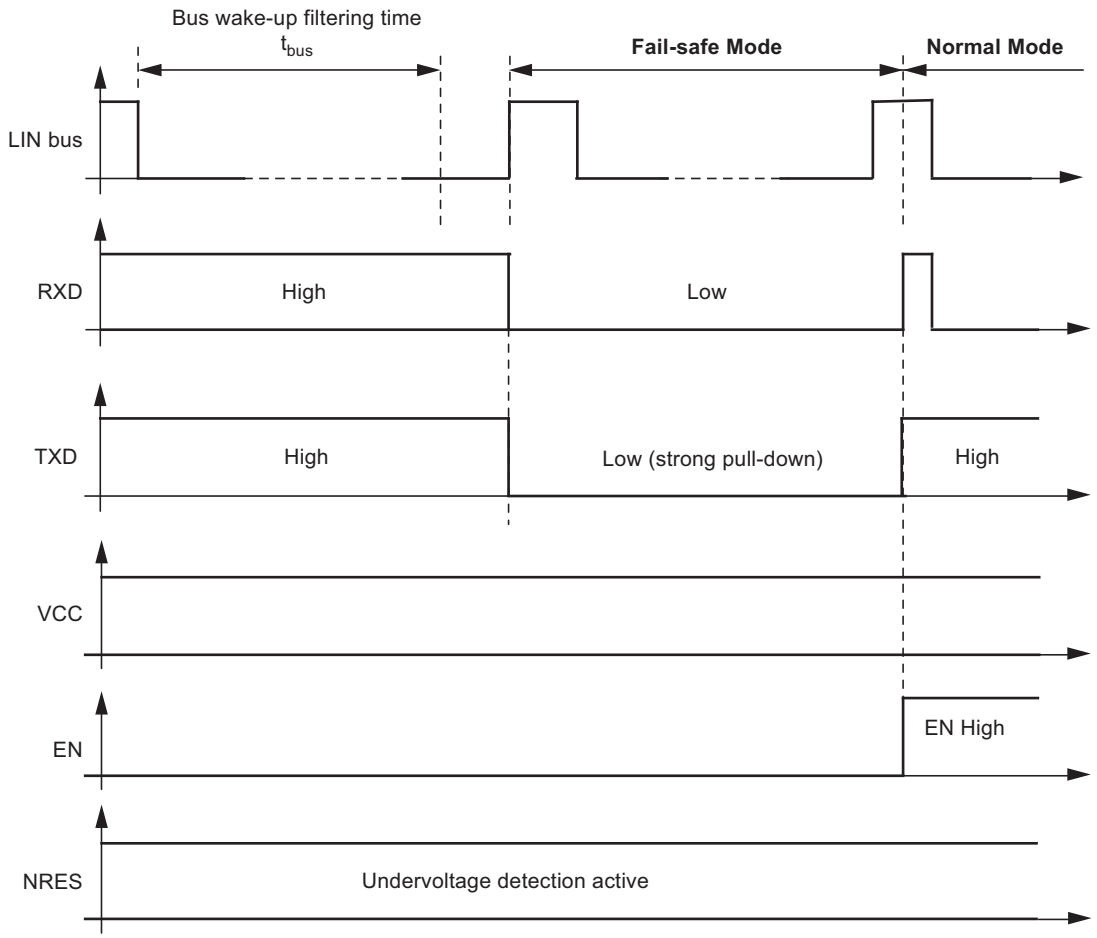
4.3 Wake-up Scenarios from Silent Mode or Sleep Mode

4.3.1 Remote Wake-up via LIN Bus

4.3.1.1 Remote Wake-up from Silent Mode

A remote wake-up from silent mode is only possible if TXD is high. A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) and the following rising edge at pin LIN (see Figure 4-4) results in a remote wake-up request. The device switches from silent mode to fail-safe mode, the VCC voltage regulator remains activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD and TXD (strong pull-down at TXD). EN high can be used to switch directly to normal mode.

Figure 4-4. LIN Wake-up from Silent Mode



4.3.1.2 Remote Wake-up from Sleep Mode

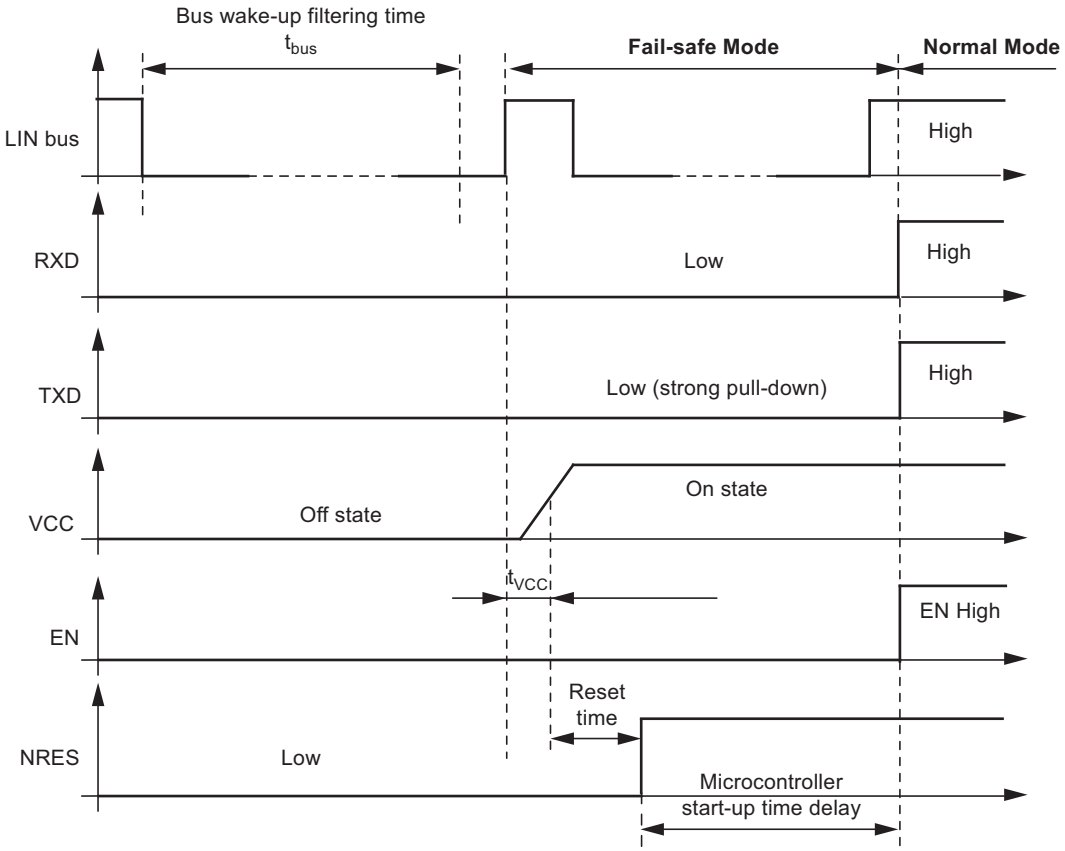
A voltage less than the LIN pre-wake detection V_{LINL} at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (> t_{bus}) together with a subsequent rising edge at the LIN pin results in a remote wake-up request. The device switches from sleep mode to fail-safe mode.

The VCC regulator is activated, and the internal LIN slave termination resistor is switched ON. The remote wake-up request is indicated by a low level at RXD and TXD (strong pull-down at TXD) (see Figure 4-5).

EN high can be used to switch directly from sleep/silent to fail-safe mode. If EN is still high after V_{VCC} ramp-up and the undervoltage reset time, the IC switches to normal mode.

Figure 4-5. LIN Wake-up from Sleep Mode



4.3.2 Local Wake-up via WKin Pin

A falling edge at the WKin pin followed by a low level maintained for a certain time period (> t_{WKin}) results in a local wake-up request. The device switches to fail-safe mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. When the WKin pin is low, it is possible to switch to silent mode or sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high > 10µs before the negative edge at WKin starts a new local wake-up request.

Figure 4-6. Local Wake-up from Sleep Mode

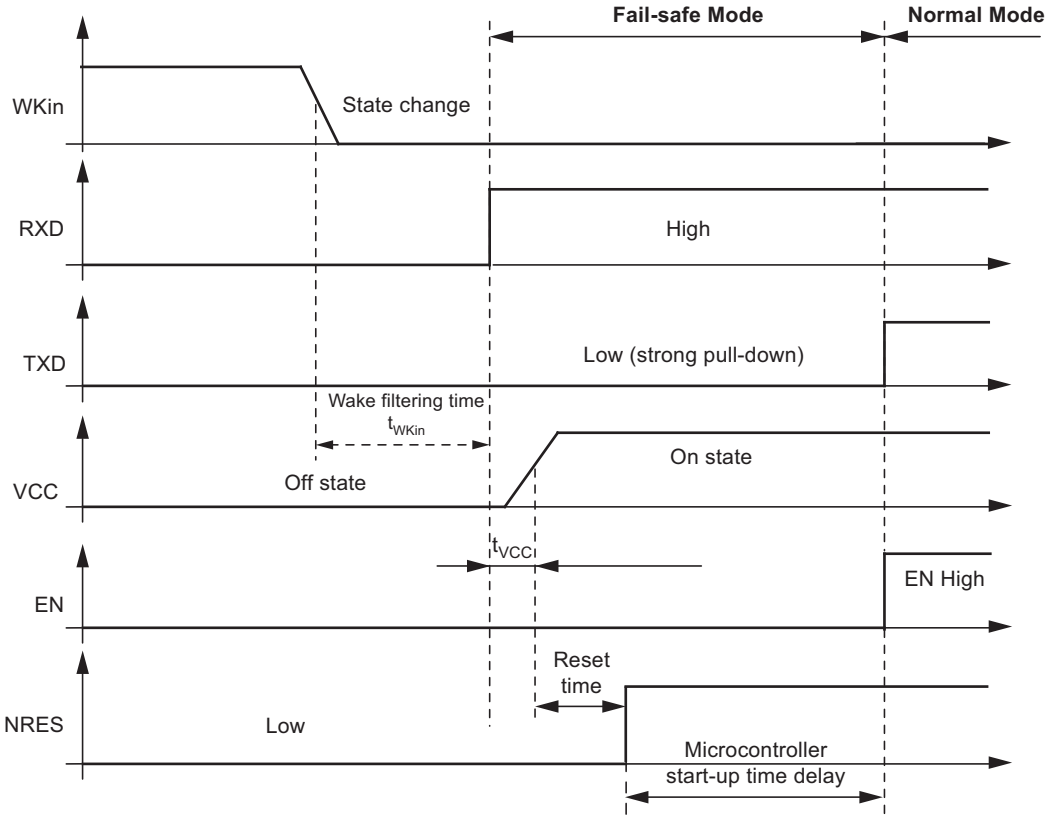
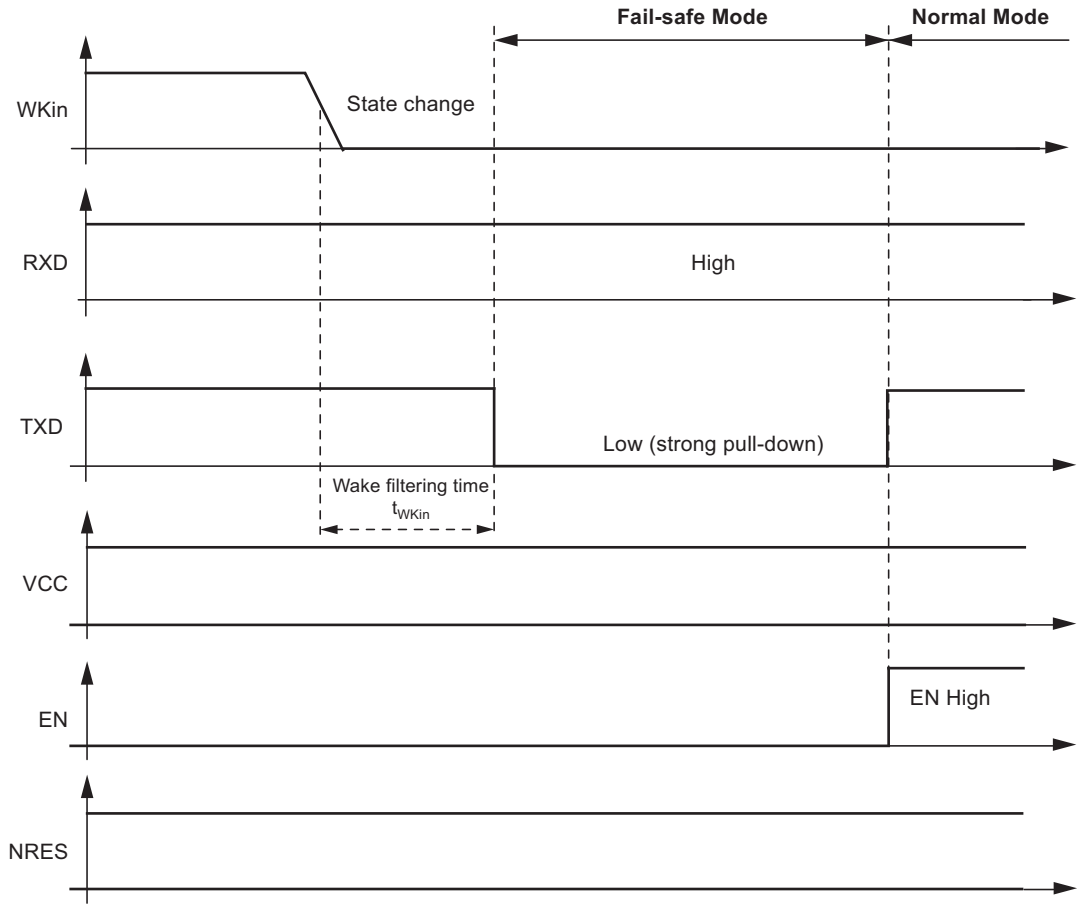


Figure 4-7. Local Wake-up from Silent Mode



4.3.3 Wake-up Source Recognition

The device can distinguish between different wake-up sources (see Table 4-3). The wake-up source can be read on the TXD and RXD pin in fail-safe mode. These flags are immediately reset if the microcontroller sets the EN pin to high and the IC is in normal mode.

Table 4-3. Signaling in Fail-safe Mode

Fail-safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin)	Low	High
$V_{VS\_th\_N\_F\_down}$ (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

4.4 Behavior under Low Supply Voltage Conditions

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor. If V_{VS} is higher than the minimum VS operation threshold $V_{VS\_th\_U\_F\_up}$ (typ. 2.25V), the IC mode changes from unpowered mode to fail-safe mode. As soon as V_{VS} exceeds the undervoltage threshold $V_{VS\_th\_F\_N\_up}$ (typ. 4.6V), the LIN transceiver and the dual low-side switches can be activated. The VCC output voltage reaches its nominal value after t_{VCC}. This parameter depends on the externally applied VCC capacitor and the load. The NRES output is low for the reset time delay t_{reset}. During this time t_{reset}, no mode change is possible.

The behaviour of VCC, NRES and VS is shown in following diagrams (ramp-up and ramp-down):

Figure 4-8. VCC and NRES versus VS (Ramp-up) for Atmel ATA663331

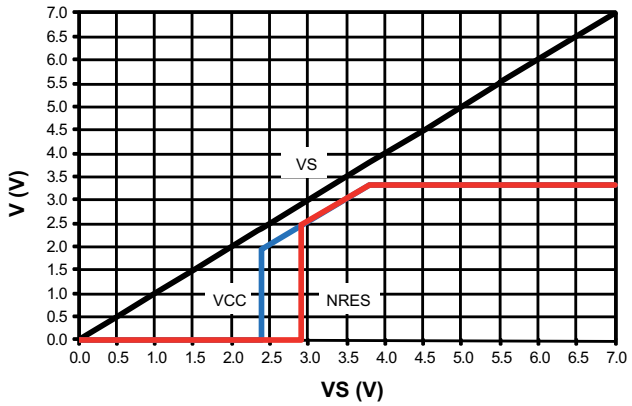


Figure 4-9. VCC and NRES versus VS (Ramp-down) for Atmel ATA663331

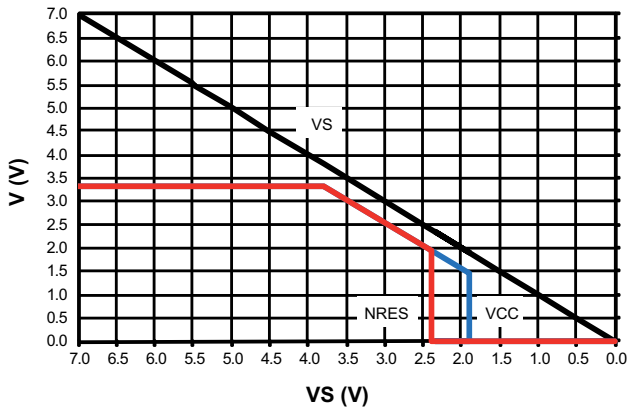


Figure 4-10. VCC and NRES versus VS (Ramp-up) for ATA663354

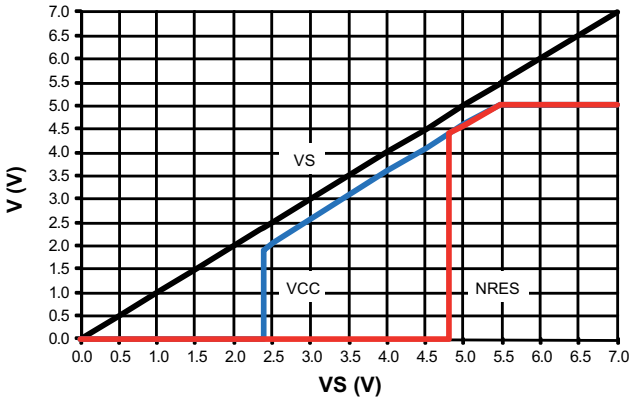
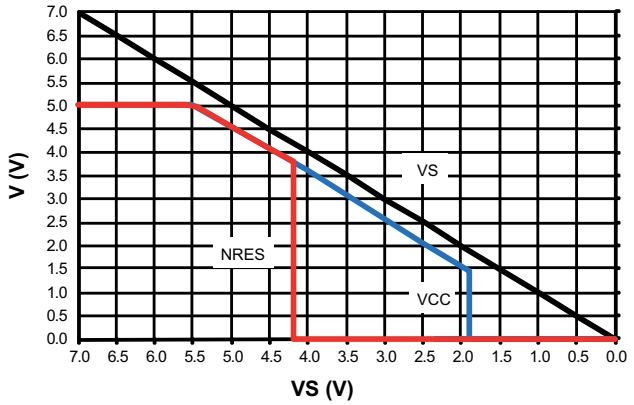


Figure 4-11. VCC and NRES versus VS (Ramp-down) for ATA663354



Please note that the upper graphs are only valid if the VS ramp-up and ramp-down time is much slower than the VCC ramp-up time t_{Vcc} and the NRES delay time t_{reset}.

If during **sleep mode** the voltage level of V_{VS} drops below the undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typ. 4.3V), the operation mode is not changed and no wake-up is possible. Only if the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typ. 2.05V), does the IC switch to unpowered mode.

If during **silent mode** the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ the IC switches into fail-safe mode. If the supply voltage on pin VS drops below the VS operation threshold $V_{VS\_th\_U\_down}$ (typ. 2.05V), does the IC switch to unpowered mode.

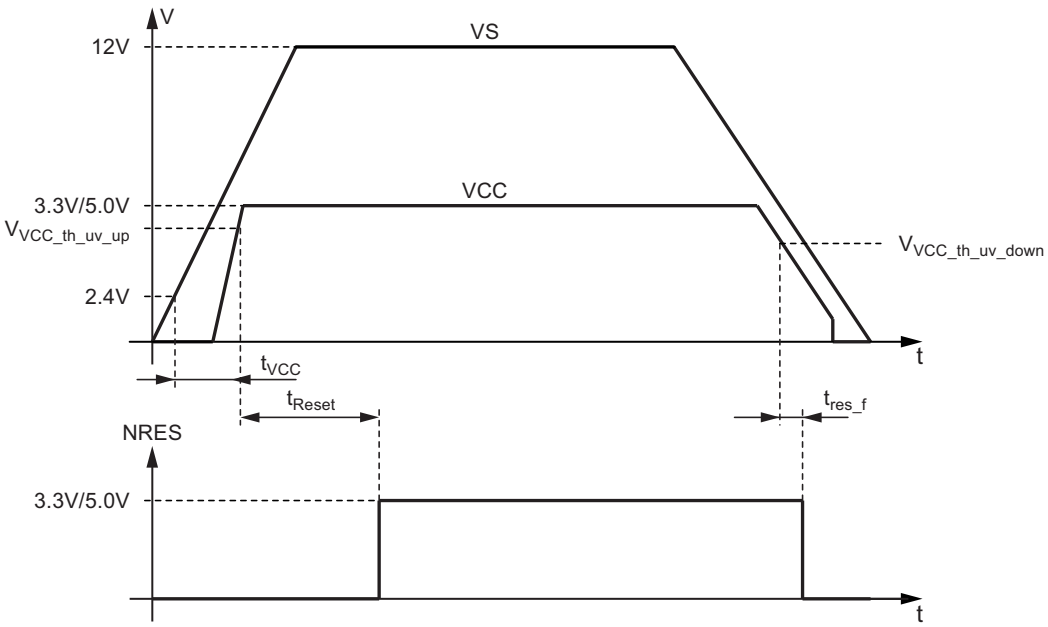
If during **normal mode** the voltage level on pin VS drops below the VS undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typ. 4.3V), the IC switches to fail-safe mode. This means the LIN transceiver and the dual low-side drivers are disabled in order to avoid malfunctions or false bus messages. The voltage regulator remains active.

> **For ATA663331**: In this undervoltage situation it is possible to switch the device into sleep mode or silent mode by a falling edge at the EN input. This feature ensures that switching into these two current saving modes is always possible, allowing current consumption to be even further reduced.
>
> When the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ (typ. 2.6V) the IC switches into fail-safe mode.
>
> **For ATA663354**: Because of the VCC undervoltage condition in this situation, the IC is in fail-safe mode and can be switched into sleep mode only.
>
> Only when the supply voltage V_{VS} drops below the operation threshold $V_{VS\_th\_U\_down}$ (typ. 2.05V) does the IC switch to unpowered mode.

The current consumption of the ATA6633xx in silent mode or in fail-safe mode is always below 170µA, even when the supply voltage V_{VS} is lower than the regulator's nominal output voltage VCC.

4.5 Voltage Regulator

Figure 4-12. VCC Voltage Regulator: Supply Voltage Ramp-up and Ramp-down

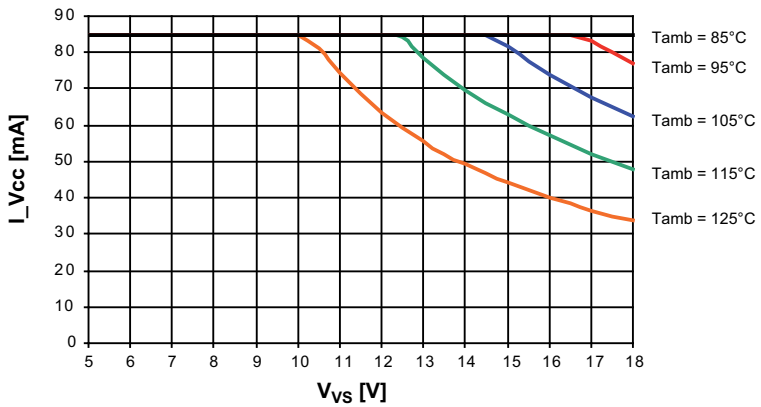


The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use a MLC capacitor with a minimum capacitance of 3.5µF together with a 100nF ceramic capacitor. Depending on the application, the values of these capacitors can be modified by the customer.

When the Atmel® ATA6633xx is being soldered onto the PCB, it is mandatory to connect the heat slug with a wide GND plate on the printed board to achieve a good heat sink.

The main power dissipation of the IC is created from the VCC output current I_{VCC}, which is needed for the application. Figure 4-13 shows the safe operating area of the Atmel ATA6633xx without considering any output current of the drivers (LS1out, LS2out, HSout).

Figure 4-13. Power Dissipation: Safe Operating Area: Regulator's Output Current I_{VCC} versus Supply Voltage V_{VS} at Different Ambient Temperatures (R_{thja} = 45K/W assumed)



5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_{VS} - DC voltage - T_a = 25°C, t_{Pulse} ≤ 500ms, I_{VCC} ≤ 85mA - T_a = 25°C, t_{Pulse} ≤ 2min, I_{VCC} ≤ 85mA	V_{VS}	–0.3		+40 +43.5 +28	V
Logic pin voltage levels (TXD, EN, HSin, LS1in, LS2in, NRES)	V_{LOGIC}	–0.3		+5.5	V
LIN bus levels V_{LIN} - DC voltage - Pulse time ≤ 500ms	V_{LIN}	–27		+40 +43.5	V V
V_{VCC} - DC voltage - DC input current	V_{VCC} I_{VCC}	–0.3		+5.5 +200	V mA
Logic level pins injection currents - t_{Pulse} ≤ 2min	I_{LOGIC}	–5		+5	mA
HSout - DC voltage - DC output current - DC current injection levels V_{HSout} < 0V and V_{HSout} > V_{VS}	V_{HSout} I_{HSout} I_{HSout}	–0.3 –50 –20		V_{VS} + 0.3 +10	V mA mA
LS1out and LS2out - DC voltage - DC output current	V_{LSout} I_{LSout}	–0.3		+42.5 +250	V mA
LS1out and LS2out clamping energies - Single event - Repetitive (f ≤ 5Hz)	E_{AS} E_{AR}	10 2			mJ
WKin voltage levels - DC voltage -Transient voltage according to ISO7637 (coupling 1nF), (with 2.7kΩ serial resistor)	V_{WKin}	–0.3 –150		+40 +100	V
ESD according to IBEE LIN EMC Test spec. 1.0 following IEC 61000-4-2 - Pin VS, WKin and LIN to GND (WKin with ext. circuitry acc. applications diagram)		±6			kV
ESD according to ISO10605, with 330pF/330Ω - Pin HSout (100Ω series resistor, 22nF to GND) to GND		±6			kV
ESD (HBM following STM5.1 with 1.5kΩ / 100pF) - Pin VS, LIN, HSout to GND - Pin WKin to GND		 ±6 ±5			 kV kV
Component Level ESD (HBM acc. ANSI/ESD STM5.1) JESD22-A114 AEC-Q100 (002)		±3			kV
CDM ESD STM 5.3.1		±750			V

5. Absolute Maximum Ratings (Continued)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
ESD machine model AEC-Q100-RevF(003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

6. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thjC}		8		K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to JEDEC	R_{thja}		45		K/W
Thermal shutdown of VCC regulator	T_{VCCoff}	150	165	180	°C
Thermal shutdown of LIN output	T_{LINoff}	150	165	180	°C
Thermal shutdown of driver stages	T_{DSoff}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

7. Electrical Characteristics

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	VS pin								
1.1	Nominal DC voltage range		VS	V_{VS}	5	13.5	28	V	A
1.2	Supply current in sleep mode	Sleep mode V_{LIN} > V_{VS} – 0.5V V_{VS} < 14V, T = 27°C	VS	$I_{VSsleep}$	5	10	15	µA	B
		Sleep mode V_{LIN} > V_{VS} – 0.5V V_{VS} < 14V	VS	$I_{VSsleep}$	3	11	18	µA	A
		Sleep mode, V_{LIN} = 0V Bus shorted to GND V_{VS} < 14V	VS	$I_{VSsleep\_short}$	20	50	100	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.3	Supply current in silent mode	Bus recessive 5.5V < V_{VS} < 14V, all drivers off without load at VCC T = 27°C	VS	$I_{VSsilent}$	30	47	58	µA	B
		Bus recessive 5.5V < V_{VS} < 14V, all drivers off without load at VCC	VS	$I_{VSsilent}$	30	50	64	µA	A
		Bus recessive 2V < V_{VS} < 5.5V, all drivers off without load at VCC	VS	$I_{VSsilent}$	50	130	170	µA	A
		Silent mode 5.5V < V_{VS} < 14V, all drivers off Bus shorted to GND without load at VCC	VS	$I_{VSsilent\_short}$	50	80	120	µA	A
1.4	Supply current in normal mode	Bus recessive V_{VS} < 14V, all drivers off without load at VCC	VS	I_{VSrec}	150	230	300	µA	A
1.5	Supply current in normal mode	Bus dominant (internal LIN pull-up resistor active) V_{VS} < 14V, all drivers off without load at VCC	VS	I_{VSdom}	200	700	950	µA	A
1.6	Supply current in fail-safe mode	Bus recessive 5.5V < V_{VS} < 14V, all drivers off without load at VCC	VS	I_{VSfail}	40	55	80	µA	A
		Bus recessive 2V < V_{VS} < 5.5V, all drivers off without load at VCC	VS	$I_{VSsilent}$	50	130	170	µA	A
1.7	VS undervoltage threshold (switching from normal mode to fail-safe mode)	Decreasing supply voltage	VS	$V_{VS\_th\_N\_F\_down}$	3.9	4.3	4.7	V	A
		Increasing supply voltage	VS	$V_{VS\_th\_F\_N\_up}$	4.1	4.6	4.9	V	A
1.8	VS undervoltage hysteresis		VS	$V_{VS\_hys\_F\_N}$	0.1	0.25	0.4	V	A
1.9	VS operation threshold (switching to unpowered mode)	Switch to unpowered mode	VS	$V_{VS\_th\_U\_down}$	1.9	2.05	2.3	V	A
		Switch from unpowered mode to fail-safe mode	VS	$V_{VS\_th\_U\_F\_up}$	2.0	2.25	2.4	V	A
1.10	VS undervoltage hysteresis		VS	$V_{VS\_hys\_U}$	0.1	0.2	0.3	V	A
2	RXD output pin								
2.1	Low level output sink capability	Normal mode, V_{LIN} = 0V, I_{RXD} = 2mA	RXD	V_{RXDL}		0.2	0.4	V	A
2.2	High level output source capability	Normal mode V_{LIN} = V_{VS}, I_{RXD} = –2mA	RXD	V_{RXDH}	V_{VCC} – 0.4V	V_{VCC} – 0.2V		V	A
3	TXD input/output pin								
3.1	Low-level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		TXD	V_{TXDH}	2		V_{VCC} + 0.3V	V	A
3.3	Pull-up resistor	V_{TXD} = 0V	TXD	R_{TXD}	40	70	100	kΩ	A
3.4	High-level leakage current	V_{TXD} = V_{VCC}	TXD	I_{TXD}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.5	Low-level output sink current at wake-up request	Fail-safe Mode $V_{LIN} = V_{VS}$ V_{WAKE} = 0V V_{TXD} = 0.4V	TXD	I_{TXD}	2	2.5	8	mA	A
4	EN input pin								
4.1	Low-level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		EN	V_{ENH}	2		V_{VCC} + 0.3V	V	A
4.3	Pull-down resistor	$V_{EN} = V_{VCC}$	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
5	NRES open drain output pin								
5.1	Low-level output voltage	$V_{VS} \geq 5.5V$ I_{NRES} = 2mA	NRES	V_{NRESL}		0.2	0.4	V	A
5.2	Undervoltage reset time	$V_{VS} \geq 5.5V$ C_{NRES} = 20pF	NRES	t_{Reset}	2	4	6	ms	A
5.3	Reset debounce time for falling edge	$V_{VS} \geq 5.5V$ C_{NRES} = 20pF	NRES	t_{res_f}	0.5		10	µs	A
5.4	Switch-off leakage current	V_{NRES} = 5.5V	NRES	I_{NRES_L}	–3		+3	µA	A
6	VCC voltage regulator Atmel ATA663331								
6.1	Output voltage VCC	4V < V_{VS} < 18V (0mA to 50mA)	VCC	V_{VCCnor}	3.234		3.366	V	A
		4.5V < V_{VS} < 18V (0mA to 85mA)	VCC	V_{VCCnor}	3.234		3.366	V	C
6.2	Output voltage V_{VCC} at low V_{VS}	3V < V_{VS} < 4V	VCC	V_{VCClow}	$V_{VS} – V_D$		3.366	V	A
6.3	Regulator drop voltage	V_{VS} > 3V, I_{VCC} = –15mA	VCC	V_{D1}		100	150	mV	A
6.4	Regulator drop voltage	V_{VS} > 3V, I_{VCC} = –50mA	VCC	V_{D2}		300	500	mV	A
6.5	Line regulation maximum	4V < V_{VS} < 18V	VCC	VCC_{line}		0.1	0.2	%	A
6.6	Load regulation maximum	5mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
6.7	Output current limitation	V_{VS} > 4V	VCC	I_{VCClim}		–180	–120	mA	A
6.8	Load capacity	MLC capacitor	VCC	C_{load}	3.5	4.7		µF	D
6.9	VCC undervoltage threshold (NRES ON)	Referred to VCC V_{VS} > 4V	VCC	$V_{VCC\_th\_uv\_down}$	2.3	2.6	2.8	V	A
	VCC undervoltage threshold (NRES OFF)	Referred to VCC V_{VS} > 4V	VCC	$V_{VCC\_th\_uv\_up}$	2.4	2.7	2.9	V	A
6.10	Hysteresis of VCC undervoltage threshold	Referred to VCC V_{VS} > 4V	VCC	$V_{VCC\_hys\_uv}$	100	200	300	mV	A
6.11	Ramp-up time V_{VS} > 4V to VCC = 3.3V	C_{VCC} = 4.7µF I_{load} = –5mA at VCC	VCC	t_{VCC}		1	1.5	ms	A
7	VCC voltage regulator Atmel ATA663354								
7.1	Output voltage VCC	5.5V < V_{VS} < 18V (0mA to 50mA)	VCC	V_{VCCnor}	4.9		5.1	V	A
		6V < V_{VS} < 18V (0mA to 85mA)	VCC	V_{VCCnor}	4.9		5.1	V	C
7.2	Output voltage V_{VCC} at low V_{VS}	4V < V_{VS} < 5.5V	VCC	V_{VCClow}	$V_{VS} – V_D$		5.1	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.3	Regulator drop voltage	V_{VS} > 4V, I_{VCC} = –20mA	VCC	V_{D1}		100	200	mV	A
7.4	Regulator drop voltage	V_{VS} > 4V, I_{VCC} = –50mA	VCC	V_{D2}		300	500	mV	A
7.5	Regulator drop voltage	V_{VS} > 3.3V, I_{VCC} = –15mA	VCC	V_{D3}			150	mV	A
7.6	Line regulation maximum	5.5V < V_{VS} < 18V	VCC	VCC_{line}		0.1	0.2	%	A
7.7	Load regulation maximum	5mA < I_{VCC} < 50mA	VCC	VCC_{load}		0.1	0.5	%	A
7.8	Output current limitation	V_{VS} > 5.5V	VCC	I_{VCClim}		–180	–120	mA	A
7.9	Load capacity	MLC capacitor	VCC	C_{load}	3.5	4.7		µF	D
7.10	VCC undervoltage threshold (NRES ON)	Referred to VCC V_{VS} > 4V	VCC	$V_{VCC\_th\_uv\_down}$	4.2	4.4	4.6	V	A
	VCC undervoltage threshold (NRES OFF)	Referred to VCC V_{VS} > 4V	VCC	$V_{VCC\_th\_uv\_up}$	4.3	4.6	4.8	V	A
7.11	Hysteresis of undervoltage threshold	Referred to VCC V_{VS} > 5.5V	VCC	$V_{VCC\_hys\_uv}$	100	200	300	mV	A
7.12	Ramp-up time V_{VS} > 5.5V to V_{VCC} = 5V	C_{VCC} = 4.7µF I_{load} = –5mA at VCC	VCC	t_{VCC}		1	1.5	ms	A
8	LIN bus driver: bus load conditions: Load 1 (Small): 1nF, 1kΩ; Load 2 (Large): 10nF, 500Ω; C_{RXD} = 20pF, Load 3 (Medium): 6.8nF, 660Ω characterized on samples 10.7 and 10.8 specifies the timing parameters for proper operation at 20kBit/s and 10.9kBit/s and 10.10kBit/s at 10.4kBit/s								
8.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	0.9 × V_{VS}		V_{VS}	V	A
8.2	Driver-dominant voltage	V_{VS} = 7V R_{load} = 500Ω	LIN	$V_{\_LoSUP}$			1.2	V	A
8.3	Driver-dominant voltage	V_{VS} = 18V R_{load} = 500Ω	LIN	$V_{\_HiSUP}$			2	V	A
8.4	Driver-dominant voltage	V_{VS} = 7V R_{load} = 1000Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
8.5	Driver-dominant voltage	V_{VS} = 18V R_{load} = 1000Ω	LIN	$V_{\_HiSUP\_1k}$	0.8			V	A
8.6	Pull-up resistor to V_{VS}	The serial diode is mandatory	LIN	R_{LIN}	20	30	47	kΩ	A
8.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
8.8	LIN current limitation V_{BUS} = V_{Bat_max}		LIN	I_{BUS_LIM}	40	120	200	mA	A
8.9	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current Driver off V_{BUS} = 0V V_{VS} = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1	–0.35		mA	A
8.10	Leakage current LIN recessive	Driver off 8V < V_{VS} < 18V 8V < V_{BUS} < 18V V_{BUS} ≥ V_{VS}	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
8.11	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	GND_{Device} = V_{VS} V_{VS} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.12	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{VS} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_bat}$		0.1	2	µA	A
8.13	Capacitance on the LIN pin to GND		LIN	C_{LIN}			20	pF	D
9	LIN bus receiver								
9.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN	V_{BUS_CNT}	0.475 × V_{VS}	0.5 × V_{VS}	0.525 × V_{VS}	V	A
9.2	Receiver dominant state	V_{EN} = 5V/3.3V	LIN	V_{BUSdom}	–27		0.4 × V_{VS}	V	A
9.3	Receiver recessive state	V_{EN} = 5V/3.3V	LIN	V_{BUSrec}	0.6 × V_{VS}		40	V	A
9.4	Receiver input hysteresis	V_{hys} = V_{th_rec} – V_{th_dom}	LIN	V_{BUShys}	0.028 × V_{VS}	0.1 × V_{VS}	0.175 × V_{VS}	V	A
9.5	Pre-wake detection LIN High-level input voltage		LIN	V_{LINH}	V_{VS} – 2V		V_{VS} + 0.3V	V	A
9.6	Pre-wake detection LIN Low-level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_{VS} – 3.3V	V	A
10	Internal timers								
10.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	50	100	150	µs	A
10.2	Time delay for mode change from fail-safe mode to normal mode via the EN pin	V_{EN} = 5V/3.3V	EN	t_{norm}	5	15	20	µs	A
10.3	Time delay for mode change from normal mode to sleep mode via the EN pin	V_{EN} = 0V	EN	t_{sleep}	5	15	20	µs	A
10.4	TXD-dominant time-out time	V_{TXD} = 0V	TXD	t_{dom}	20	40	60	ms	A
10.6	Time delay for mode change from silent mode to normal mode via the EN pin	V_{EN} = 5V/3.3V	EN	t_{s_n}	5	15	40	µs	A
10.7	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_{VS} $TH_{Dom(max)}$ = 0.581 × V_{VS} V_{VS}= 7.0V to 18V t_{Bit} = 50µs D1 = $t_{bus\_rec(min)}$/(2 × t_{Bit})	LIN	D1	0.396				A
10.8	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × V_{VS} $TH_{Dom(min)}$ = 0.284 × V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 50µs D2 = $t_{bus\_rec(max)}$/(2 × t_{Bit})	LIN	D2			0.581		A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.9	Duty cycle 3	$TH_{Rec(max)}$ = 0.778 × V_{VS} $TH_{Dom(max)}$ = 0.616 × V_{VS} V_{VS} = 7.0V to 18V t_{Bit} = 96µs D3 = $t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
10.10	Duty cycle 4	$TH_{Rec(min)}$ = 0.389 × V_{VS} $TH_{Dom(min)}$ = 0.251 × V_{VS} V_{VS} = 7.6V to 18V t_{Bit} = 96µs D4 = $t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A
10.11	Slope time falling and rising edge at LIN	V_{VS} = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
10.12	TXD release time after dominant time-out detection		TXD	t_{DTOrel}	10		20	µs	B
11	Receiver electrical AC parameters of the LIN physical layer LIN receiver, RXD load conditions: C_{RXD} = 20pF								
11.1	Propagation delay of receiver	V_{VS} = 7.0V to 18V t_{rx_pd} = max(t_{rx_pdr}, t_{rx_pdf})	RXD	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_{VS} = 7.0V to 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}	RXD	t_{rx_sym}	–2		+2	µs	A
12	WKin pin								
12.1	High-level input voltage		WKin	V_{WKinH}	V_{VS} – 1V		V_{VS} + 0.3V	V	A
12.2	Low-level input voltage	Initializes a wake-up signal	WKin	V_{WKinL}	–1		V_{VS} – 3.3V	V	A
12.3	WKin pull-up current	V_{VS} < 28V, V_{WKin} = 0V	WKin	I_{WKin}	–30	–10	–3	µA	A
12.4	High-level leakage current	V_{VS} = 28V, V_{WKin} = 28V	WKin	I_{WKinL}	–5		+5	µA	A
12.5	Debounce time of low pulse for wake-up via WKin pin	V_{WKin} = 0V	WKin	t_{WKin}	50	100	150	µs	A
13	WKout pin								
13.1	Low level output sink capability	V_{WKin} = V_{VS} I_{WKout} = 2mA	WKout	V_{WKoutL}		0.2	0.4	V	A
13.2	High level output source capability	V_{WKin} = 0V I_{WKout} = –2mA	WKout	V_{WKoutH}	V_{VCC} – 0.4V	V_{VCC} – 0.2V		V	A
14	LS1out, LS2out pins								
14.1	Output drain-to-source on resistance	I_{LSout} = 100mA	LSout	$R_{DSon,LS}$			3	Ω	A
14.2	Leakage current	–0.2V < V_{LSout} < 40V	LSout	I_{LSleak}			10	µA	A
14.3	Active clamping voltage	I_{LSout} = 20mA	LSout	$V_{LSclamp}$	43	44	48	V	A
14.4	Short-circuit detection threshold	5.5V < V_{VS} < 28V	LSout	V_{SCth_LS}	1.25	1.5	1.75	V	A
14.9	Switch-on slope (fall time)	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1nF transition from 80% down to 20% of V_{VS}	LSout	$t_{LSslope,fall}$	5		20	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
14.10	Switch-off slope (rise time)	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1nF transition from 20% to 80% of V_{VS}	LSout	$t_{LSslope,rise}$	5		20	µs	A
14.11	Switch-on delay	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1nF time from LSin = high to V_{LSout} = 50% of V_{VS}	LSout	t_{LSdel}	5		30	µs	A
14.12	Switch-off delay	V_{VS} = 16V R_{load} = 100Ω C_{load} = 1nF time from LSin = low to V_{LSout} = 50% of V_{VS}	LSout	t_{LSdel}	20		50	µs	A
14.13	Short circuit detection debouncing time		LSout	t_{Lsdeb}	2	3.75	10	µs	B
15	LS1in, LS2in pins								
15.1	Low-level voltage input		LSin	V_{LSin_L}	–0.3		$0.3V_{VCC}$	V	A
15.2	High-level voltage input		LSin	V_{LSin_H}	$0.7V_{VCC}$		V_{VCC} + 0.3	V	A
15.3	Pull-down resistor	V_{LSin} = V_{VCC}	LSin	R_{LSin}	50	100	150	kΩ	A
15.4	Low-level input current	V_{LSin} = 0V	LSin	I_{LSin}	–1		+1	µA	A
15.5	Maximum switching frequency	$R_{Load,LSxout}$ ≥ 100Ω $L_{Load,LSxout}$ ≤ 1mH	LSin	$f_{LSin,max}$	1			kHz	D
16	HSout pin								
16.1	Output drain-to-source on resistance	I_{HSout} = –20mA	HSout	$R_{DSon,HS}$			20	Ω	A
16.2	Leakage current	–0.2V < V_{HSout} < V_{VS} + 0.2V	HSout	$I_{leak,HS}$			2	µA	A
16.5	Switch-off slope (fall time)	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1nF transition from 80% down to 20% of V_{VS}	HSout	$t_{HSslope,fall}$	0.5		5	µs	A
16.6	Switch-on slope (rise time)	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1nF transition from 20% to 80% of V_{VS}	HSout	$t_{HSslope,rise}$	0.5		5	µs	A
16.7	Switch-on delay	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1nF time from HSin=HIGH to V_{HSout} = 50% of V_{VS}	HSout	t_{HSdel}	3		20	µs	A
16.8	Switch-off delay	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1nF time from HSin=LOW to V_{HSout} = 50% of V_{VS}	HSout	t_{HSdel}	3		20	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

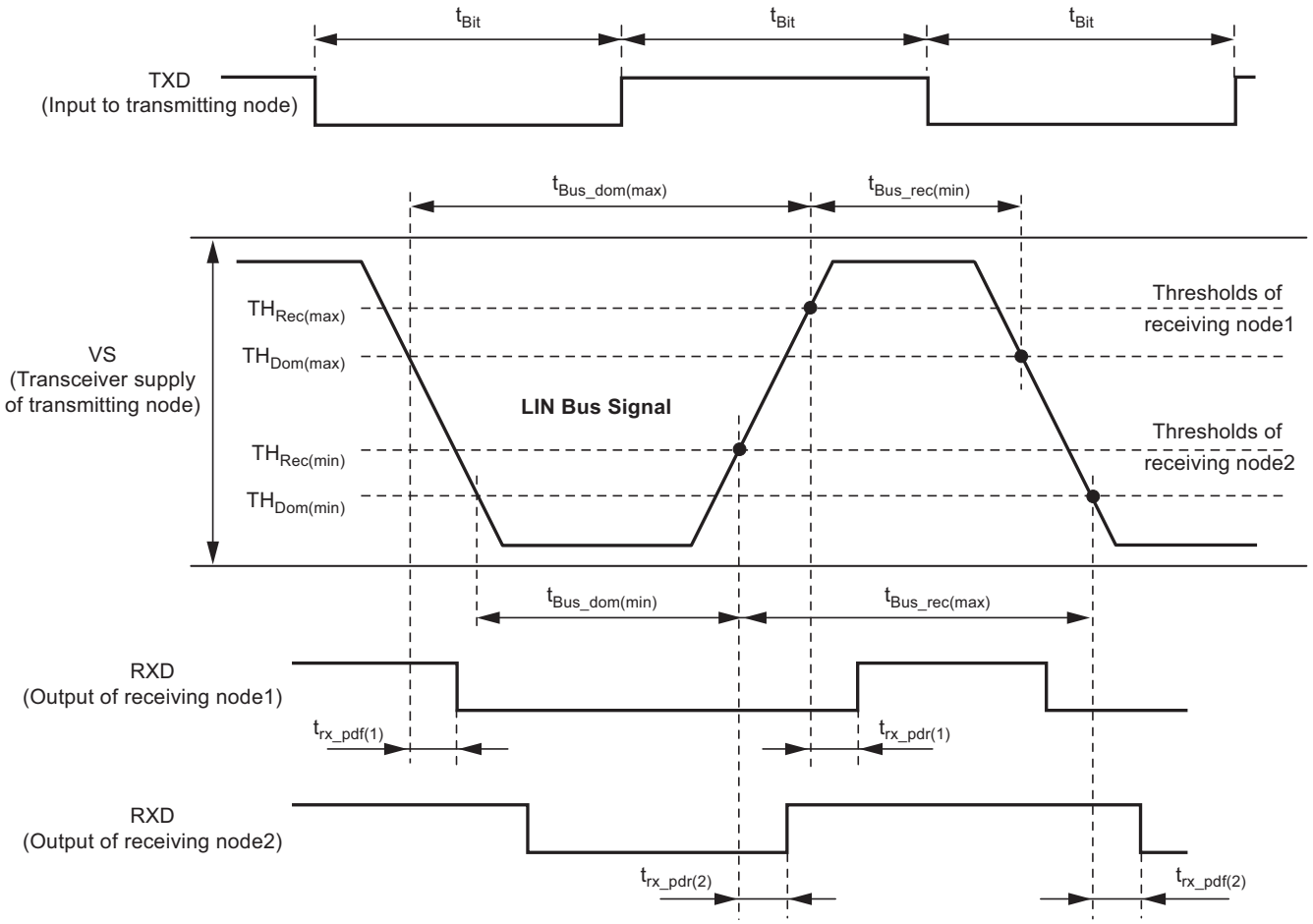
7. Electrical Characteristics (Continued)

5V < V_{VS} < 28V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
16.9	Short-circuit detection threshold		HSout	V_{SCth_HS}	V_{VS} – 6V		V_{VS} – 2V	V	A
16.10	Short-circuit deb. time		HSout	t_{HS_deb}	2		10	µs	A
17	HSin pin								
17.1	Low-level voltage input		HSin	V_{HSin_L}	–0.3		$0.3V_{VCC}$	V	A
17.2	High-level voltage input		HSin	V_{HSin_H}	$0.7V_{VCC}$		V_{VCC} + 0.3	V	A
17.3	Pull-down resistor	V_{HSin} = V_{VCC}	HSin	R_{HSin}	50	100	150	kΩ	A
17.4	Low-level input current	V_{HSin} = 0V	HSin	I_{HSin}	–1		+1	µA	A
17.5	Maximum switching frequency	R_{load} = 560Ω	LSin	$f_{HSin,max}$	5			kHz	D

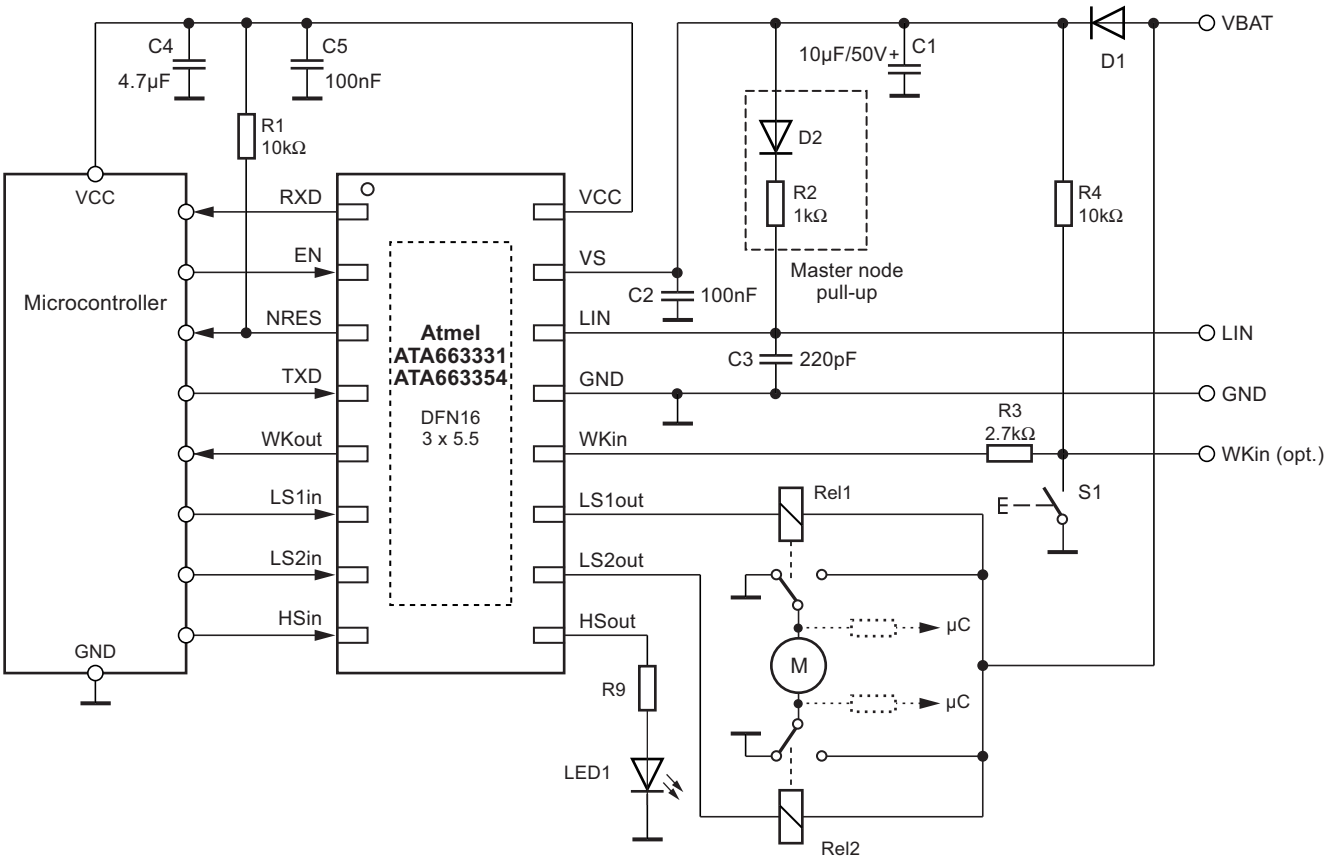
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 7-1. Definition of Bus Timing Characteristics



8. Application Circuits

Figure 8-1. Typical Application Circuit

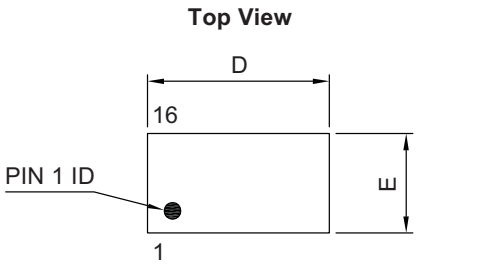


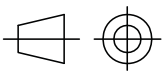
Note: Heat Slug must be connected to ground.

9. Ordering Information

Extended Type Number	Package	Remarks
ATA663331-GDQW	DFN16	3.3V LIN system basis chip, Pb-free, 6k, taped and reeled
ATA663354-GDQW	DFN16	5V LIN system basis chip, Pb-free, 6k, taped and reeled

10. Package Information

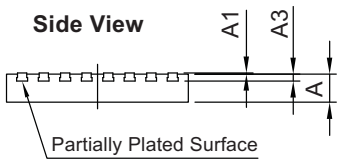


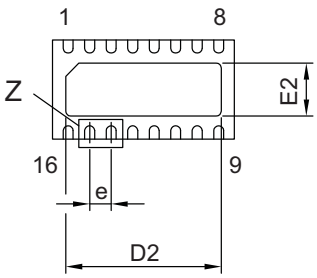


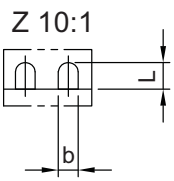
technical drawings
according to DIN
specifications

Dimensions in mm

Two Step Singulation process







COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.8	0.85	0.9	
A1	0.0	0.035	0.05	
A3	0.16	0.21	0.26	
D	5.4	5.5	5.6	
D2	4.6	4.7	4.8	
E	2.9	3	3.1	
E2	1.5	1.6	1.7	
L	0.35	0.4	0.45	
b	0.25	0.3	0.35	
e		0.65		

10/11/13

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	Package: VDFN_5.5x3_16L Exposed pad 4.7x1.6		6.543-5168.01-4	1

11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9231A-AUTO-08/15	• Initial revision.

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