

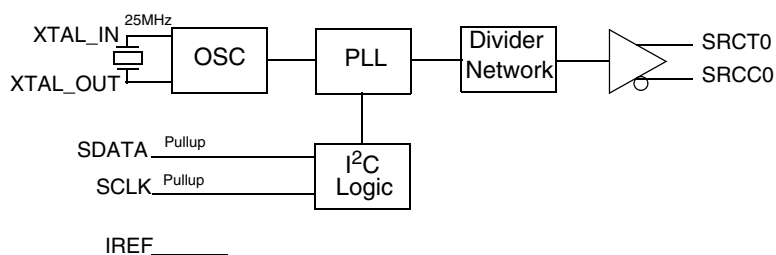
General Description

The 841S101 is a PLL-based clock synthesizer specifically designed for PCI_Express™ Clock applications. This device generates a 100MHz differential HCSL clock from a input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference is applied to the XTAL_IN pin with the XTAL_OUT pin left floating. The device offers spread spectrum clock output for reduced EMI applications. An I²C bus interface is used to enable or disable spread spectrum operation as well as select either a down spread value of -0.35% or -.5%. The 841S101 is available in a lead-free 16-Lead TSSOP package.

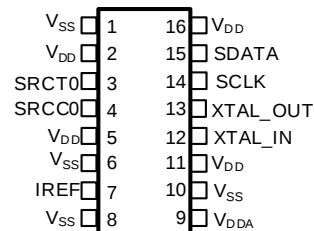
Features

- One 0.7V current mode differential HCSL output pair
- Crystal oscillator interface: 25MHz
- Output frequency: 100MHz
- RMS phase jitter @ 100MHz (12kHz – 20MHz): 1.23ps (typical)
- Cycle-to-cycle jitter: 20ps (maximum)
- I²C support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI) reduction
- 3.3V operating supply mode
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) package
- PCI Express Gen 1, 2 and 3 jitter compliant

Block Diagram



Pin Assignment



841S101
16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 6, 8, 10	V _{SS}	Power		Power supply ground.
2, 5, 11, 16	V _{DD}	Power		Power supply pins.
3, 4	SRCT0, SRCC0	Output		Differential output pair. HCSL interface levels.
7	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode SRCCx, SRCTx clock outputs.
9	V _{DDA}	Power		Analog supply for PLL.
12, 13	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
14	SCLK	Input	Pullup	I ² C compatible SCLK. This pin has an internal pullup resistor. Open drain. LVCMOS/LVTTL interface levels.
15	SDATA	I/O	Pullup	I ² C compatible SDATA. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			2		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal I²C serial interface is provided. Through the Serial Data Interface, various device functions, such as clock output buffers, can be individually enabled or disabled. The registers associated with the

serial interface initialize to their default setting upon power-up, and therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually

indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 3A.

The block write and block read protocol is outlined in Table 3B, while Table 3C outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3A. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation.
6:5	Chip select address, set to "00" to access device.
4:0	Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be "00000".

Table 3B. Block Read and Block Write Protocol

Bit	Description = Block Write	Bit	Description = Block Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 1 - 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 - 8 bits	30:37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
	Data Byte/Slave Acknowledges	39:46	Data Byte 1 from slave - 8 bits
	Data Byte N - 8 bits	47	Acknowledge
	Acknowledge from slave	48:55	Data Byte 2 from slave - 8 bits
	Stop	56	Acknowledge
			Data Bytes from Slave/Acknowledge
			Data Byte N from slave - 8 bits
			Not Acknowledge

Table 3C. Byte Read and Byte Write Protocol

Bit	Description = Byte Write	Bit	Description = Byte Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data Byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Registers

Table 3D. Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	1	Reserved	Reserved
3	1	Reserved	Reserved
2	1	SRC[T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z) 1 = Enable
1	0	Reserved	Reserved
0	0	Reserved	Reserved

NOTE: Pup denotes Power-up.

Table 3E. Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 3F. Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	SRCT/C	Spread Spectrum Selection 0 = -0.35%, 1 = -0.5%
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	SRC	SRC Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 3G. Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 3H. Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	1	Reserved	Reserved

Table 3I. Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 3J. Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Hi-Z Select 0 = Hi-Z, 1 = REF/N
6	0	TEST_MODE	TEST Clock Mode Entry Control 0 = Normal Operation, 1 = REF/N or Hi-Z Mode
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

NOTE: Pup denotes Power-up.

Table 3K. Byte 7: Control Register 7

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	1		Vendor ID Bit 0

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.5V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, θ_{JA}	86.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.22$	3.3	V_{DD}	V
I_{DD}	Power Supply Current				80	mA
I_{DDA}	Analog Supply Current				22	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SDATA, SCLK	2.2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	SDATA, SCLK	-0.3		0.8	V
I_{IH}	Input High Current	SDATA, SCLK $V_{DD} = V_{IN} = 3.465V$			10	μA
I_{IL}	Input Low Current	SDATA, SCLK $V_{DD} = 3.465V, V_{IN} = 0V$	-150			μA

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. PCI Express Jitter Specifications, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	$f = 100MHz$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		13.3	19.3	86	ps
$t_{REFCLK_HF_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	$f = 100MHz$, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)		1.1	1.53	3.1	ps
$t_{REFCLK_LF_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	$f = 100MHz$, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.19	0.32	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	$f = 100MHz$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.18	0.30	0.8	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note* section in the datasheet.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 6B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			100		MHz
f_{REF}	Reference frequency			25		MHz
$\text{jit}(\emptyset)$	Phase Jitter, RMS (Random); NOTE 1	25MHz crystal, $f = 100\text{MHz}$, Integration Range: 12kHz – 20MHz		1.23		ps
$\text{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 2	PLL Mode			20	ps
t_L	PLL Lock Time				55	ms
F_M	SSC Modulation Frequency; NOTE 4	25MHz Crystal	30	32	33.33	kHz
SSC_{RED}	Spectral Reduction; NOTE 4		-7	-10		dB
V_{RB}	Ring-back Voltage Margin; NOTE 4, 5		-100		100	mV
V_{MAX}	Absolute Max. Output Voltage; NOTE 6, 7				1150	mV
V_{MIN}	Absolute Min. Output Voltage; NOTE 6, 8		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 6, 9, 10		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 6, 9, 11				140	mV
	Rise/Fall Edge Rate; NOTE 6, 12	Measured between 150mV to +150mV	0.6		4.0	V/ns
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized using a 25MHz quartz crystal.

NOTE 1: Refer to phase jitter plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Spread Spectrum clocking enabled.

NOTE 4: Measurement taken from differential waveform.

NOTE 5: T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150\text{mV}$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{RB} \pm 100\text{mV}$ differential range.

NOTE 6: Measurement taken from single-ended waveform.

NOTE 7: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 8: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

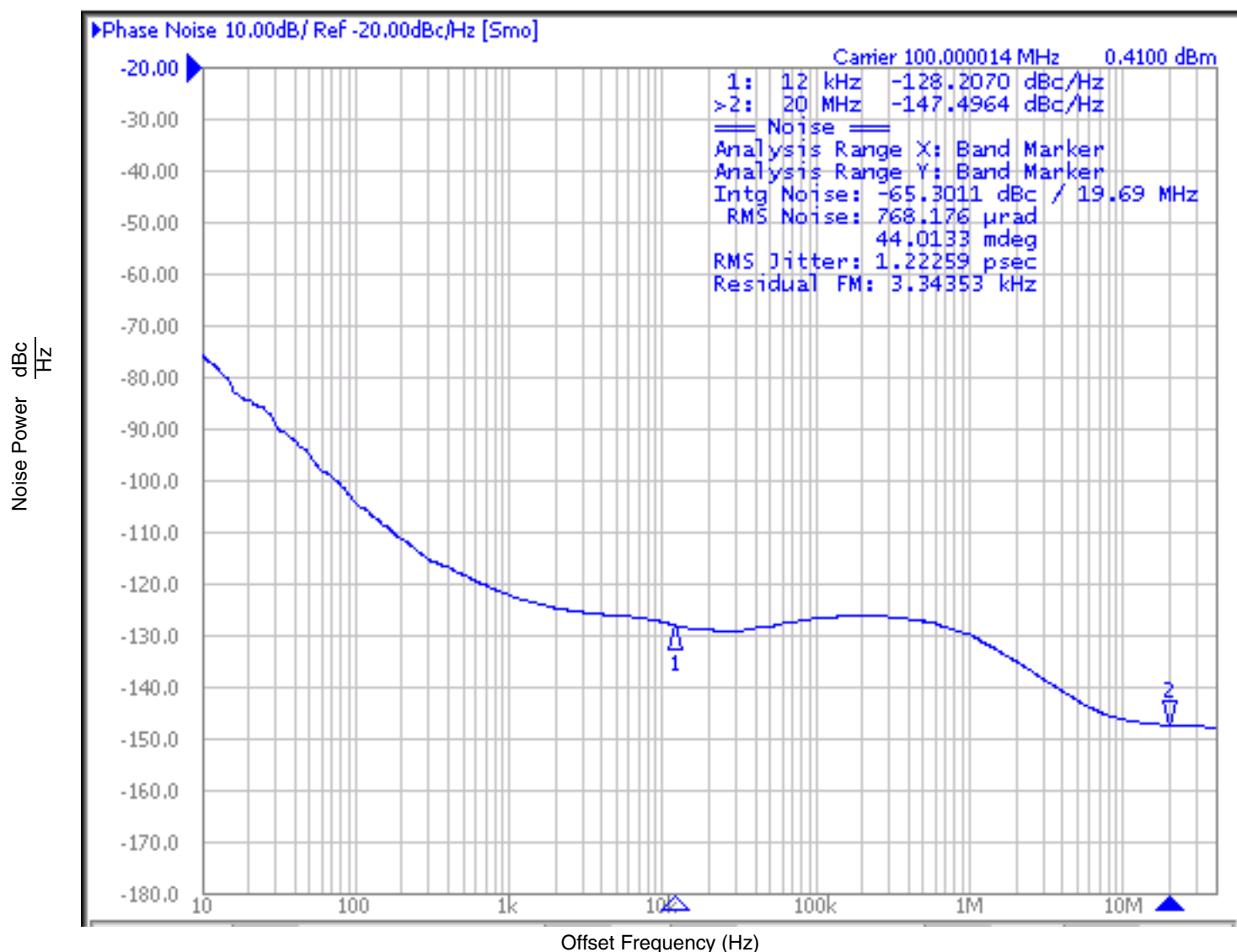
NOTE 9: Measured at crossing point where the instantaneous voltage value of the rising edge of SRCT equals the falling edge of SRCC.

NOTE 10: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

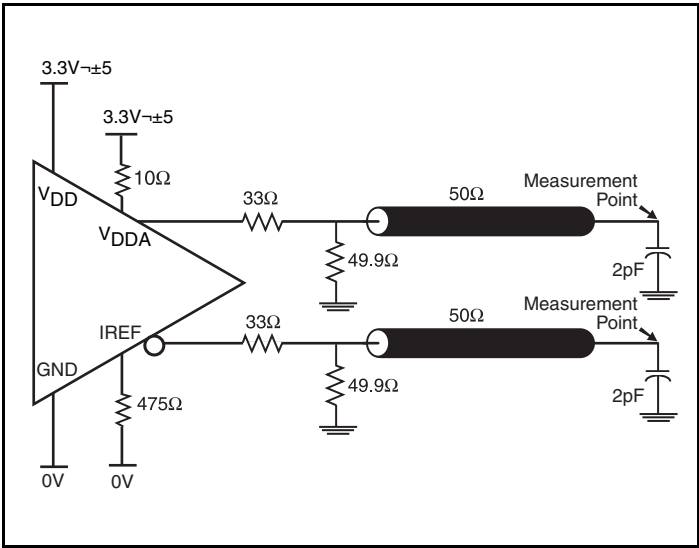
NOTE 11: Defined as the total variation of all crossing voltages of rising SRCT and falling SRCC, This is the maximum allowed variance in V_{cross} for any particular system.

NOTE 12: Measured from -150mV to +150mV on the differential waveform (SRCT minus SRCC). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

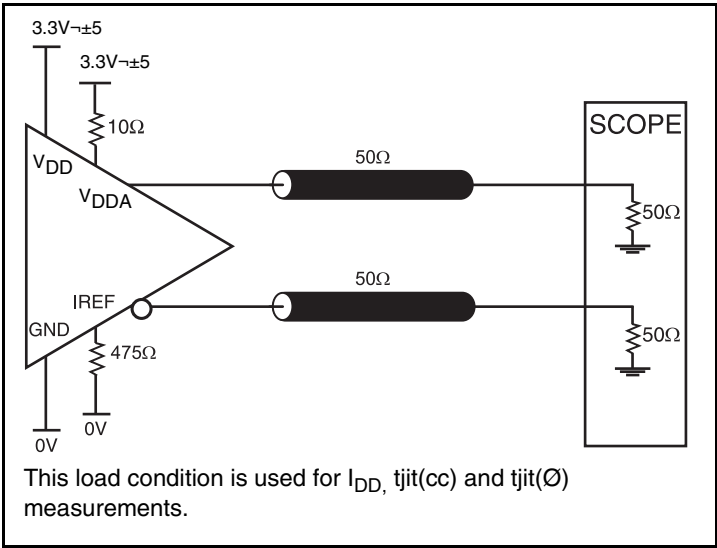
Typical Phase Noise at 100MHz



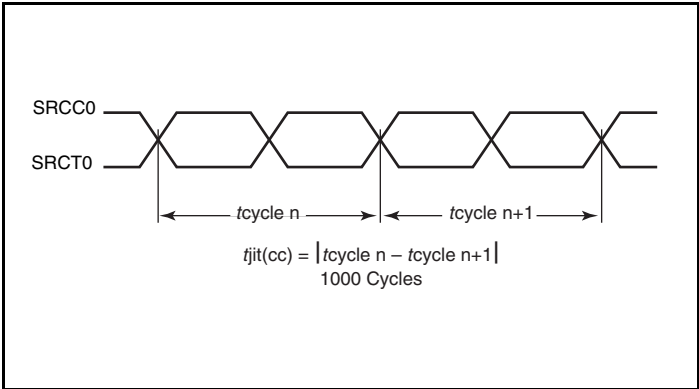
Parameter Measurement Information



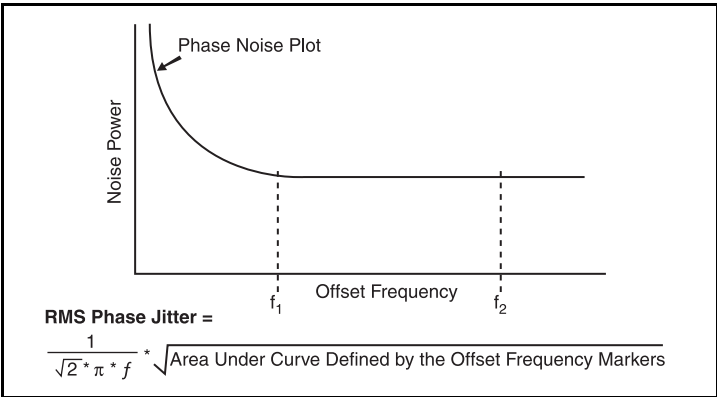
3.3V HCSL Output Load AC Test Circuit



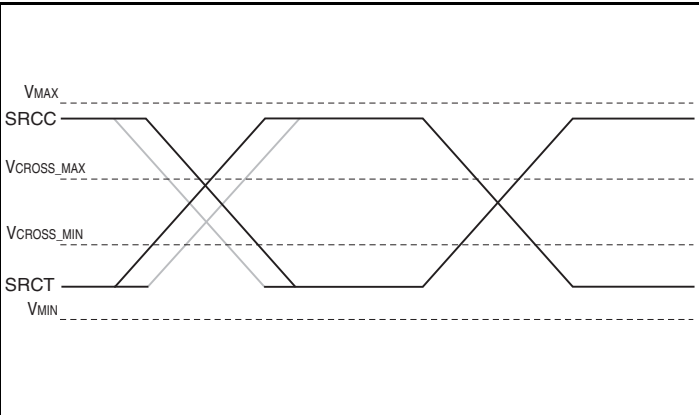
3.3V HCSL Output Load AC Test Circuit



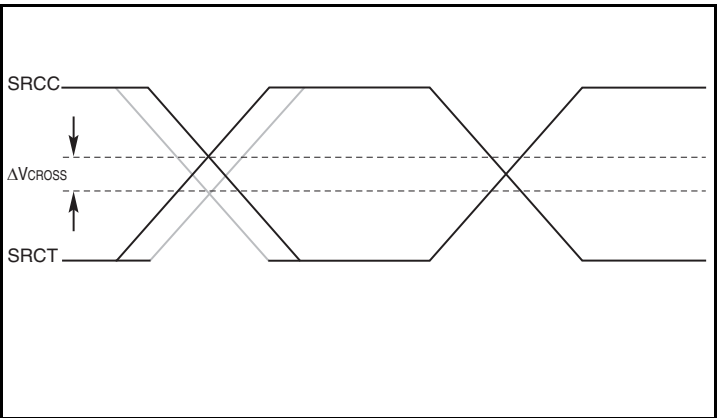
Cycle-to-Cycle Jitter



RMS Phase Jitter

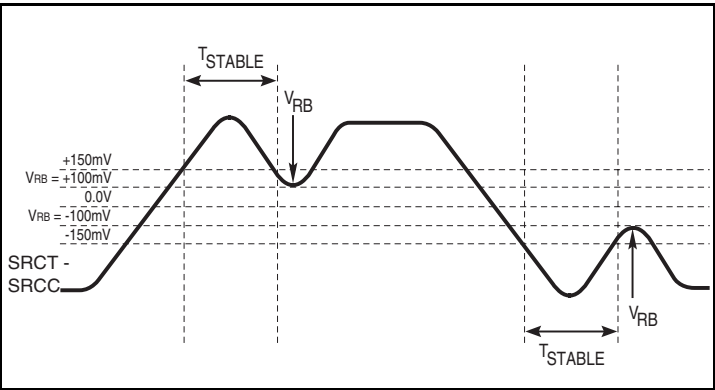


Single-ended Measurement Points for Absolute Cross Point and Swing

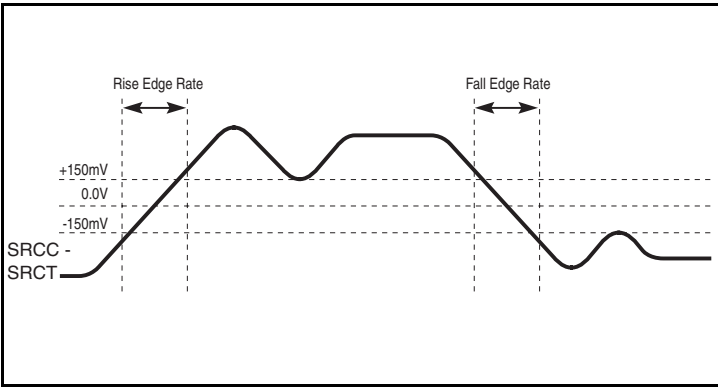


Single-ended Measurement Points for Delta Cross Point

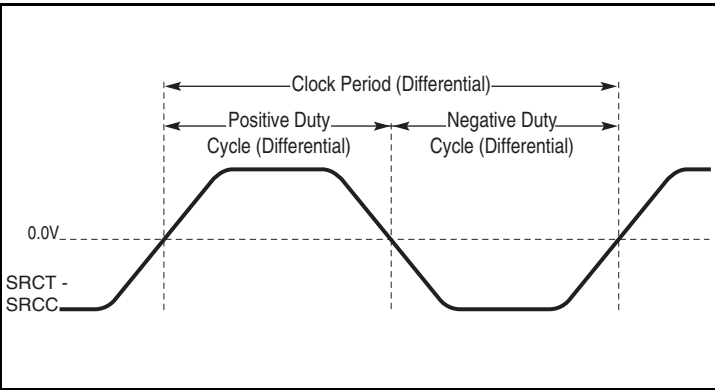
Parameter Measurement Information, continued



Differential Measurement Points for Ringback



Differential Measurement Points for Rise/Fall Edge Rate



Differential Measurement Points for Duty Cycle/Period

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841S101 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

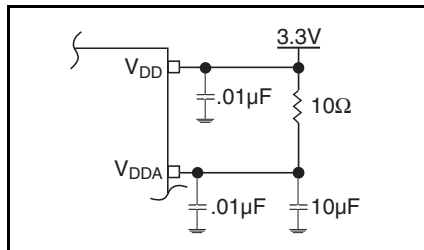


Figure 1. Power Supply Filtering

Recommendations for Unused Input Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

Crystal Input Interface

The 841S101 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and

were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

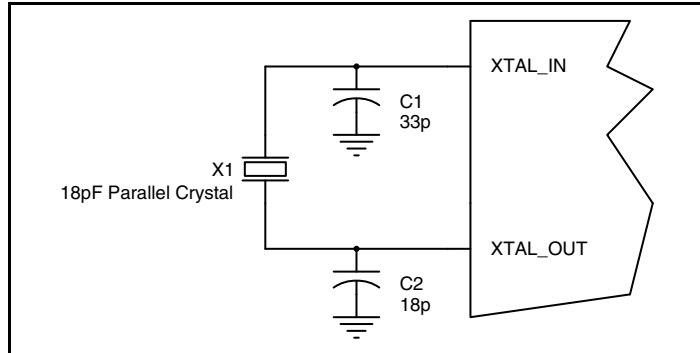


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

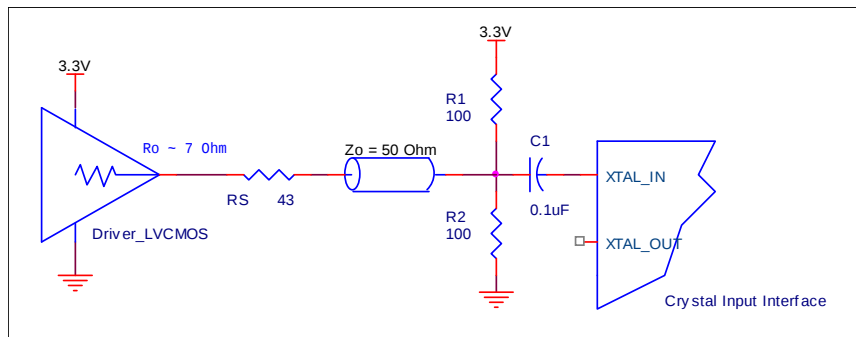


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

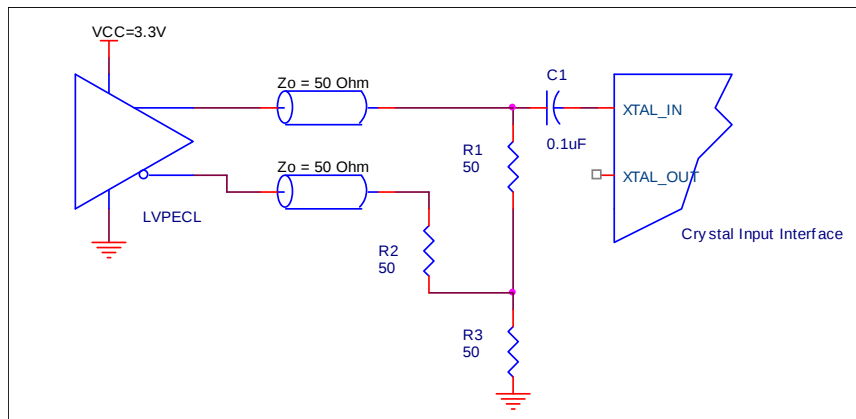


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommended Termination

Figure 4A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

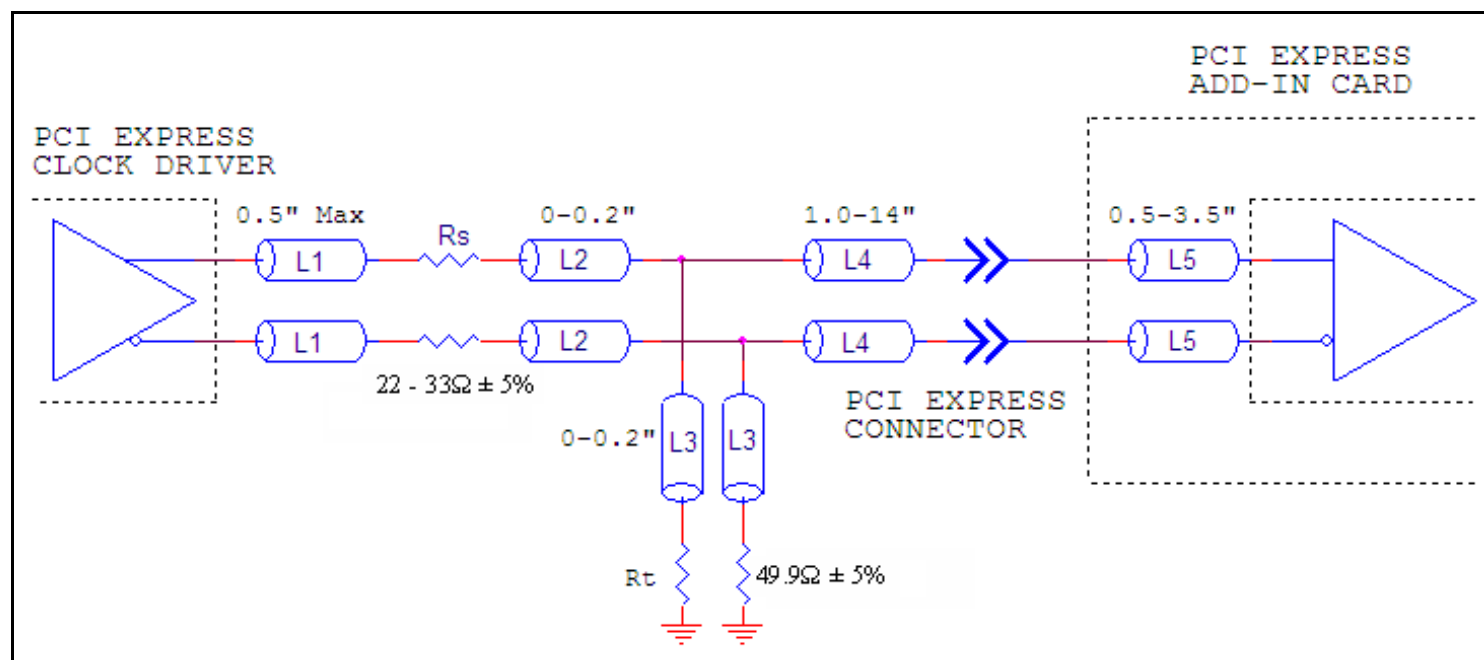


Figure 4A. Recommended Termination

Figure 4B is the recommended termination for applications which require a point to point connection and contain the driver and receiver

on the same PCB. All traces should all be 50Ω impedance.

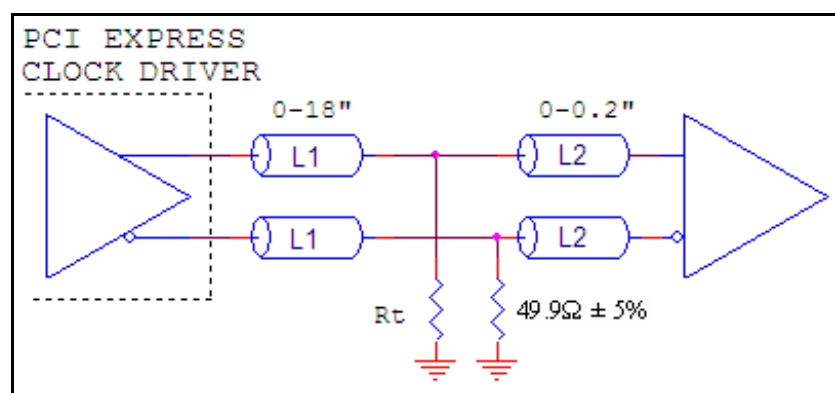


Figure 4B. Recommended Termination

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

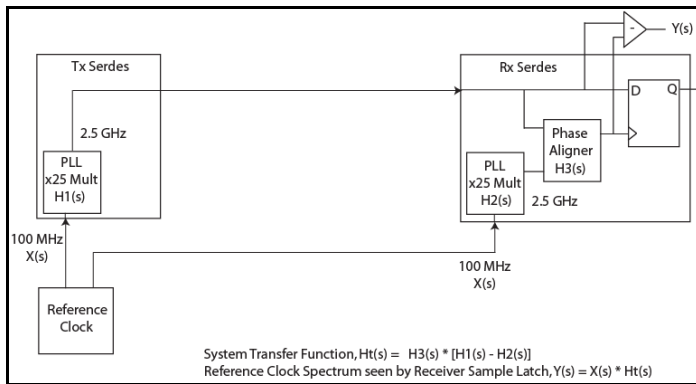
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

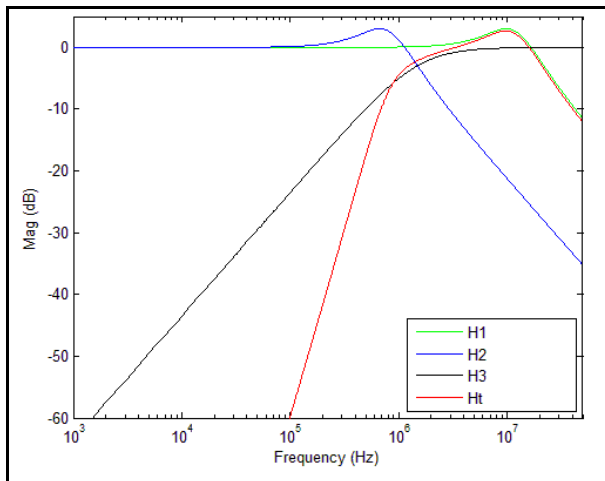
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on $X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$.



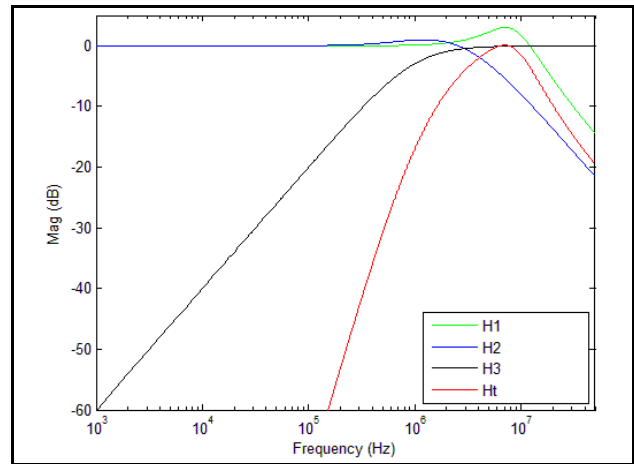
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

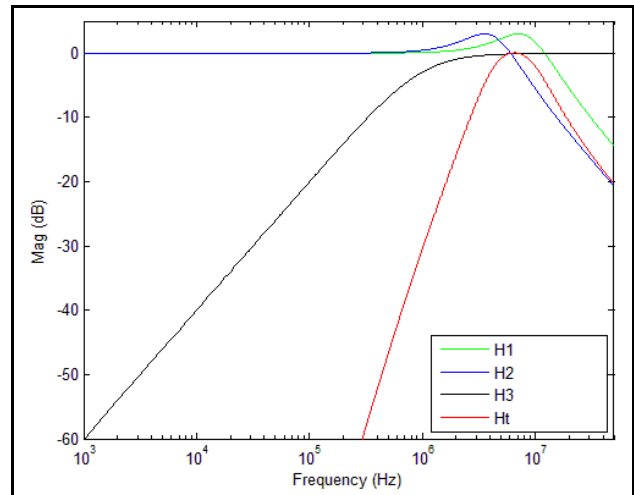


PCI Express Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

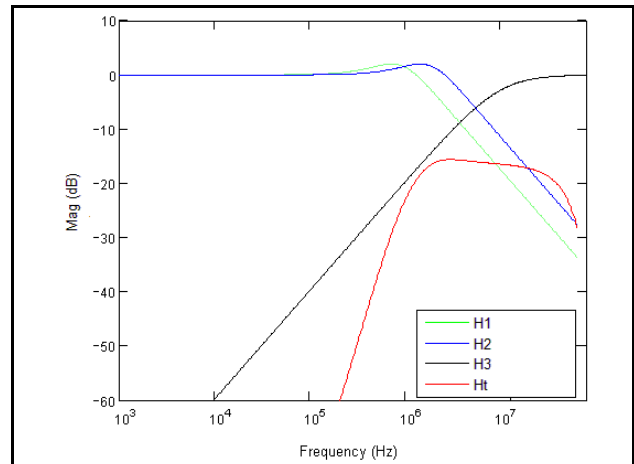


PCI Express Gen 2A Magnitude of Transfer Function



PCI Express Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCI Express Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

Schematic Layout

Figure 5 shows an example of 841S101 application schematic. In this example, the device is operated at $V_{DD} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The C1 = 18pF and C2 = 33pF are recommended for frequency accuracy. For different board layouts,

the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of HCSL termination are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

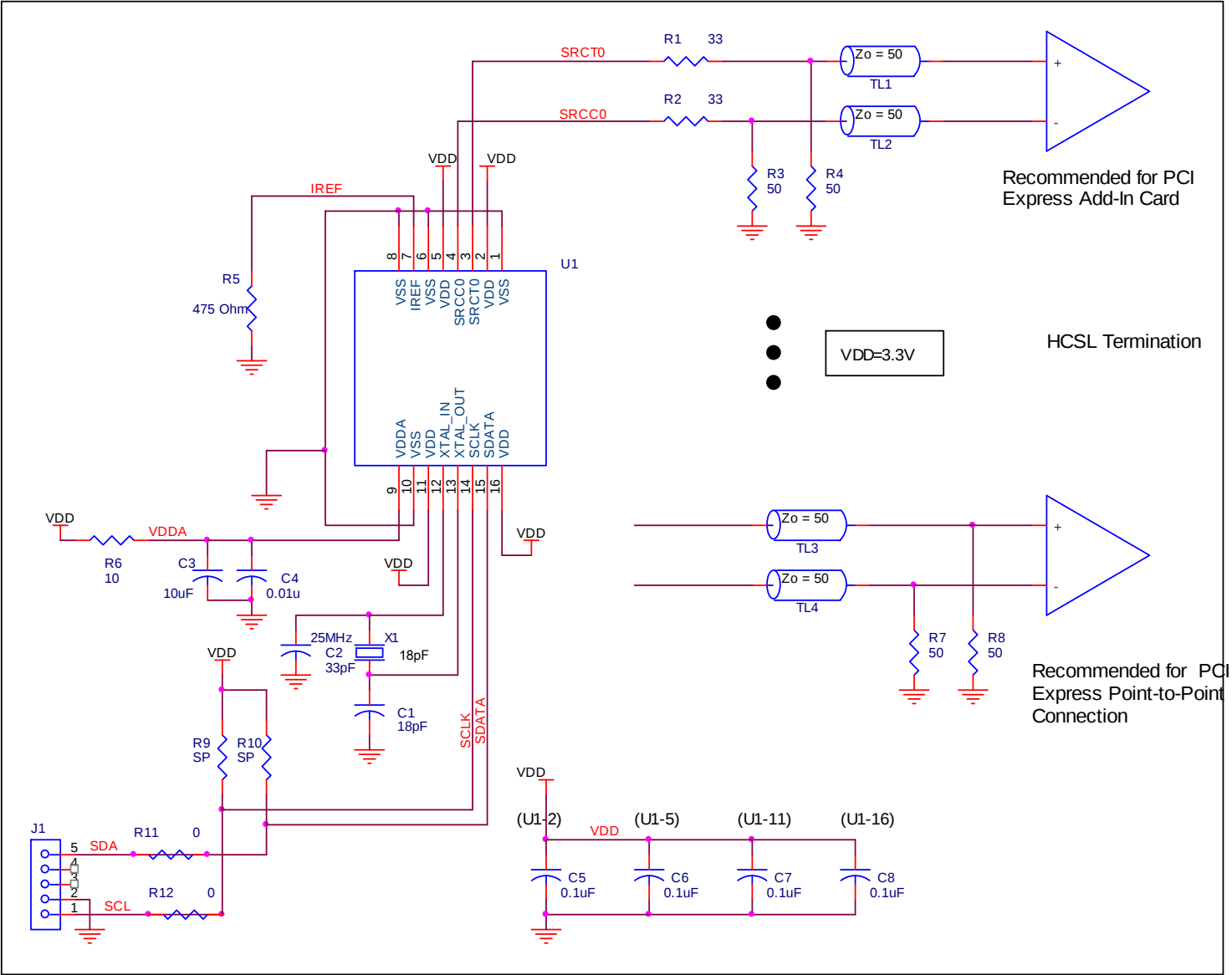


Figure 5. 841S101 Application Schematic.

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used with 0.5% down-spread from the nominal 100MHz clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 6A* below.

The 841S101 triangle modulation frequency deviation is 0.5% down-spread from the nominal clock frequency. An example of the

amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 6B*. The ratio of this difference to the fundamental frequency is typically 0.5%. The resulting spectral reduction will be greater than 7dB, as shown in *Figure 2B*. It is important to note the 841S101 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

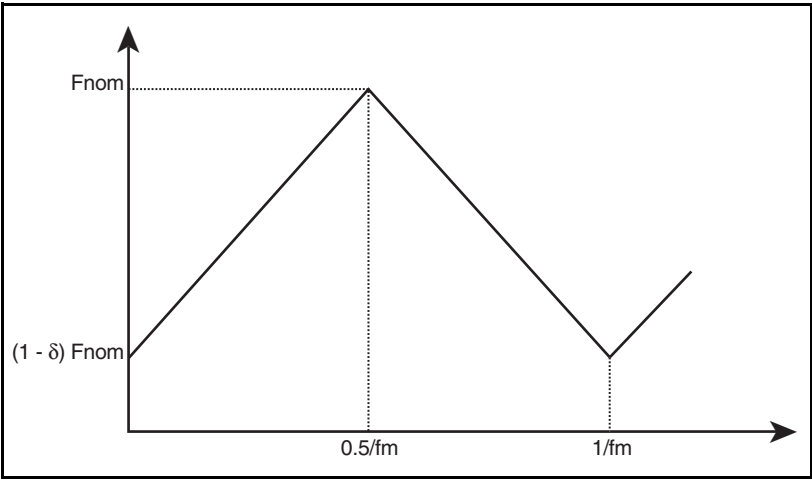


Figure 6A. Triangle Frequency Modulation

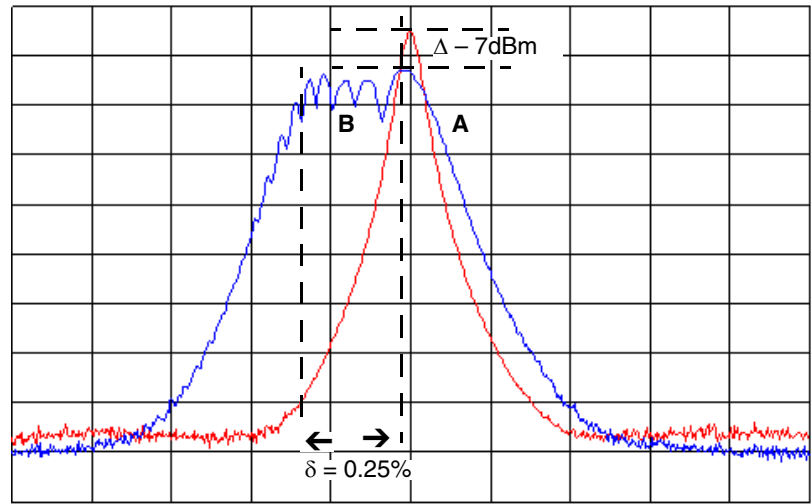


Figure 6B. 100MHz Clock Output In Frequency Domain
(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

Power Considerations

This section provides information on power dissipation and junction temperature for the 841S101. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 841S101 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85°C is as follows:

$$I_{DD_MAX} = 73mA$$

$$I_{DDA_MAX} = 19mA$$

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (73mA + 19mA) = \mathbf{318.78mW}$
- Power (outputs)_{MAX} = **44.5mW/Loaded Output pair**

$$\mathbf{Total\ Power_{_MAX} = 318.78mW + 44.5mW = 363.28mW}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.9°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.363W * 86.9^\circ C/W = 116.5^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.9°C/W	82.5°C/W	80.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 7*.

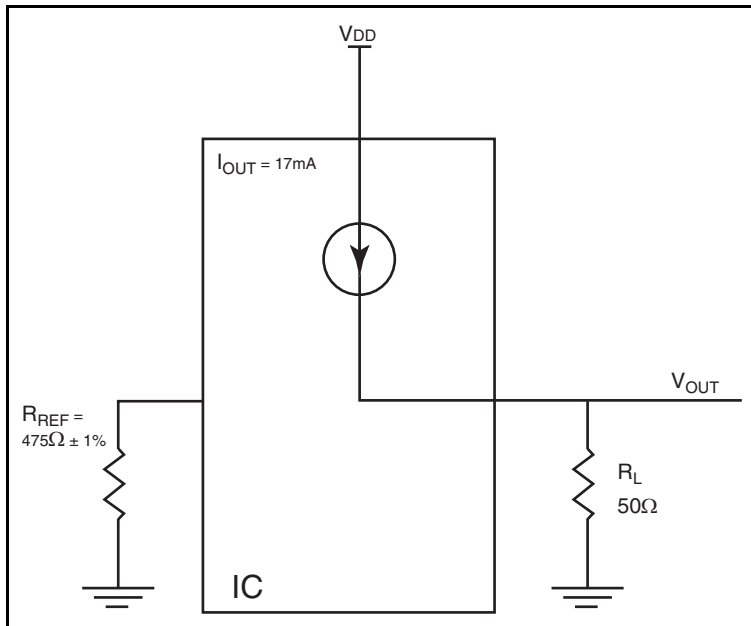


Figure 7. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX} .

$$\text{Power} = (V_{DD_MAX} - V_{OUT}) * I_{OUT},$$

$$\text{since } V_{OUT} = I_{OUT} * R_L$$

$$= (V_{DD_MAX} - I_{OUT} * R_L) * I_{OUT}$$

$$= (3.465V - 17mA * 50\Omega) * 17mA$$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.9°C/W	82.5°C/W	80.4°C/W

Transistor Count

The transistor count for 841S101 is: 11,775

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

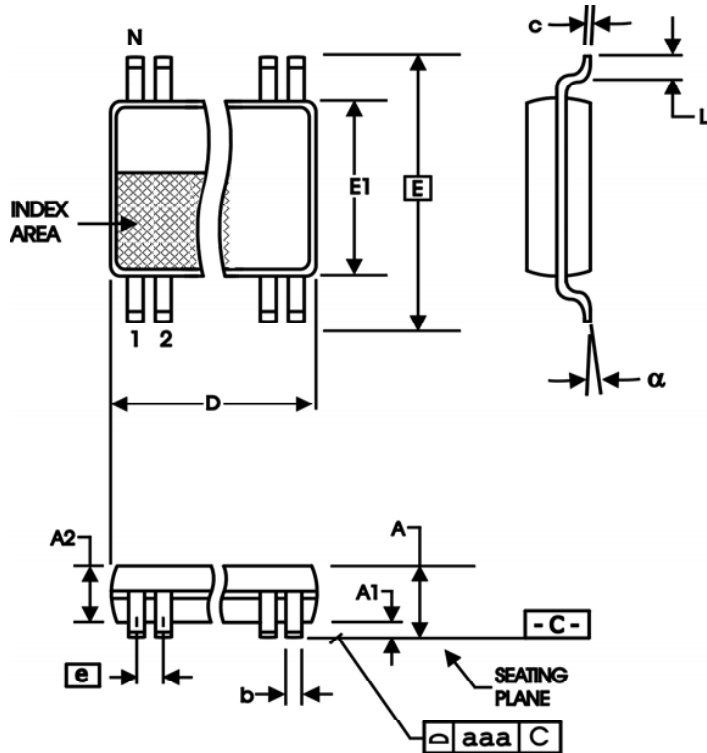


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa	0.10	

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841S101EGILF	1S101EIL	“Lead-Free” 16 Lead TSSOP	Tube	-40°C to 85°C
841S101EGILFT	1S101EIL	“Lead-Free” 16 Lead TSSOP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	10	21	Ordering Information Table - corrected marking.	6/24/10
B	10	22	Ordering Information Table - deleted Tape & Reel count and table note. Updated datasheet header/footer. Deleted "ICS" prefix, "I" suffix from part number	5/25/16

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
 4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
 5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
 6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
 7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
 8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
 9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
 10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
 11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/