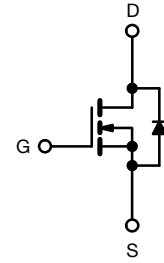
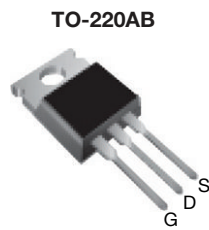


N-Channel 60 V(D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.072
Q_g max. (nC)	25	
Q_{gs} (nC)	5.8	
Q_{gd} (nC)	11	
Configuration	Single	

FEATURES

- Dynamic dV/dt rating
 - Fast switching
 - Ease of paralleling
- Simple drive requirements



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	60	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	20	A
		T _C = 100 °C		12	
Pulsed Drain Current ^a			I _{DM}	68	
Linear Derating Factor				0.40	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	100	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	60	W
Peak Diode Recovery dV/dt ^c			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^d	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 403\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 17\text{ A}$ (see fig. 12).
c. $I_{SD} \leq 17\text{ A}$, $dI/dt \leq 140\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.
d. 1.6 mm from case.

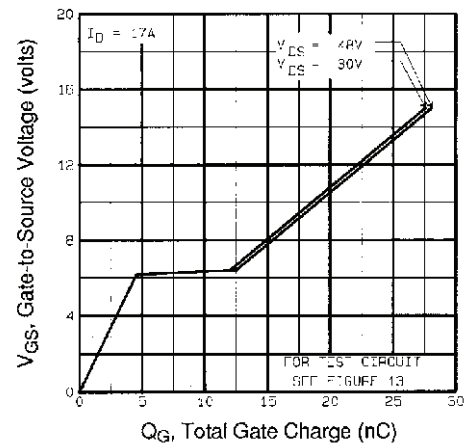
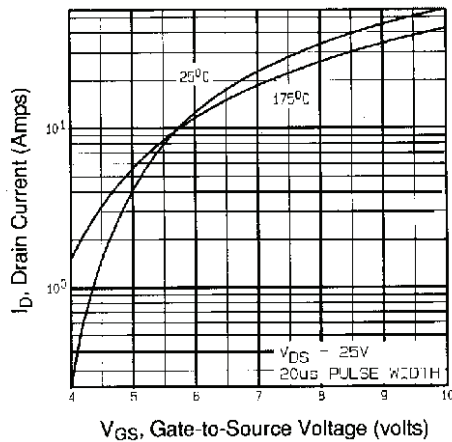
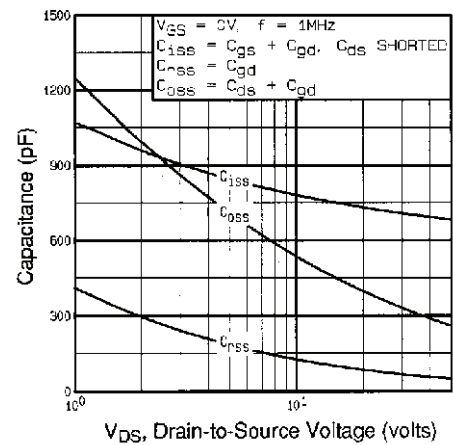
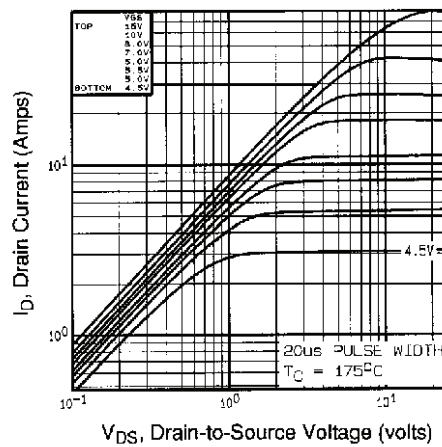
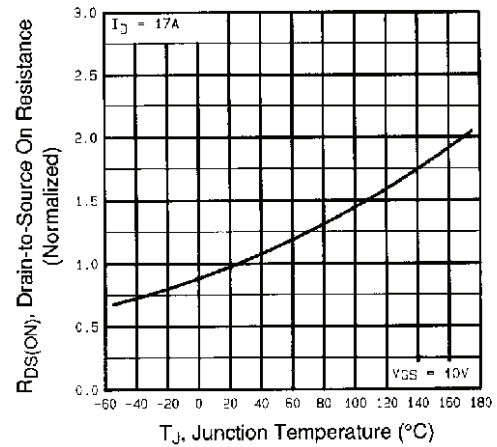
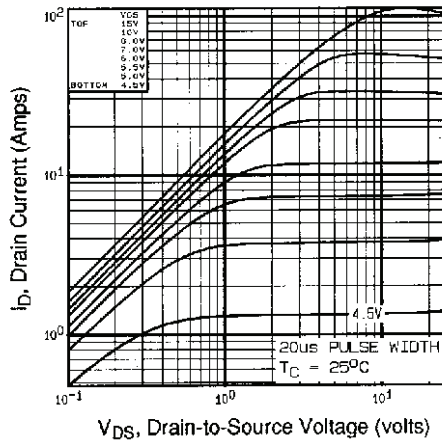
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.061	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	3.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A ^b	-	0.072	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 25 V, I _D = 10 A		5.5	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	640	-	pF
Output Capacitance	C _{oss}			-	360	-	
Reverse Transfer Capacitance	C _{rss}			-	79	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 17 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	25	nC
Gate-Source Charge	Q _{gs}			-	-	5.8	
Gate-Drain Charge	Q _{gd}			-	-	11	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 17 A, R _g = 18 Ω, R _D = 1.7 Ω, see fig. 10 ^b		-	13	-	ns
Rise Time	t _r			-	58	-	
Turn-Off Delay Time	t _{d(off)}			-	25	-	
Fall Time	t _f			-	42	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	68	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 17 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 17 A, dI/dt = 100 A/μs		-	88	180	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.29	0.64	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



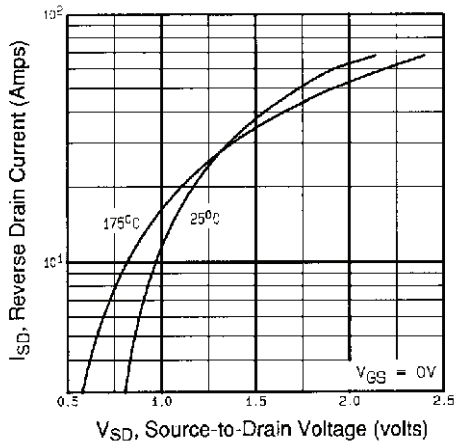


Fig. 7 - Typical Source-Drain Diode Forward Voltage

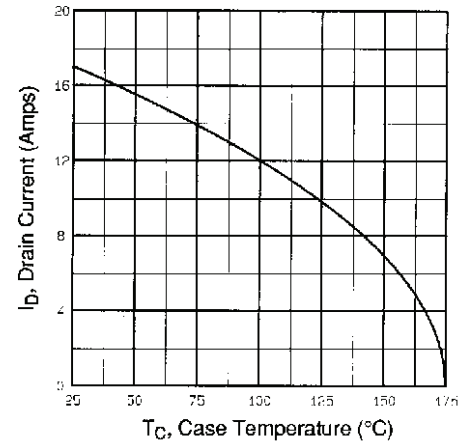


Fig. 9 - Maximum Drain Current vs. Case Temperature

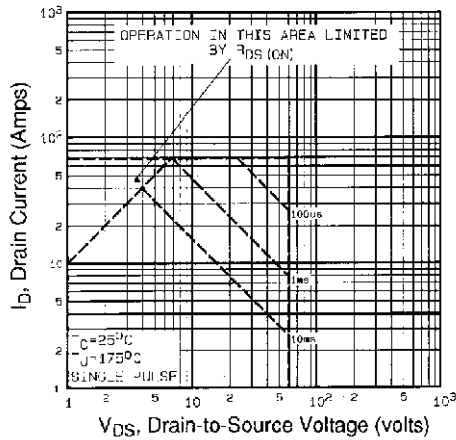


Fig. 8 - Maximum Safe Operating Area

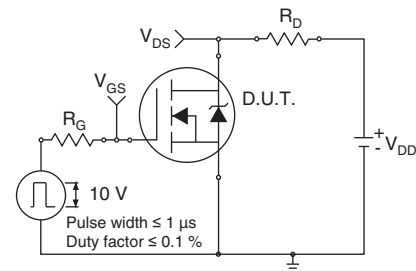


Fig. 10a - Switching Time Test Circuit

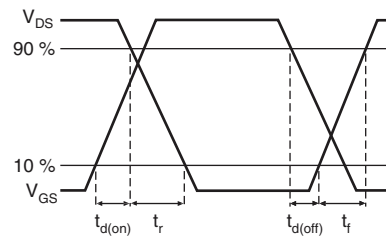


Fig. 10b - Switching Time Waveforms

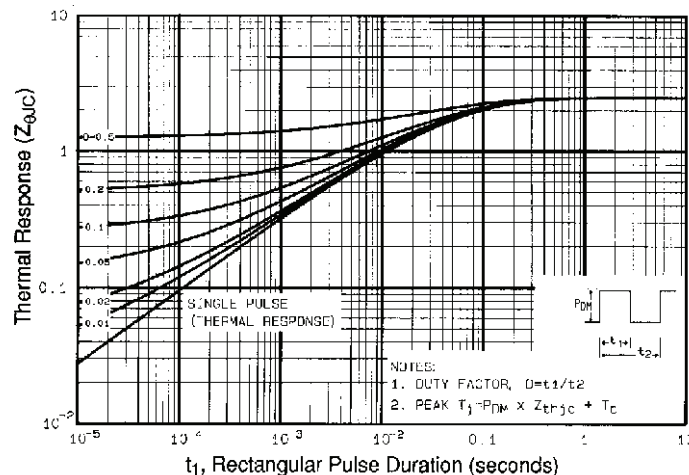


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

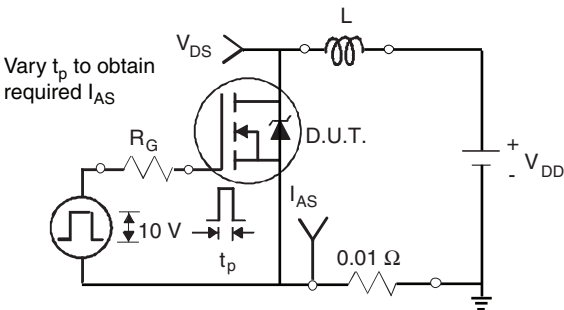


Fig. 12a - Unclamped Inductive Test Circuit

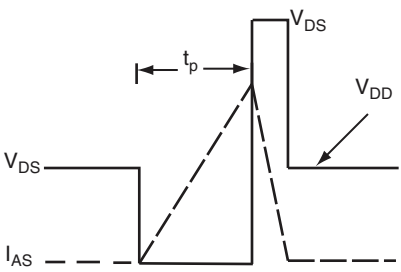


Fig. 12b - Unclamped Inductive Waveforms

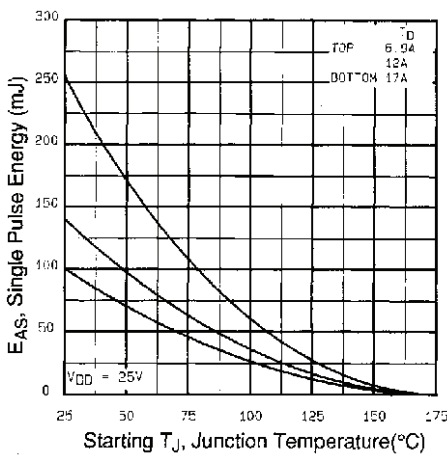


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

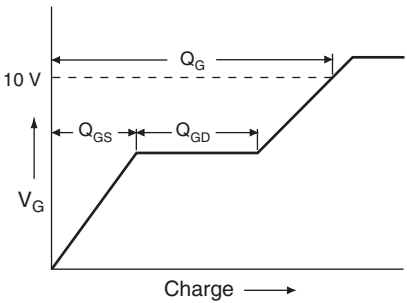


Fig. 13a - Basic Gate Charge Waveform

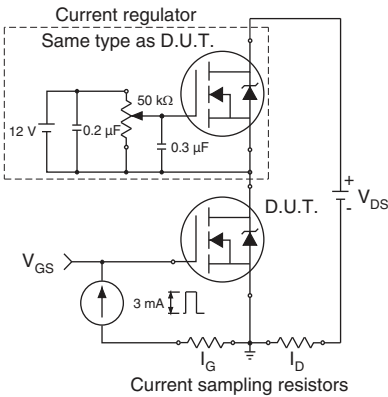
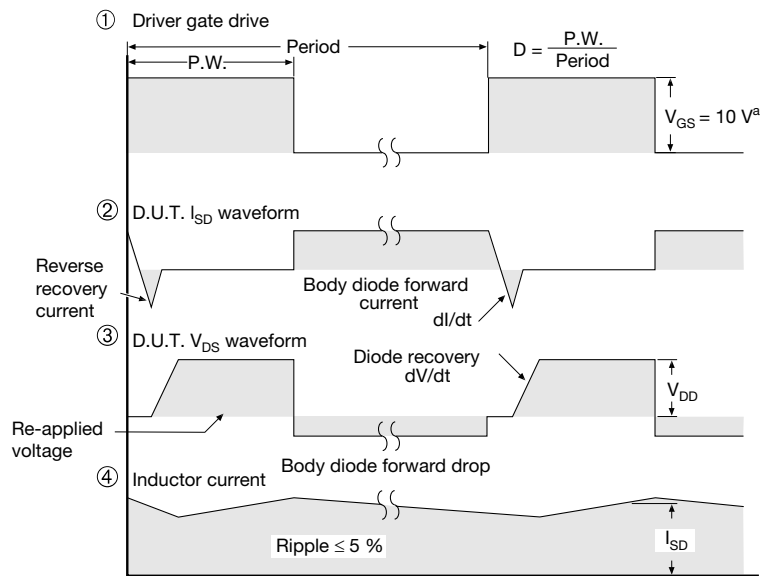
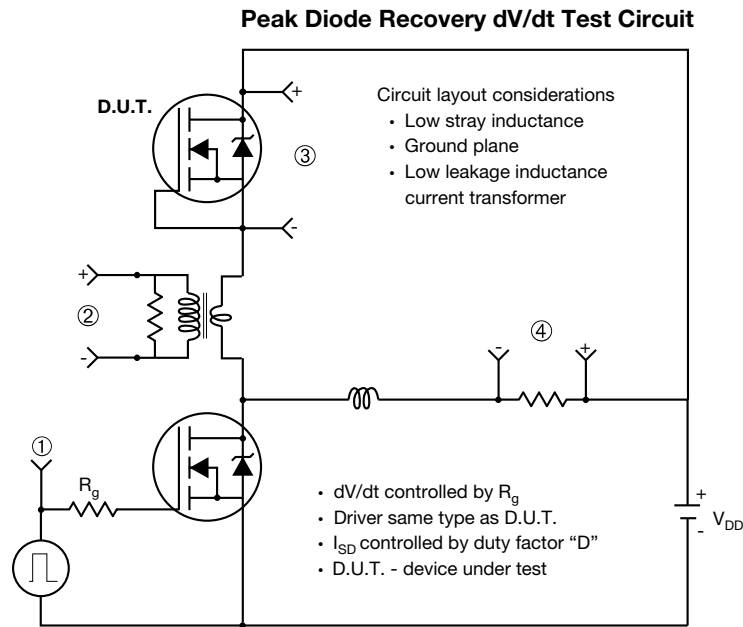


Fig. 13b - Gate Charge Test

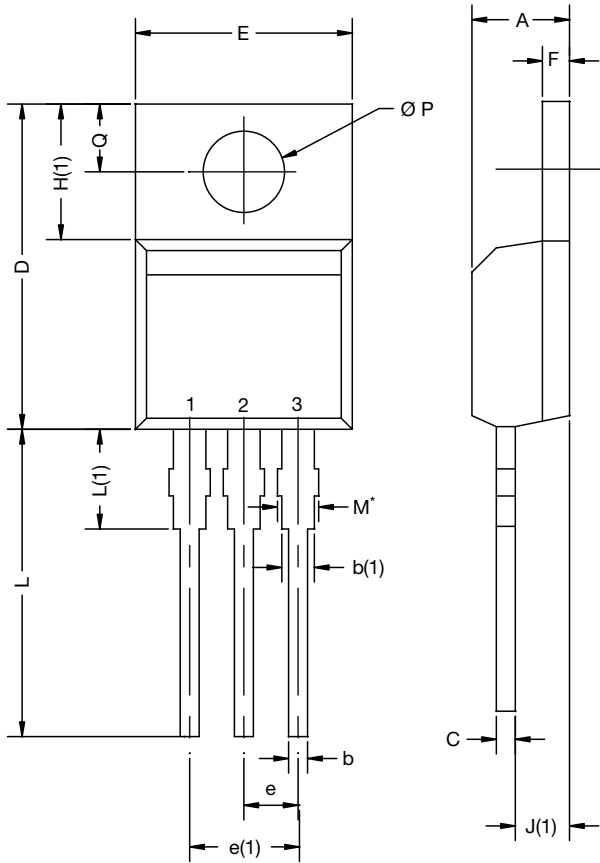


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-220



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

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