

- Slave Speech Synthesizers, LPC, MELP, CELP
- Two Channel FM Synthesis, PCM
- 8-Bit Microprocessor With 61 instructions
- 3.3V to 6.5V CMOS Technology for Low Power Dissipation
- Direct Speaker Drive Capability
- Internal Clock Generator That Requires No External Components
- Two Software-Selectable Clock Speeds
- 10-kHz or 8-kHz Speech Sample Rate

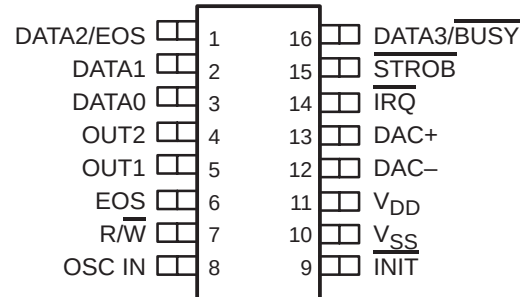
description

The MSP53C391 and MSP53C392 are catalog MSP50C3x codes which implements the functionality of a slave speech synthesizer. They communicate with a master microprocessor using two control lines ($\overline{R/W}$ and $\overline{STROBE}$) and either a 4-bit data bus (MSP53C391) or an 8-bit data bus (MSP53C392).

Either the MSP53C391 or the MSP53C392 can synthesize speech using several different compression algorithms; LPC, MELP, or CELP. They also can synthesize two-channel music using FM synthesis.

See the MSP50C3x User's Guide (literature number: SLOU006B) for more information about the MSP50C3x family.

**MSP53C391
N PACKAGE
(TOP VIEW)**



**MSP53C392
N PACKAGE
(TOP VIEW)**

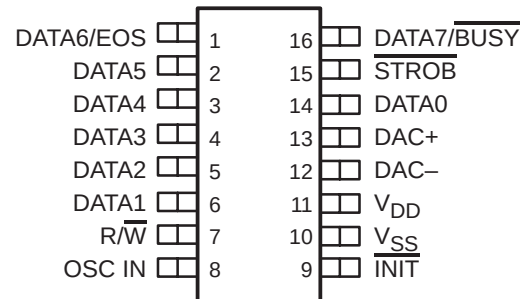


Table 1. MSP53C39x Family

DEVICE	FEATURES
MSP53C391	4-bit data bus
MSP53C392	8-bit data bus



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MSP53C391, MSP53C392 SLAVE SPEECH SYNTHESIZERS

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{DD} (see Note 1)	–0.3 V to 8 V
Supply current, I_{DD} or I_{SS} (see Note 2)	100 mA
Input voltage range, V_I (see Note 1)	–0.3 V to $V_{DD} + 0.3$ V
Output voltage range, V_O (see Note 1)	–0.3 V to $V_{DD} + 0.3$ V
Storage temperature range	–30°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground.
2. The total supply current includes the current out of all the I/O terminals and DAC terminals as well as the operating current of the device.

recommended operating conditions

			MAX	MAX	UNIT
V _{DD}	Supply voltage†		3.3	6.5	V
V _{IH}	High-level input voltage	V _{DD} = 3.3 V	2.5	3.3	V
		V _{DD} = 5 V	3.8	5	
		V _{DD} = 6 V	4.5	6	
V _{IL}	Low-level input voltage	V _{DD} = 3.3 V	0	0.65	V
		V _{DD} = 5 V	0	1	
		V _{DD} = 6 V	0	1.3	
T _A	Operating free-air temperature	Device functionality	0	70	°C
R _{speaker}	Minimum speaker impedance	Direct speaker drive using 2 pin push-pull DAC option	32		Ω

† Unless otherwise noted, all voltages are with respect to V_{SS} .

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going threshold voltage (INIT)	$V_{DD} = 3.5 \text{ V}$		2		V
		$V_{DD} = 6 \text{ V}$		3.4		
V_{T-}	Negative-going threshold voltage (INIT)	$V_{DD} = 3.5 \text{ V}$		1.6		V
		$V_{DD} = 6 \text{ V}$		2.3		
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$) (INIT)	$V_{DD} = 3.5 \text{ V}$		0.4		V
		$V_{DD} = 6 \text{ V}$		1.1		
I_{lkg}	Input leakage current (except for OSC IN)				2	μA
$I_{standby}$	Standby current ($\overline{\text{INIT}}$ low, SETOFF)				10	μA
$I_{DD}^{\dagger}$	Supply current	$V_{DD} = 3.3 \text{ V}, V_{OH} = 2.75 \text{ V}$		2.1		mA
		$V_{DD} = 5 \text{ V}, V_{OH} = 4.5 \text{ V}$		3.1		
		$V_{DD} = 6 \text{ V}, V_{OH} = 5.5 \text{ V}$		4.5		
I_{OH}	High-level output current (DATA0 – DATA7, OUT1, OUT2)	$V_{DD} = 3.3 \text{ V}, V_{OH} = 2.75 \text{ V}$	–4	–12		mA
		$V_{DD} = 5 \text{ V}, V_{OH} = 4.5 \text{ V}$	–5	–14		
		$V_{DD} = 6 \text{ V}, V_{OH} = 5.5 \text{ V}$	–6	–15		
		$V_{DD} = 3.3 \text{ V}, V_{OH} = 2.2 \text{ V}$	–8	–20		mA
		$V_{DD} = 5 \text{ V}, V_{OH} = 3.33 \text{ V}$	–14	–40		
		$V_{DD} = 6 \text{ V}, V_{OH} = 4 \text{ V}$	–20	–51		
I_{OL}	Low-level output current (DATA0 – DATA7, OUT1, OUT2)	$V_{DD} = 3.3 \text{ V}, V_{OL} = 0.5 \text{ V}$	5	9		mA
		$V_{DD} = 5 \text{ V}, V_{OL} = 0.5 \text{ V}$	5	9		
		$V_{DD} = 6 \text{ V}, V_{OL} = 0.5 \text{ V}$	5	9		
		$V_{DD} = 3.3 \text{ V}, V_{OL} = 1.1 \text{ V}$	10	19		mA
		$V_{DD} = 5 \text{ V}, V_{OL} = 1.67 \text{ V}$	20	29		
		$V_{DD} = 6 \text{ V}, V_{OL} = 2 \text{ V}$	25	35		
I_{OH}	High-level output current (DAC)	$V_{DD} = 3.3 \text{ V}, V_{OH} = 2.75 \text{ V}$	–30	–50		mA
		$V_{DD} = 5 \text{ V}, V_{OH} = 4.5 \text{ V}$	–35	–60		
		$V_{DD} = 6 \text{ V}, V_{OH} = 5.5 \text{ V}$	–40	–65		
		$V_{DD} = 3.3 \text{ V}, V_{OH} = 2.3 \text{ V}$	–50	–90		mA
		$V_{DD} = 5 \text{ V}, V_{OH} = 4 \text{ V}$	–90	–140		
		$V_{DD} = 6 \text{ V}, V_{OH} = 5 \text{ V}$	–100	–150		
I_{OL}	Low-level output current (DAC)	$V_{DD} = 3.3 \text{ V}, V_{OL} = 0.5 \text{ V}$	50	80		mA
		$V_{DD} = 5 \text{ V}, V_{OL} = 0.5 \text{ V}$	70	90		
		$V_{DD} = 6 \text{ V}, V_{OL} = 0.5 \text{ V}$	80	110		
		$V_{DD} = 3.3 \text{ V}, V_{OL} = 1 \text{ V}$	100	140		mA
		$V_{DD} = 5 \text{ V}, V_{OL} = 1 \text{ V}$	140			
		$V_{DD} = 6 \text{ V}, V_{OL} = 1 \text{ V}$	150			
$f_{osc(low)}$	Oscillator frequency [‡]	$V_{DD} = 5 \text{ V}, T_A = 25^{\circ}\text{C},$ Target frequency = 15.36 MHz	14.89	15.36	15.86	MHz
$f_{osc(high)}$	Oscillator frequency [‡]	$V_{DD} = 5 \text{ V}, T_A = 25^{\circ}\text{C},$ Target frequency = 19.2 MHz	18.62	19.2	19.7	MHz

[†] Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

[‡] The frequency of the internal clock has a temperature coefficient of approximately $-0.2 \text{ \%}/^{\circ}\text{C}$ and a V_{DD} coefficient of approximately $\pm 1\%/V$.

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switching characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_r Rise time, DATA0 – DATA7, DAC	$V_{DD} = 3.3\text{ V}$, $C_L = 100\text{ pF}$, 10% to 90%		50		ns
t_f Fall time, DATA0– DATA7, DAC	$V_{DD} = 3.3\text{ V}$, $C_L = 100\text{ pF}$, 10% to 90%		50		ns

timing requirements

	MIN	MAX	UNIT
Initialization			
t_{INIT} $\overline{INIT}$ pulsed low while the MSP53C39x has power applied (see Figure 1)	1		μs
t_{SETUP} Delay between rising edge of $\overline{INIT}$ and device initialization complete	5		ms
Writing (Slave Mode)			
$t_{su1(R/W)}$ Setup time, $R/\overline{W}$ low before $\overline{STROB}$ goes low (see Figure 2)	20		ns
$t_{su(d)}$ Setup time, data valid before $\overline{STROB}$ goes high (see Figure 2)	100		ns
$t_{h1(R/W)}$ Hold time, $R/\overline{W}$ low after $\overline{STROB}$ goes high (see Figure 2)	20		ns
$t_{h(d)}$ Hold time, data valid after $\overline{STROB}$ goes high (see Figure 2)	30		ns
t_W Pulse duration, $\overline{STROB}$ low (see Figure 2)	100		ns
t_r Rise time, $\overline{STROB}$ (see Figure 2)		50	ns
t_f Fall time, $\overline{STROB}$ (see Figure 2)		50	ns
Reading (Slave Mode)			
$t_{su2(R/W)}$ Setup time, $R/\overline{W}$ before $\overline{STROB}$ goes low (see Figure 3)	20		ns
$t_{h2(R/W)}$ Hold time, $R/\overline{W}$ after $\overline{STROB}$ goes high (see Figure 3)	20		ns
t_{dis} Output disable time, data valid after $\overline{STROB}$ goes high (see Figure 3)	0	30	ns
t_W Pulse duration, $\overline{STROB}$ low (see Figure 3)	100		ns
t_r Rise time, $\overline{STROB}$ (see Figure 3)		50	ns
t_f Fall time, $\overline{STROB}$ (see Figure 3)		50	ns
t_d Delay time for $\overline{STROB}$ low to data valid (see Figure 3)		50	ns

PARAMETER MEASUREMENT INFORMATION

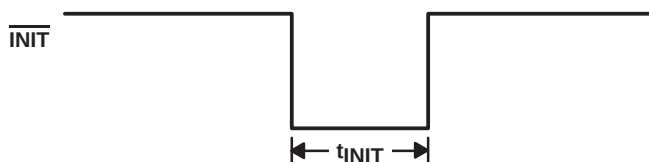


Figure 1. Initialization Timing Diagram

PARAMETER MEASUREMENT INFORMATION

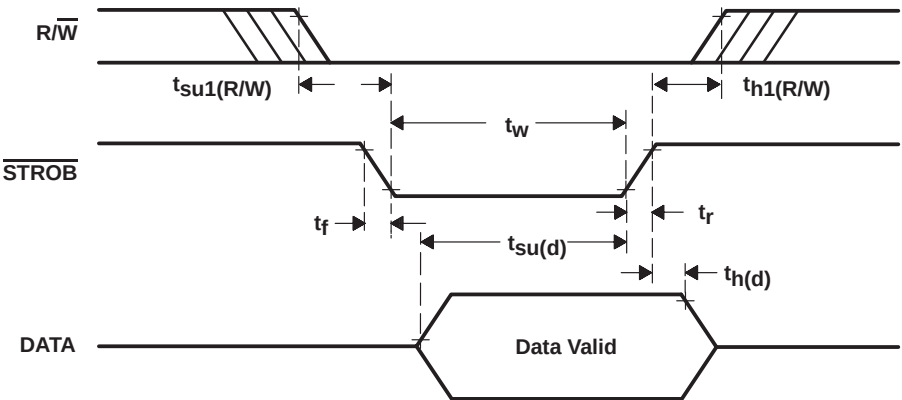


Figure 2. Write Timing Diagram (Slave Mode)

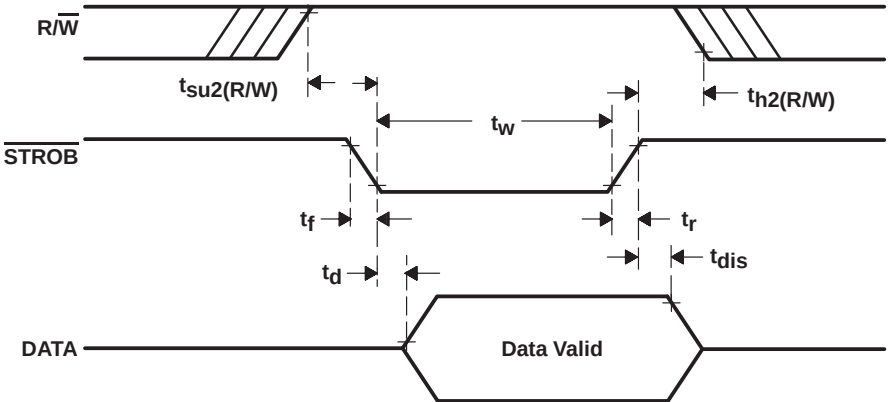


Figure 3. Read Timing Diagram (Slave Mode)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MSP53C391NI2D	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
MSP53C392DWI2D	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
MSP53C392NI2D	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

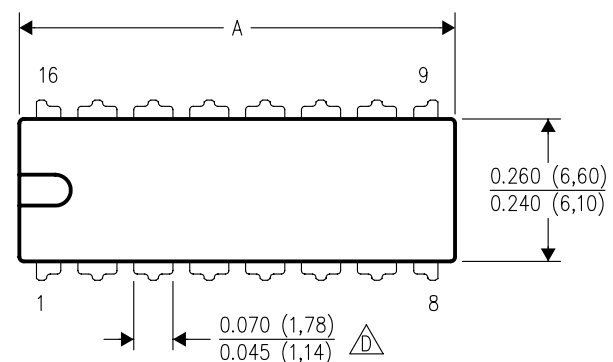
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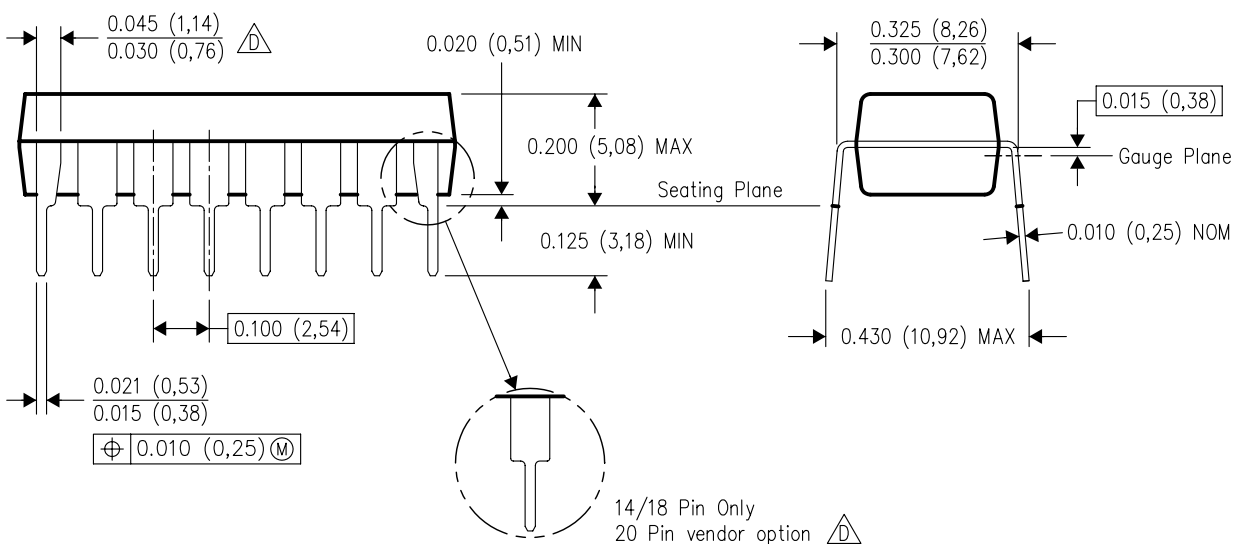
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

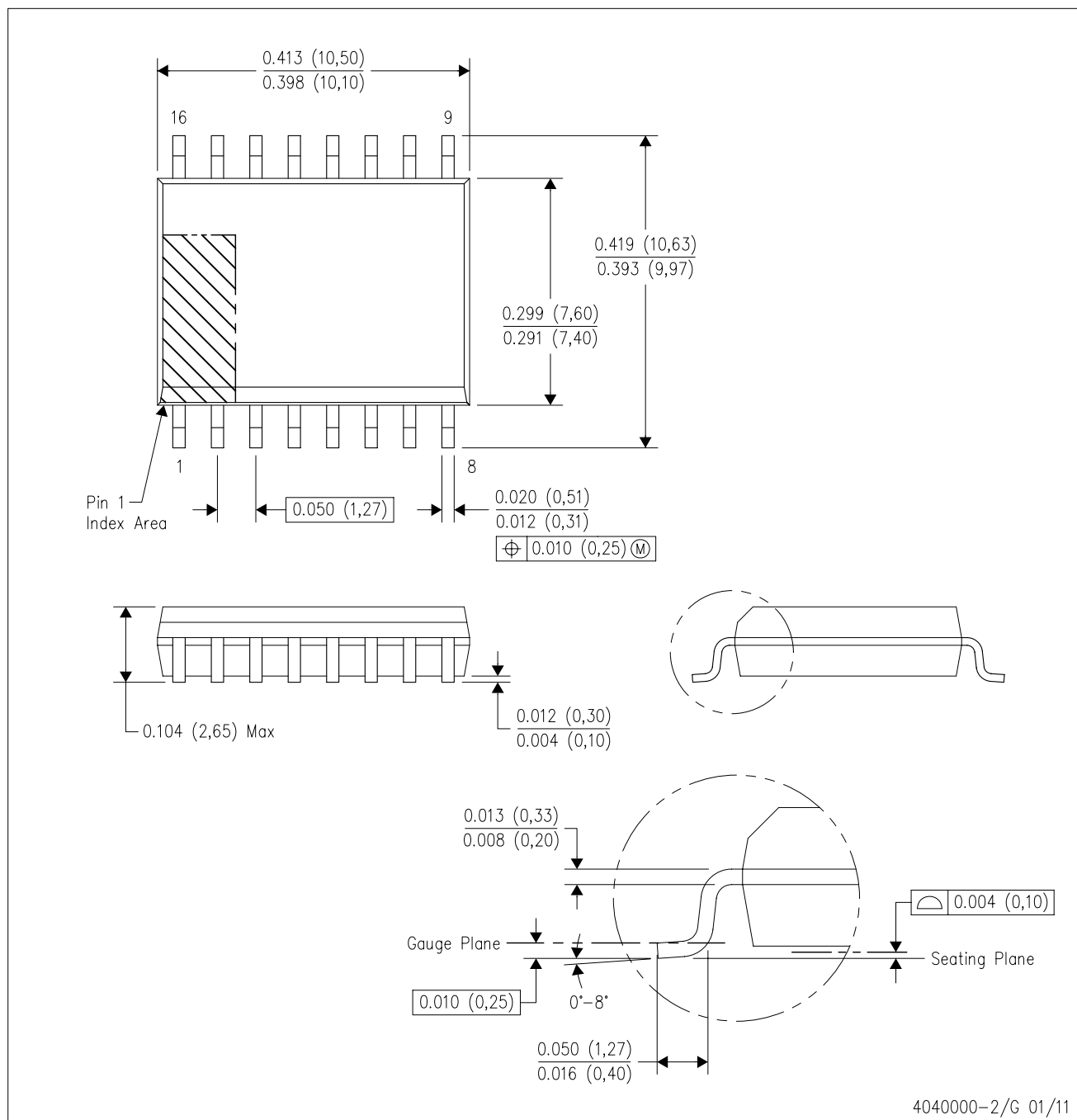


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



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