Descriptions

FSA4480UCX is a high performance USB Type-C switch combo of High-Speed Data, Hi-Fi Audio and Side Band Use (SBU). The Audio path is capable of wide audio swing and results in ultra-low distortion. With excellent THD+N performance and wide frequency response, FSA4480UCX is an ideal device for Hi-Fi system application. The USB path of wide bandwidth has very low bit-to-bit skew and channel-to-channel cross-talk, and it is compatible with high-speed USB 2.0 eye diagram and maintains good signal integrity.

The Side Band Use (SBU) configures internal switches to Ground and MIC connections on headset. GND sense path supports quasi-differential amplifier architectures, which reduces cross-talk and improves sound quality. SBU ports can also be configured to deliver eDP AUX signal.

FSA4480UCX incorporates High Voltage Protection (OVP) to both SBU and USB ports on Type-C receptacle side. Both GPIO and I2C controls are 1.8V logic compatible. 25-Ball Wafer Level Chip Scale Package (WLCSP) 2.04mm x 2.04mm with Pb-free and Halogen-free, makes it ideal for mobile device.

Features

- Wide VCC Supply Range (2.5v~25v) can be powered by either LDO or VBUS
- USB Path Insertion loss: -1dB@430MHz, -2dB@930MHz, -3dB@1.4GHz
- Hi-Fi Audio Path: THD+N=-110dB, 0.707Vrms, f=100Hz, 32Ω Load,
- Audio Path Insertion loss: -1dB@500MHz, -2dB@860MHz, -3dB@1.2GHz
- In-Built OVP to both DC 16V-tolerant SBUx/GSBUx ports and DC 17V-tolerant DP_R/DN_L ports on Type-C receptacle
- IEC 64000-4-5 Surge Protection w/o External TVS: DP_R/DN_L ports 20V, SBUx/GSBUx ports: 80V
- OMTP and CTIA Pinout Support and Audio Sense Path for Quasi Differential Configuration
- Audio Path Soft Turn-On/Off for Pop & Click Elimination
- Power-off Truly Isolated and Noise Removal
- Configurable to Deliver eDP AUX Signal

Applications

- USB Type-C Receptacle, 4G/5G Smart Phone, Mobile and AI Device

Order Information

Part Number	Package	
FSA4480UCX	CSP-25	Tape and Reel

Functional Diagram

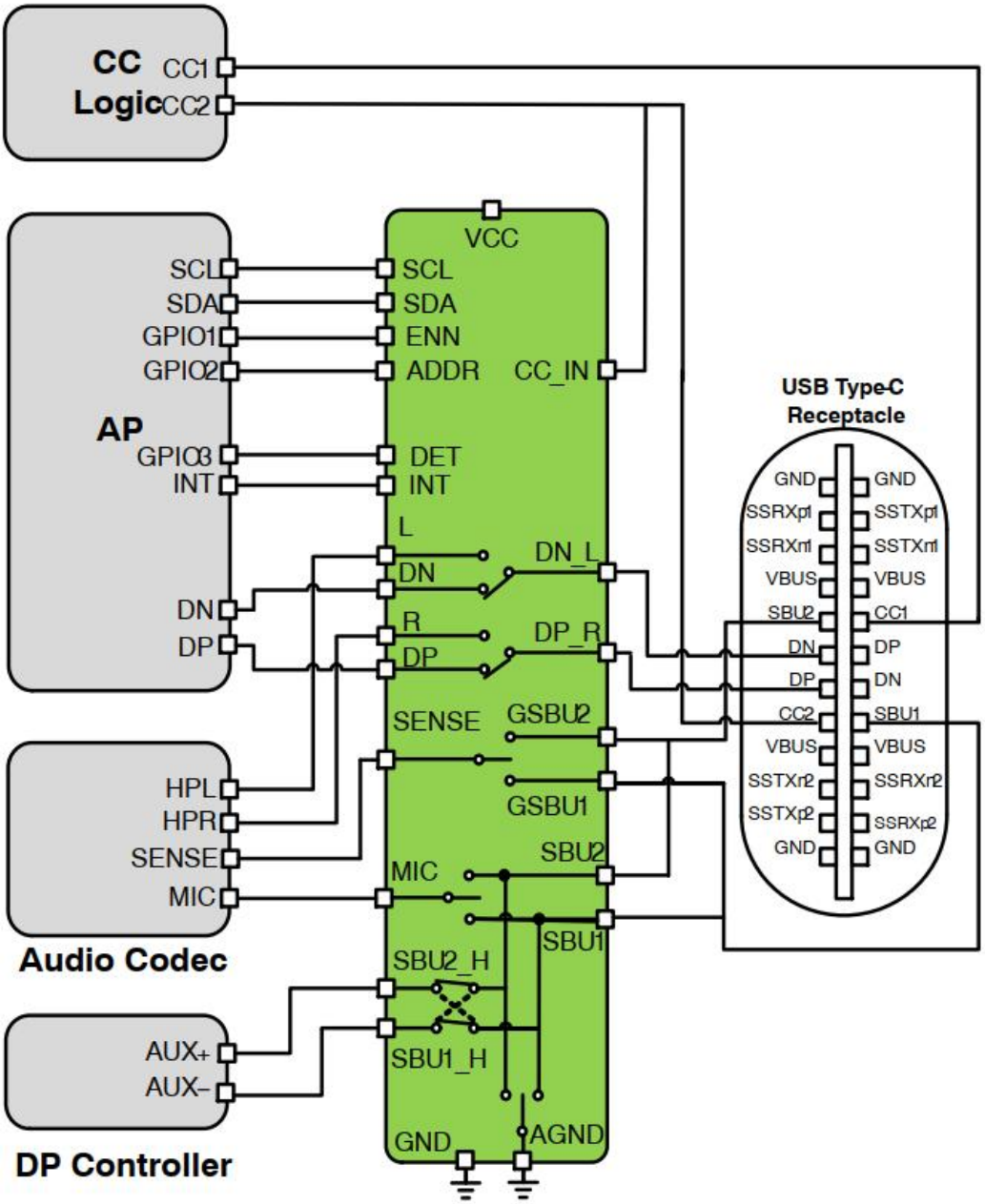


Fig.1 Functional Diagram

Pin Configuration

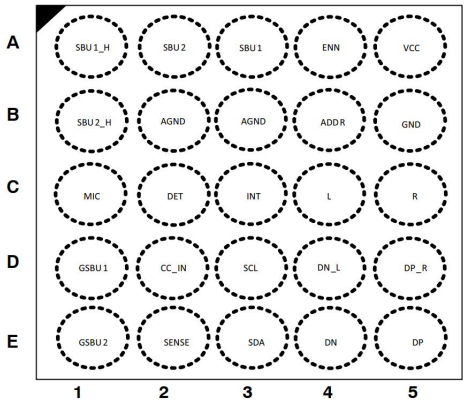
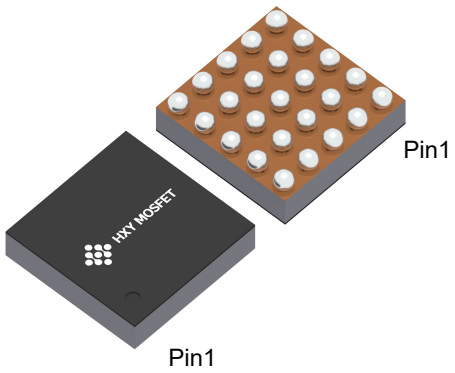


Fig.2 Top-Through



CSP-25

Pin Descriptions

Pin #	Name	Type	Description
A5	VCC	PWR	2.5~25V Positive Supply
B5	GND	GND	Primary Ground Connection. Must be Connected to System Ground
D5	DP_R	I/O	Right Audio / Positive USB2.0 Data Common Line
D4	DN_L	I/O	Left Audio / Negative USB2.0 Data Common Line
E5	DP	I/O	Positive USB2.0 Data Line
E4	DN	I/O	Negative USB2.0 Data Line
C5	R	I/O	Right Line for Audio Signals
C4	L	I/O	Left Line for Audio Signals
A3	SBU1	I/O	Sideband Use wire 1
A2	SBU2	I/O	Sideband Use wire 2
C1	MIC	O	Analog Audio Microphone
B2	AGND2	GND	Analog Ground 2
B3	AGND1	GND	Analog Ground 1
E2	SENSE	O	Analog Ground Sense Return
C3	INT	O	Open Drain Interrupt Output
D2	CC_IN	I	Audio Accessory Attachment Detection Input
D1	GSBU1	I/O	Star-connection with SBU1 to Headset Jack as Audio Ground Sense Path 1
E1	GSBU2	I/O	Star-connection with SBU2 to Headset Jack as Audio Ground Sense Path 2
C2	DET	O	Push-pull output. DET changes status in response to CC_IN voltage level.
D3	SCL	I	I2C Clock wire
E3	SDA	I/O	I2C Data wire
B1	SBU2_H	I	System Side Sideband Use wire 2, can be configured as eDP AUX path
A1	SBU1_H	I	System Side Sideband Use wire 1, can be configured as eDP AUX path
A4	ENN	I	Chip Enable, Active Low, Internal Pull-Down by 470KΩ
B4	ADDR	I	I2C Slave Address

Table-1 Pin Descriptions

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1)

		Range	Unit
Power Supply Voltage	VCC	-0.5 ~ 25	V
Control Pins	SCL, SDA, ADDR, ENN, INT_N	-0.5 ~ 6.5	V
	CC_IN	-0.5 ~ 25	V
Signal Pins	DP_R, DN_L	-3.3 ~ 17	V
	L, R, DP, DN, MIC, SENSE, SBU1_H, SBU2_H	-0.3 ~ 6.5	V
	SBU1, GSBU1, SBU2, GSBU2	-0.3 ~ 16	V
Storage Temperature Range	TSTG	-55 ~ 150	°C
ESD HBM, ANSI/ ESDA/JEDEC JS-001-2012	VCC	±8	kV
	SCL, SDA, ADDR, ENN, INT_N	±8	kV
	CC_IN	±8	kV
	DP_R, DN_L	±8	kV
	L, R, DP, DN, MIC, SENSE, SBU1_H, SBU2_H	±8	kV
	SBU1, GSBU1, SBU2, GSBU2	±8	kV
ESD MM, JESD22-A115	VCC	±400	V
	SCL, SDA, ADDR, ENN, INT_N	±400	V
	CC_IN	±400	V
	DP_R, DN_L	±300	V
	L, R, DP, DN, MIC, SENSE, SBU1_H, SBU2_H	±400	V
	SBU1, GSBU1, SBU2, GSBU2	±800	V
ESD CDM, JESD22-C101	All Pins	±1500	V

Table-2 Absolute Maximum Ratings

(1) Stresses beyond those listed in Table-2 *Absolute Maximum Ratings* may cause permanent damage to the device. They are stress ratings only, which do not imply functional operation of the device at these or any other conditions. Beyond those indicated under *Recommended Operating Conditions*, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommend Operating Conditions

		Range	Unit
Power Supply Voltage	VCC	2.7 ~ 20	V
Control Pins	SCL, SDA, ADDR, ENN, INT_N	0 ~ 5.0	V
	CC_IN	0 ~ 20	V
Signal Pins	L, R, DP_R, DN_L	-3.6 ~ 5.0	V
	DP, DN, MIC, SENSE, SBU1_H, SBU2_H	0 ~ 5.0	V
	SBU1, GSBU1, SBU2, GSBU2	0 ~ 3.6	V
Operating Temperature	T_A	-40 ~ 85	°C

Table-3 Recommend Operating Conditions

(1) In USB mode, any signal applied to the off−state audio inputs R, L may not swing below ground or above 1V

Electrical Characteristics (Ta=25°C, VCC=3.3V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
Under Voltage Lock Out (UVLO)	V_{UVLO}		2.2	2.4	2.6	V
UVLO Hysteresis	$V_{UVLO-HYS}$		150	200	250	mV
VCC Quiescent Current	I_Q	ENN=H, All switches off		180		uA
		USB switches on		180		uA
		Audio switches on along with MIC and SENSE		270		uA
Digital I/O		switches on				
Input logic high	V_{IH}	VCC=3.3~20V	1.6		5.5	V
Input logic low	V_{IL}	VCC=3.3~20V	-0.1		0.5	V
INT Internal pull-up resistor	R_{UP-INT}			2		MΩ
CC_IN Internal pull-up resistor	R_{UP-CC}			2		MΩ
SCL, SDA Internal pull-up resistor	R_{UP-I2C}			2		MΩ
ADDR Internal pull-down resistor	$R_{DN-ADDR}$			2		MΩ
ENN Internal pull-down resistor	R_{DN-ENN}			470		kΩ
Audio Switch On Resistance						
On-Resistance	R_{AUDIO}	V_{IS}= -3.3V~+3.3V I_{OUT}=30mA		1.3		Ω
R_{ON} Flatness(1)	$R_{FLAT(A)}$	V_{IS}= -3.3V~+3.3V I_{OUT}=30mA		0.01		Ω
R_{ON} Matching Between Channels(2)	$\Delta R_{ON(A)}$	V_{IS}= -3.3V~+3.3V I_{OUT}=30mA		0.02		Ω
Audio Switch Dynamics						
Total Harmonic Distortion	$THD+N_1$	f=20Hz to 22KHz, A-weighted V_{IS}=1Vrms @R_L=1kΩ		-106		dB
		f=20Hz to 22kHz, A-weighted V_{IS}=0.7Vrms @RL=32Ω	-110	-103		dB
Signal-to-Noise Ratio	SNR_1	f=20Hz to 22KHz, Inputs grounded @R_L=32Ω		>120		dBrA
Audio Switches OFF Isolation	OIRR	f=20Hz to 22KHz, V_L= V_R = 0.3Vrms @R_L=32Ω		-91		dB
Audio Switches Crosstalk (3) (Channel-to-Channel)	ACRX	f=20Hz to 22KHz, $V_{L\ or\ R}$ = 0.3Vrms @R_L=32Ω Source Impedance=0Ω R_L =1kΩ		-115		dB
Audio Switch -3dB Bandwidth	BW_{Audio}	R_L=50Ω		1.2		GHz
AUDIO Switch Turn-on Time	t_{ON-A}	V_{IS}= 50mV R_L=32Ω		60		mS
AUDIO Switch Turn-off Time	t_{OFF-A}	V_{IS}= 50mV R_L=32Ω		5		mS
USB Switch On Resistance						
On-Resistance	R_{USB}	V_{IS} = 0V~0.4V, I_{ON} = 8mA		3.5		Ω
R_{ON} Flatness	$R_{FLAT(U)}$	V_{IS} = 0V~3.3V, I_{ON} = 8mA		4.8		Ω
R_{ON} Matching Between Channels	$\Delta R_{ON(U)}$	V_{IS} = 0V~0.4V, I_{ON} = 8mA		0.2		Ω
USB Switch Dynamics						
USB Switch On Capacitance	C_{ON}	V_{Bias} = 0.2V, f = 1MHz		4		pF
USB Switch Off Capacitance	C_{OFF}	V_{Bias} = 0.2V, f = 1MHz		3		pF

USB Switch Off Isolation	Off_{USB}	f = 100MHz, R_T = 50Ω, C_L = 0pF		-46		dB
USB Switches Crosstalk (Channel-to-Channel)	CRX_{USB}	f = 100MHz, R_T = 50Ω, C_L = 0pF		-47		dB
USB Switch -3dB Bandwidth	BW_{USB}	R_T=50Ω, C_L=0pF Signal Power 0dBm		1.4		GHz
DP_R, DN_L Ports Over-Voltage Protection						
OVP Lockout Threshold	$V_{COM-OVP}$	Rising Edge	4.6	4.8	5.0	V
OVP Hysteresis	$V_{COM-HYS}$			400		mV
GSBU1, GSBU2 Over-Voltage Protection						
OVP Lockout Threshold	$V_{SBU-OVP}$	Rising Edge	4.6	4.8	5.0	V
OVP Hysteresis	$V_{SBU-HYS}$			400		mV
Audio Ground Switches ON RESISTANCE						
AGND-to-SBUx On-Resistance	R_{AGND}	I_{AGND} = 100 mA		60		mΩ
MIC Switch						
MIC Switch On-Resistance	R_{MIC}	V_{IS} = 0V~2.0V, I_{ON} = 10mA		2.1		Ω
MIC Switch RON Flatness	$R_{FLAT(MIC)}$	V_{IS} = 0V~2.0V, I_{ON} = 10mA		1		Ω
MIC Switch -3dB Bandwidth	BW_{MIC}	R_L=50Ω, GSBUx ties to SBUx		24		MHz
MIC Switch Off Isolation	Off_{MIC}	f = 100MHz, R_T = 50Ω		-48		dB
MIC Switch Turn-on Time	t_{ON-M}	GSBUx = 2.0V R_L=1kΩ		200		uS
MIC Switch Turn-off Time	t_{OFF-M}	GSBUx = 2.0V R_L=1kΩ		2		uS
SENSE Switch						
SENSE Switch On-Resistance	R_{SENSE}	V_{IS} = 0V~50mV, I_{ON} = 10mA		0.4		Ω
SENSE Switch -3dB Bandwidth	BW_{SENSE}	R_L=50Ω, GSBUx ties to SBUx		21		MHz
SENSE Switch Off Isolation	Off_{SENSE}	f = 100MHz, R_T = 50Ω		-47		dB
SENSE Switch Turn-on Time	t_{ON-S}	GSBUx = 50mV R_L=1kΩ		200		uS
SENSE Switch Turn-off Time	t_{OFF-S}	GSBUx = 50mV R_L=1kΩ		2		uS
SBUx_H Switch						
SBUx_H Switch On-Resistance	R_{SBUx_H}	V_{IS} = 0V~0.4V, I_{ON} = 10mA		7		Ω
SBUx_H Switch RON Flatness	$R_{FLAT(SBU\_H)}$	V_{IS} = 0V~3.3V, I_{ON} = 10mA		2		Ω
SBUx_H Switch -3dB Bandwidth	BW_{SBU_H}	R_L=50Ω, GSBUx ties to SBUx		21		MHz
SBUx_H Switch Off Isolation	Off_{SBU_H}	f = 100MHz, R_T = 50Ω		-51		dB

Table-4 Electrical Characteristics

Note:

(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance

I2C Controlling:

FSA4480UCX switching functions are controlled by 2 I2C pins: SCL and SDA pin. The timing characteristics and diagrams, as well as internal register meaning and usage are listed below:

I2C Timing Diagrams

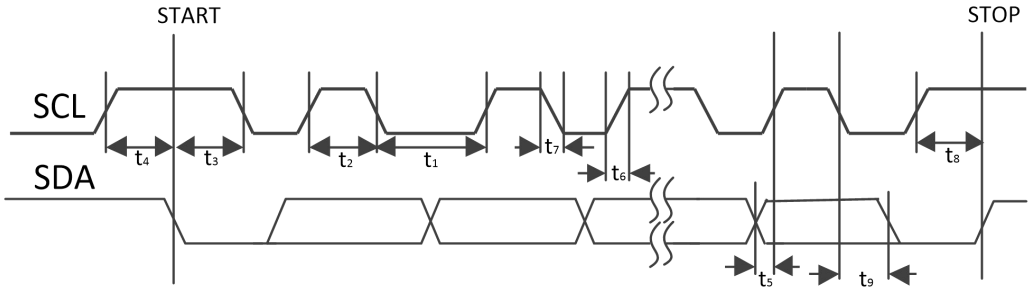


Fig.4 I2C Timing Diagrams

Note: Each of SDA and SCL pins should be pulled up by a 2.2kΩ resistor.

I2C Timing Characteristics

(Ta=25°C, VCC=3.3V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL Frequency	f_{CLK}				400	kHz
SCL Low Pulse-Width	t_1		1.3			us
SCL High Pulse-Width	t_2		0.6			us
Hold Time (Start Condition)	t_3		0.6			us
Setup Time (Start Condition)	t_4		0.6			us
Data setup time	t_5		0.1			us
SDA, SCL Rise Time	t_6				0.3	us
SDA, SCL Fall Time	t_7				0.3	us
Setup Time (Stop Condition)	t_8		0.6			us
Data Hold Time	t_9				0.9	us
Pulse Width of Spikes being Suppressed	t_{ps}				5	ns

Table-5 I2C Timing Characteristics

I2C Slave Address

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR=L	1	0	0	0	0	1	0	R/W
ADDR=H	1	0	0	0	0	1	1	R/W

Table-6 I2C Slave Address

Mode Register

Address: 0x01

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:3]	Reserved	5	Do Not Use
[2:0]	Switch Mode	3	000: DN_L to DN switch ON, DP_R to DP switch ON SBU1 to SBU1_H switch ON, SBU2 to SBU2_H switch ON
			001: DN_L to DN switch ON, DP_R to DP switch ON SBU1 to SBU2_H switch ON, SBU2 to SBU1_H switch ON
			010: DN_L to L switch ON, DP_R to R switch ON, AGND2 to SBU2 switch ON MIC to GSBU1 switch ON, SENSE to GSBU2 switch ON
			011: DN_L to L switch ON, DP_R to R switch ON,AGND1 to SBU1 switch ON MIC to GSBU2 switch ON, SENSE to GSBU1 switch ON
			100: All switches OFF
			101: All switches OFF
			110: All switches OFF
			111: AGND1 to SBU1 switch ON, AGND2 to SBU2 switch ON

Table-7 Mode Register

Manual and Interrupt Register

Address: 0x02

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:2]	Reserved	6	Do Not Use
1	Manual	1	0: Switch Status is controlled by Mode Register 0x01
			1: Switch Status is controlled by 3-bit GPIO (ENN, ADDR, INT)
0	INTC	1	0: Enable interrupt feature
			1: Disable interrupt feature

Table-8 Manual and Interrupt Register

DET Direction Register

Address: 0x03

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:1]	Reserved	7	Do Not Use
0	DET	1	0: DET goes high when CC_IN <1.2v , DET goes low when CC_IN >1.5v
			1: DET goes low when CC_IN <1.2v , DET goes high when CC_IN >1.5v

Table-9 DET Direction Register

DET Register

Address: 0x04

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:1]	Reserved	7	Do Not Use
0	DET	1	0: DET Direction is controlled by DET Direction Register 0x03
			1: DET remains high, independent of CC_IN

Table-10 DET Register

Manual Mode Control

The function is active during control Register 0x02 bit[1] = 1. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input

VCC	ENN	ADDR	INT	SENSE switch	USB switch	Audio switch	MIC/GND switch	SBU switch
OFF	X	X	X	OFF	OFF	OFF	SBU1 to AGND1 SBU2 to AGND2	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF
ON	L	L	L	OFF	DP_R to DP DN_L to DN	OFF	OFF	SBU1 to SBU1_H SBU2 to SBU2_H
ON	L	L	H	OFF	DP_R to DP DN_L to DN	OFF	OFF	SBU1 to SBU2_H SBU2 to SBU1_H
ON	L	H	L	SENSE to GSBU2	OFF	DP_R to R DN_L to L	MIC to GSBU1 SBU2 to AGND2	OFF
ON	L	H	H	SENSE to GSBU1	OFF	DP_R to R DN_L to L	MIC to GSBU2 SBU1 to AGND1	OFF
ON	H	L	L	OFF	OFF	OFF	OFF	OFF
ON	H	L	H	OFF	OFF	OFF	OFF	OFF
ON	H	H	L	OFF	OFF	OFF	OFF	OFF
ON	H	H	H	OFF	OFF	OFF	SBU1 to AGND1 SBU2 to AGND2	OFF

Table-11 Manual Mode Control

Typical Performance Curves (Ta=25°C, VCC=3.3V, CAP=0.1uF, unless otherwise noted)

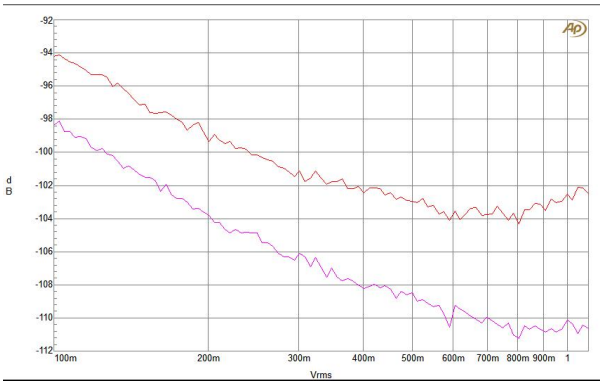


Fig.5 wi/wo A-Weighted Audio Switch THD+N vs Signal Swing @RL=32Ω f=100Hz

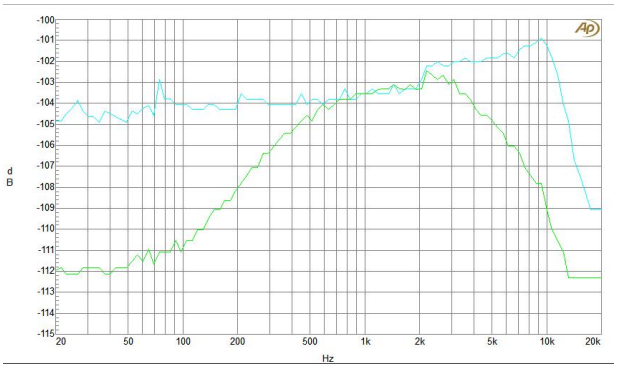


Fig.6 wi/wo A-Weighted Audio Switch THD+N vs Frequency @RL=32Ω Vs=0.7Vrms

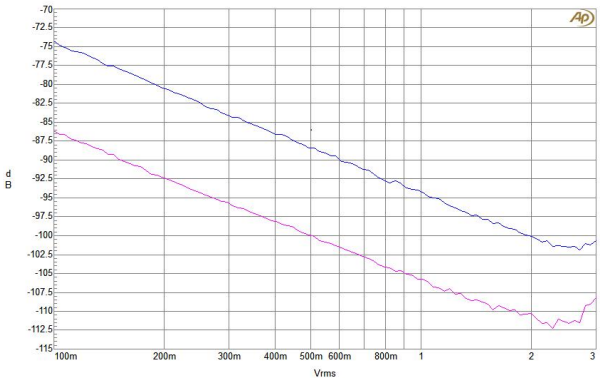


Fig.7 wi/wo A-Weighted Audio Switch THD+N vs Signal Swing @RL=1KΩ f=100Hz

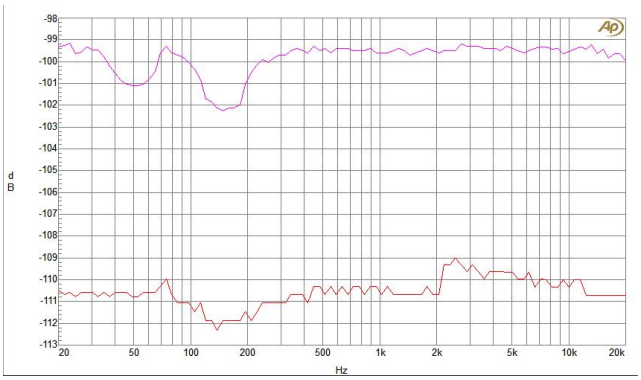


Fig.8 wi/wo A-Weighted Audio Switch THD+N vs Frequency @RL=1KΩ Vs=2.3Vrms

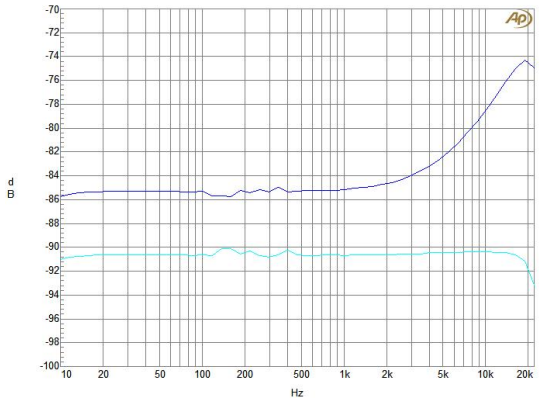


Fig.9 Audio Switch OFF-Isolation vs Frequency @RL=32Ω/1KΩ Vs=0.3Vrms

Fig.10 USB Switch Bandwidth

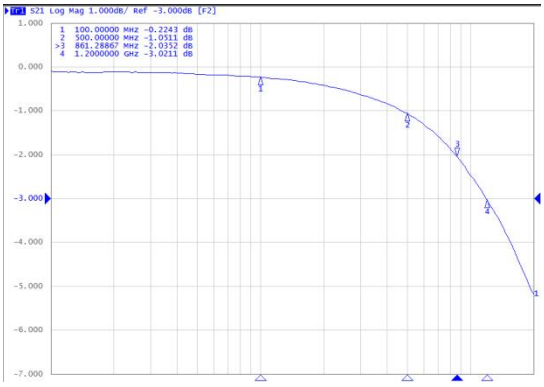


Fig.11 AUDIO Switch Bandwidth

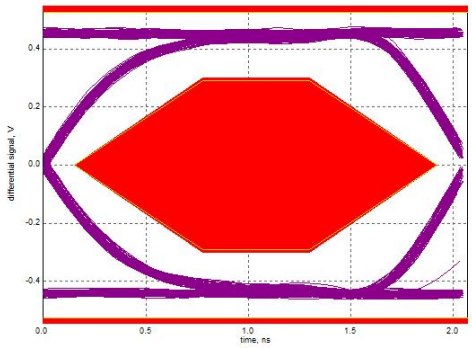


Fig.12 USB2.0 Eye Diagram of Signal Path without Switch

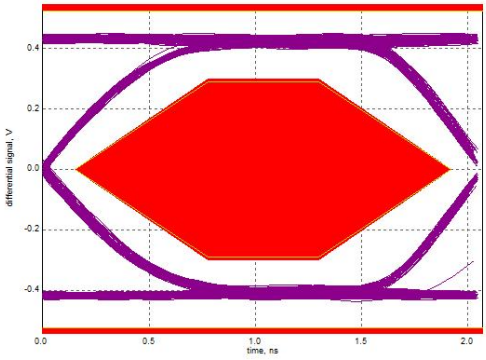


Fig.13 USB2.0 Eye Diagram of Signal Path with FSA4480UCX

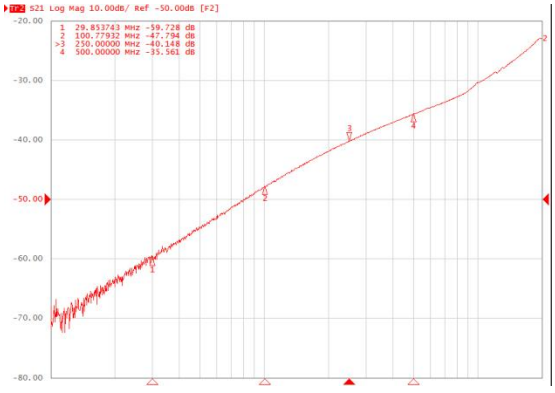


Fig.14 USB Switches Channel-to-Channel Crosstalk

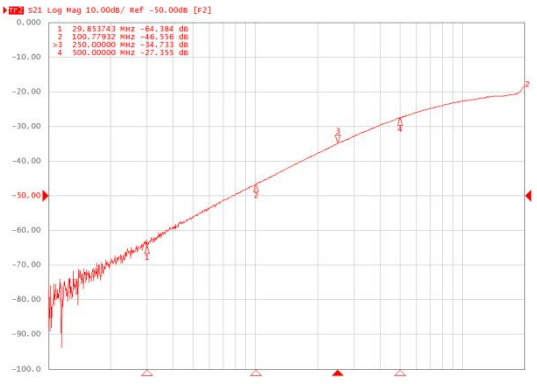


Fig.15 USB Switch OFF-Isolation

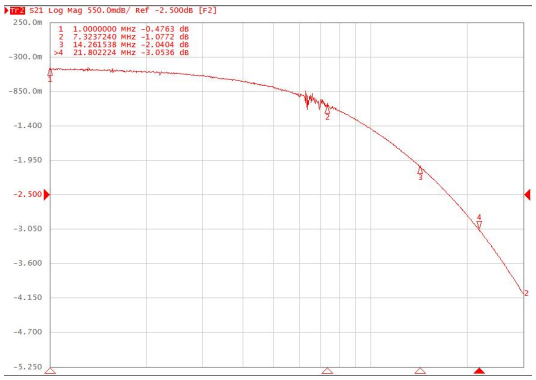


Fig.16 SBUx-to-SBUx_H Switch Insertion Loss

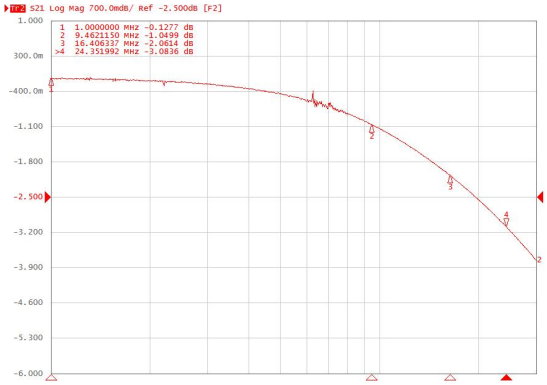


Fig.17 GSBUx-to-MIC Switch Insertion Loss

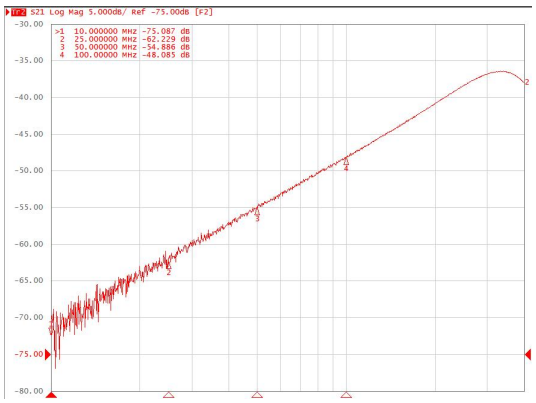


Fig.18 MIC Switch OFF Isolation

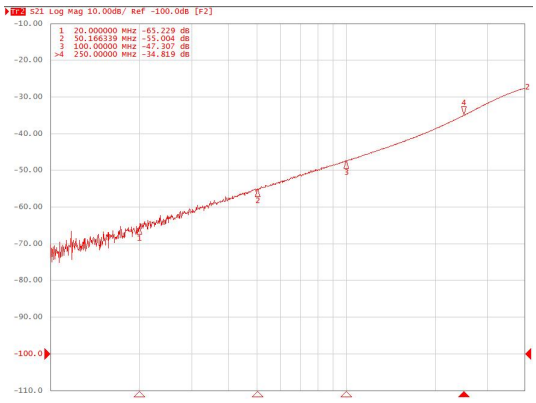


Fig.19 SENSE Switch OFF Isolation

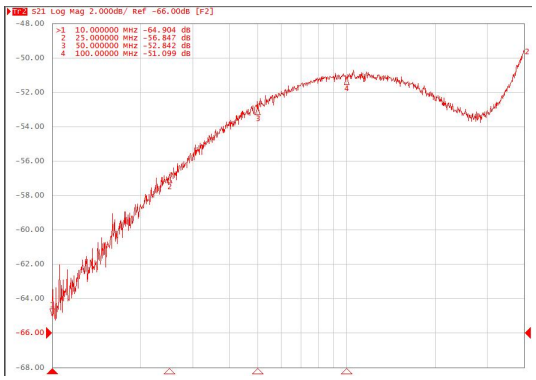


Fig.20 SBUx_H Switch OFF Isolation

Package Outline Dimensions

CSP-25

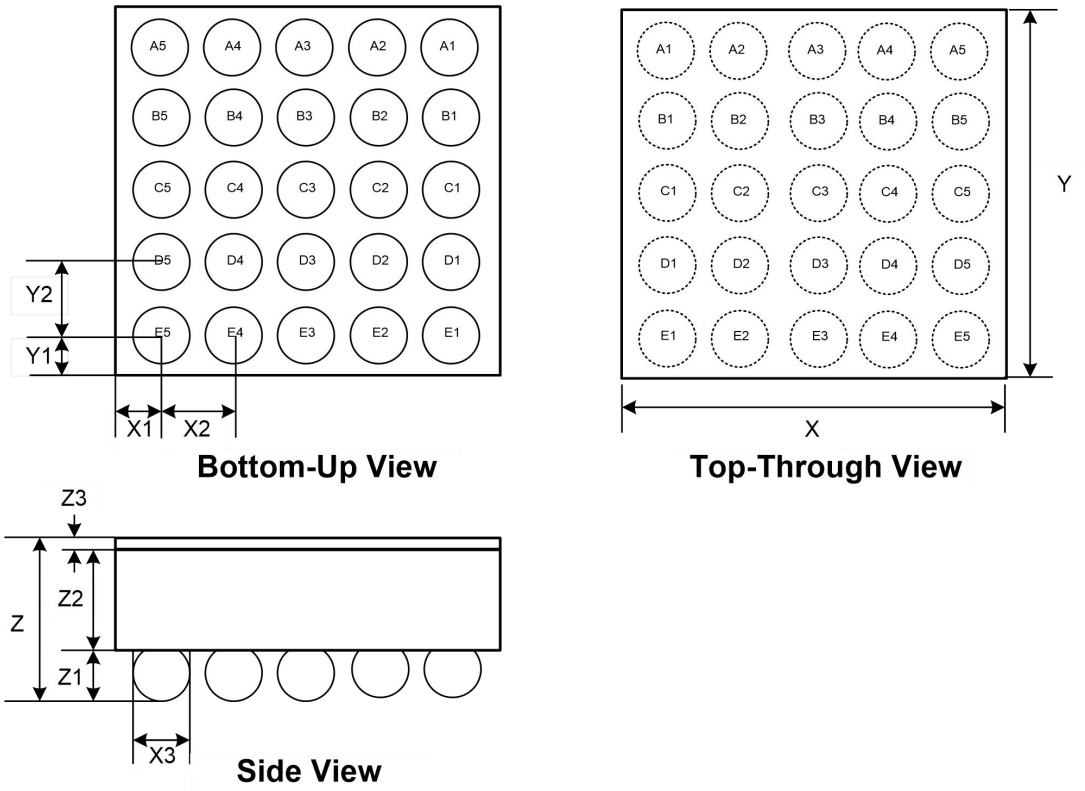


Fig.21 Package Outline Dimensions

Symbol	Dimensions In Millimeter		
	Min.	Typ.	Max.
X	2.01	2.04	2.07
Y	2.01	2.04	2.07
X1		0.18	
X2		0.40	
X3	0.175	0.205	0.235
Y1		0.18	
Y2		0.40	
Z	0.550	0.600	0.650
Z1	0.145	0.170	0.195
Z2	0.340	0.365	0.390
Z3	0.395	0.040	0.045

Table-12 Package Outline Dimensions

Attention

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