

MOSFET – Power, P-Channel, Single ATPAK

-60 V, -35 A, 29.5 mΩ

ATP113

Features

- ON-Resistance $R_{DS(on)}$ 1 = 22.5 mΩ (typ)
- 4 V Drive
- Protection Diode in
- Input Capacitance C_{iss} = 2400 pF (typ)
- This Device is a Pb-Free and Halogen Free

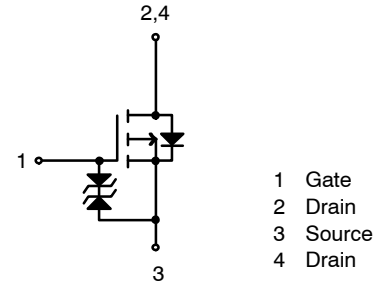
ABSOLUTE MAXIMUM RATINGS (Ta = 25°C) (Note 1)

Parameter	Symbol	Conditions	Value	Unit
Drain-to-Source Voltage	V_{DSS}		-60	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D		-35	A
Drain Current (PW ≤ 10 μs)	I_{DP}	PW ≤ 10 μs, duty cycle ≤ 1%	-105	A
Allowable Power Dissipation	P_D	Tc = 25°C	50	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		-55 to +150	°C
Avalanche Energy (Single Pulse) (Note 1)	E_{AS}		95	mJ
Avalanche Current (Note 2)	I_{AV}		-18	A

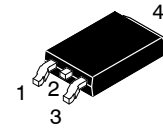
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{DD} = -10$ V, $L = 500$ μH, $I_{AV} = -18$ A

2. $L \leq 500$ μH, Single pulse

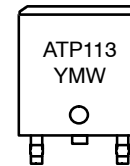


ELECTRICAL CONNECTION



**DPAK (Single Gauge) / ATPAK
CASE 369AM**

MARKING DIAGRAM



ATP113 = Specific Device Code
Y = Year of Production
M = Assembly Operation Month
W = Work Week in the Month

ORDERING INFORMATION

Device	Package	Shipping†
ATP113-TL-H	DPAK / ATPAK (Pb-Free and Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Value			Unit
			Min	Typ	Max	
Drain to Source Breakdown Voltage	V _{(BR)DSS}	I _D = -1 mA, V _{GS} = 0 V	-60	-	-	V
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V	-	-	-1	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = +16 V, V _{DS} = 0 V	-	-	+10	μA
Cutoff Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.2	-	-2.6	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10 V, I _D = -18 A	-	37	-	S
Static Drain to Source On-State Resistance	R _{DS(on)1}	I _D = -18 A, V _{GS} = -10 V	-	22.5	29.5	mΩ
	R _{DS(on)2}	I _D = -9 A, V _{GS} = -4.5 V	-	27	38	mΩ
	R _{DS(on)3}	I _D = -5 A, V _{GS} = -4 V	-	29	44	mΩ
Input Capacitance	C _{iss}	V _{DS} = -20 V, f = 1 MHz	-	2400	-	pF
Output Capacitance	C _{oss}		-	250	-	pF
Reverse Transfer Capacitance	C _{rss}		-	195	-	pF
Turn-ON Delay Time	t _{d(on)}	See specified Test Circuit.	-	15	-	ns
Rise Time	t _r		-	125	-	ns
Turn-OFF Delay Time	t _{d(off)}		-	250	-	ns
Fall Time	t _f		-	200	-	ns
Total Gate Charge	Q _g	V _{DS} = -30 V, V _{GS} = -10 V, I _D = -35 A	-	55	-	nC
Gate to Source Charge	Q _{gs}		-	7.5	-	nC
Gate to Drain "Miller" Charge	Q _{gd}		-	12	-	nC
Diode Forward Voltage	V _{SD}	I _S = -35 A, V _{GS} = 0 V	-	-0.98	-1.5	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Switching Time Test Circuit

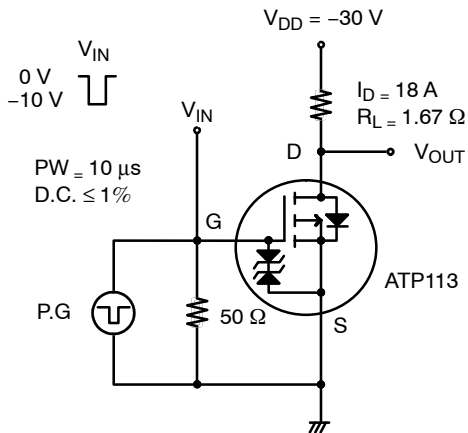


Figure 1. Switching Time Test Circuit

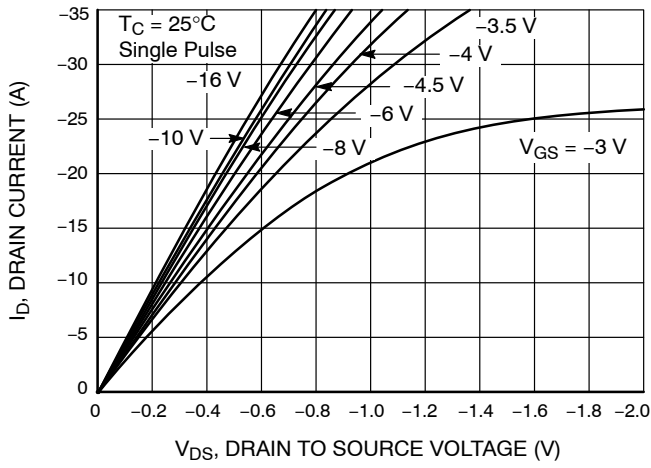


Figure 2. $I_D - V_{DS}$

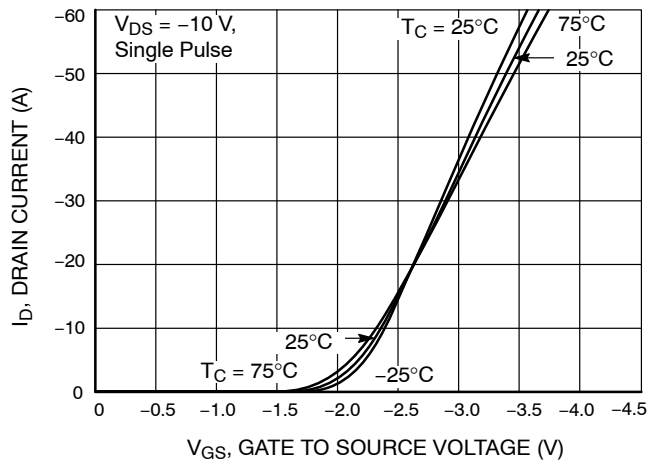


Figure 3. $I_D - V_{GS}$

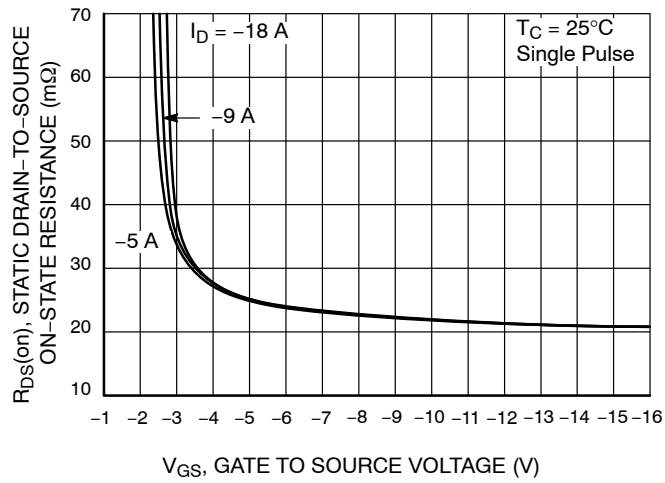


Figure 4. $R_{DS(on)} - V_{GS}$

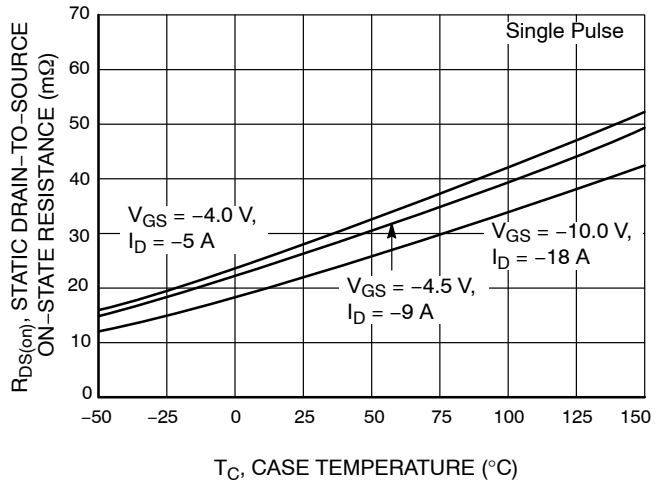


Figure 5. $R_{DS(on)} - T_C$

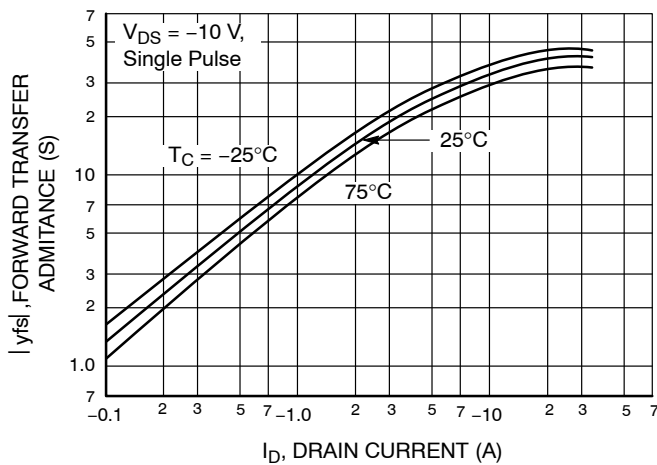


Figure 6. $|y_{fs}| - I_D$

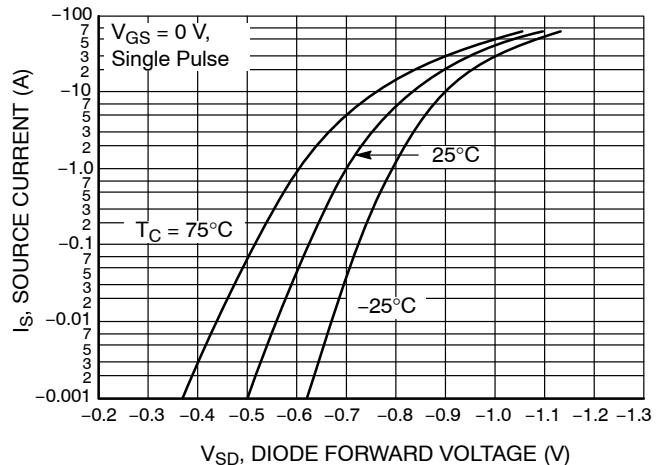


Figure 7. $I_S - V_{SD}$

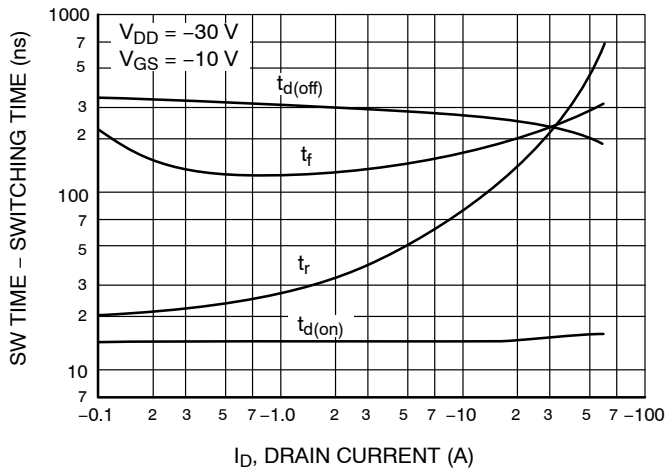


Figure 8. SW Time – I_D

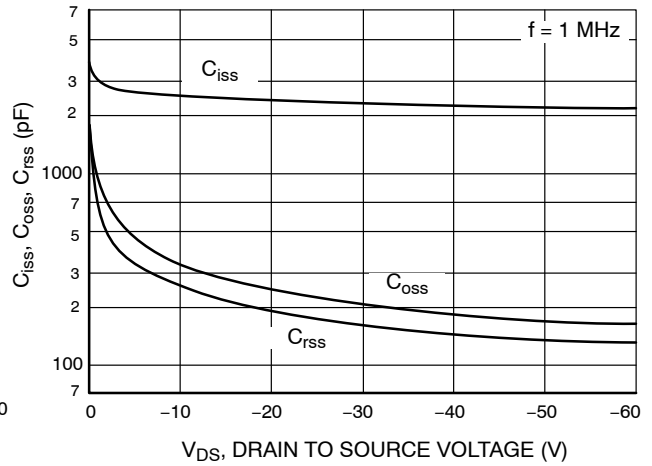


Figure 9. C_{iss} , C_{oss} , C_{rss} – V_{DS}

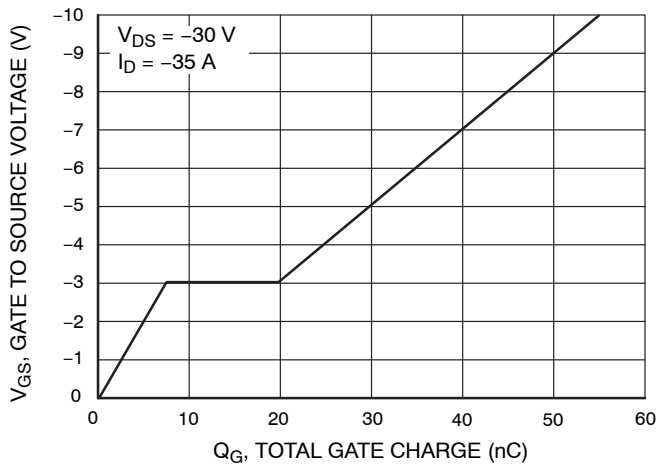


Figure 10. V_{GS} – Q_g

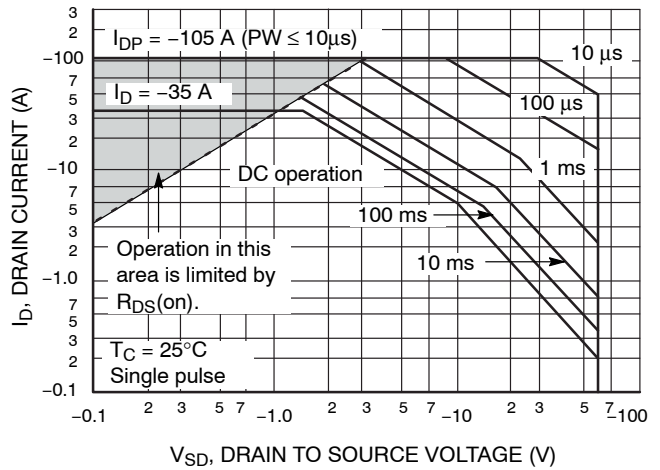


Figure 11. ASO

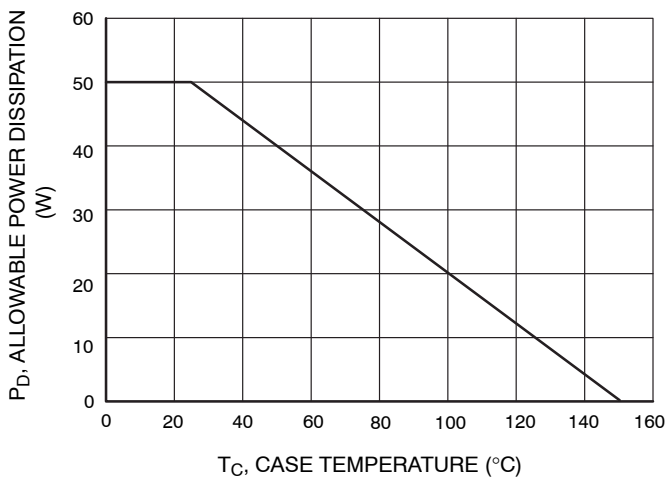


Figure 12. P_D – T_C

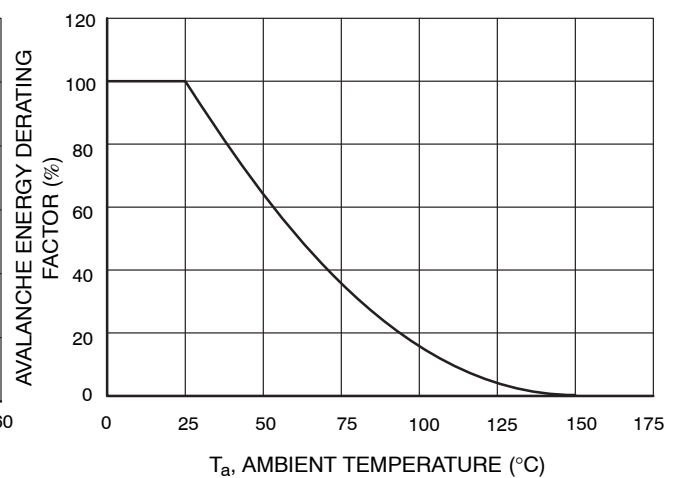


Figure 13. E_{AS} – T_a

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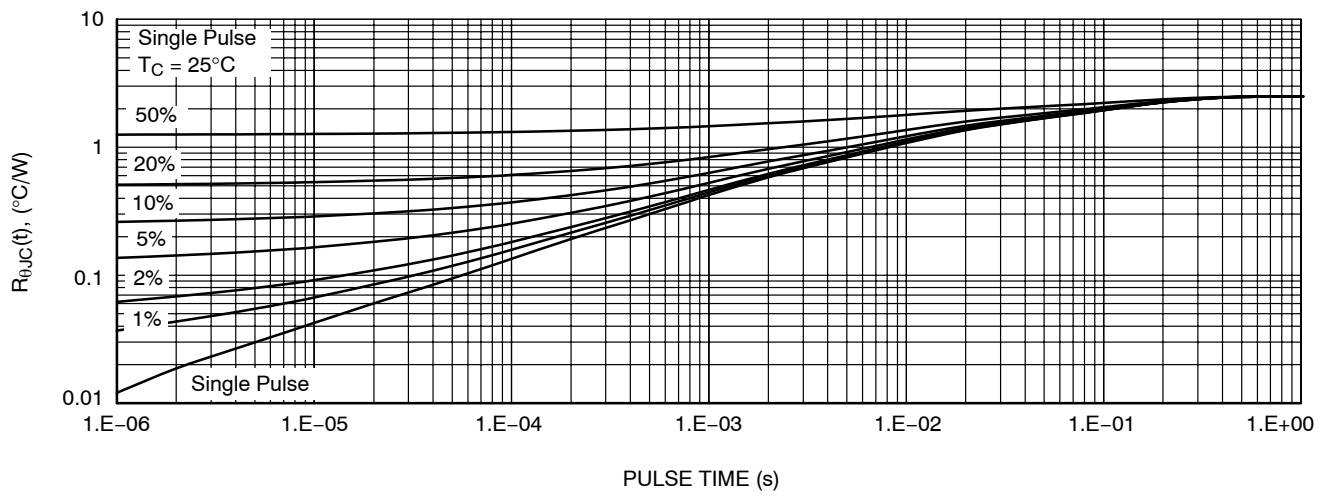
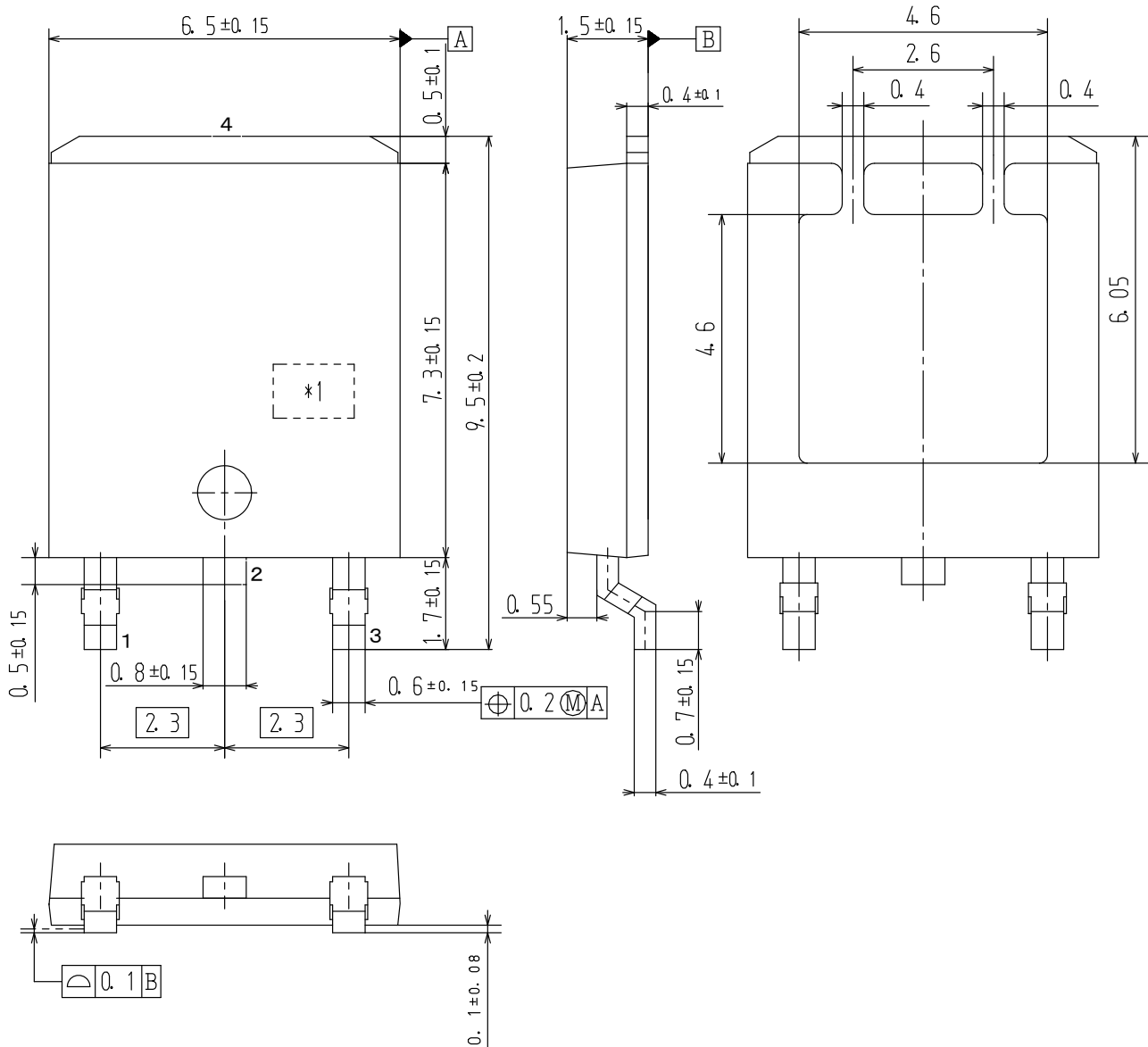


Figure 14. Thermal Response

DPAK (Single Gauge) / ATPAK
CASE 369AM
ISSUE O

DATE 29 FEB 2012



Pin2 is idle pin with electrical designation only carried

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