CD4027 CMOS Dual J-K Flip-Flop

1. General Description

1.1 Description

CD4027 is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K,Set,Reset, and Clock input signals. Buffered Q and Q signals are provided as outputs. This input-output arrangement provides for compatible operation with the CD4013B dual D type flip-flop.

The CD4027 is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

1.2 Features

- Set - Reset capability
- Static flip-flop operation - retains state indefinitely with clock level either “High” or “Low”
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 18V
- Maximum input current of 1μA at 18V and 25℃
- 5V,10V, and 15V parametric ratings

1.3 Device Information

PART NUMBER	PACKAGE
CD4027	DIP
	SOP
	TSSOP

2. Pin Description and Functional Diagram

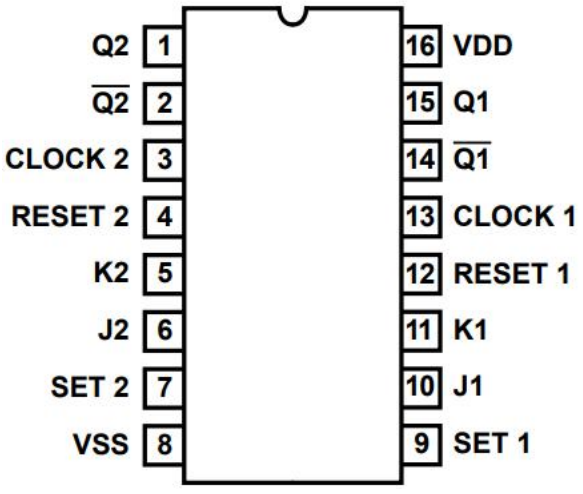


Figure 2.1 Top View

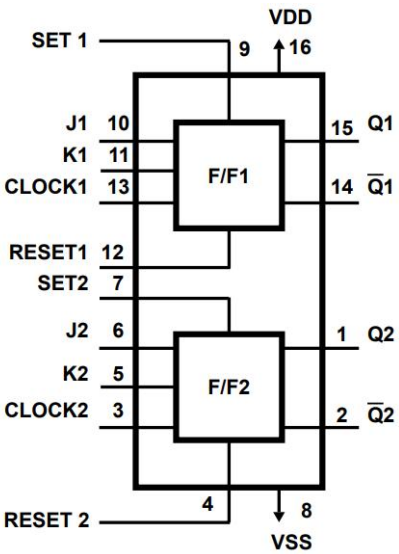


Figure 2.2 Functional Diagram

PIN No.	NAME	I/O	FUNCTION
1	Q2	O	Q Output for Channel 2
2	$\overline{Q2}$	O	Inverted Q Output for Channel 2
3	CLOCK2	I	Clock Input for Channel 2
4	RESET2	I	Reset Input for Channel 2
5	K2	I	K Input for Channel 2
6	J2	I	J Input for Channel 2
7	SET2	I	Set Input for Channel 2
8	VSS		Ground
9	SET1	I	Set Input for Channel 1
10	J1	I	J Input for Channel 1
11	K1	I	K Input for Channel 1
12	RESET1	I	Reset Input for Channel 1
13	CLOCK1	I	Clock Input for Channel 1
14	$\overline{Q1}$	O	Inverted Q Output for Channel 1
15	Q1	O	Q Output for Channel 1
16	VDD		Supply Voltage

3. System Diagram

3.1 Logic Diagram

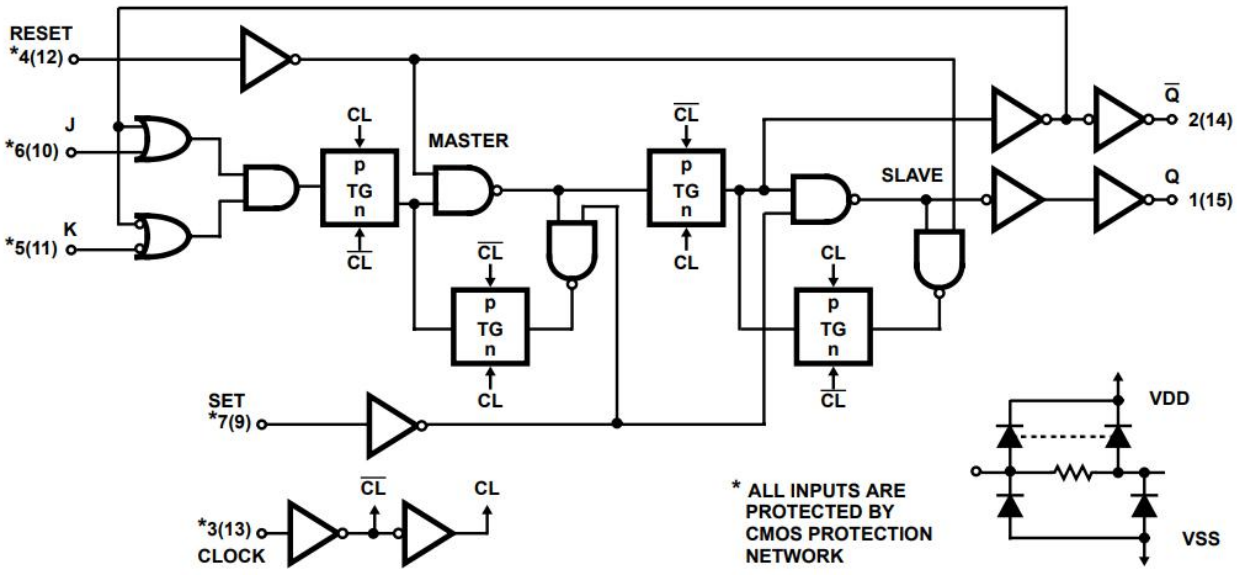


Figure 3.1：CD4027 Logic Diagram(One of Two Identical J-K Flip-Flops)

3.2 Truth Table

Clock	Present State					Next State	
	Input				Output	Output	
	J	K	S	R	Q	Q	$\overline{Q}$
↑	1	X	0	0	0	1	0
↑	X	0	0	0	1	1	0
↑	0	X	0	0	0	0	1
↑	X	1	0	0	1	0	1
↓	X	X	0	0	X	No Change	
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

X = Don't Care, 1 ≡ High State, 0 ≡ Low State,↑=positive-going transition,↓=negative-going transition

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V_{DD}	DC Supply Voltage Range (Voltage Referenced to VSS Terminals)	-0.5	20	V
V_I	Input Voltage Range, All Inputs	0.5	VDD+0.5	V
P_D	Power Dissipation		500	mW
T_J	Junction Temperature		125	℃
T_{OP}	Operating Temperature	-40	85	℃

Absolute maximum ratings are those values beyond which the device could be permanently damaged,These are stress ratings only,which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

4.2 Electrical Characteristics

4.2.1 DC Specifications

(T_a=25℃, voltages are referenced to VSS (ground=0V), unless otherwise specified)

Symbol	Parameter	Test Condition			MIN	TYP	MAX	Unit
		VO	VIN	VDD				
I_{DD}	Supply Current	--	0,5	5	--	0	1	uA
		--	0,10	10	--	0	1	uA
		--	0,18	18	--	0	1	uA
I_{OL}	Low Level Output Current	0.4	0,5	5	1	3	--	mA
		0.5	0,10	10	4	8	--	mA
		1.5	0,15	15	15	30	--	mA
I_{OH}	High Level Output Current	4.6	0,5	5	-0.5	-1.5	--	mA
		2.5	0,5	5	-3	-7	--	mA
		9.5	0,10	10	-2	-4	--	mA
		13.5	0,15	15	-7	-14	--	mA
V_{OL}	Low Level Output Voltage	--	0,5	5	--	0	0.05	V
		--	0,10	10	--	0	0.05	V
		--	0,15	15	--	0	0.05	V
V_{OH}	High Level Output Voltage	--	0,5	5	4.95	5	--	V
		--	0,10	10	9.95	10	--	V
		--	0,15	15	14.95	15	--	V
V_{IL}	Low Level Input Voltage	0.5,4.5	--	5	--	--	1.5	V
		1,9	--	10	--	--	3	V
		1.5,13.5	--	15	--	--	4	V
V_{IH}	High Level Input Voltage	0.5,4.5	--	5	3.5	--	--	V
		1,9	--	10	7	--	--	V
		1.5,13.5	--	15	11	--	--	V
I_{IN}	Input Leakage Current	--	0,18	18	--	0	±1	uA

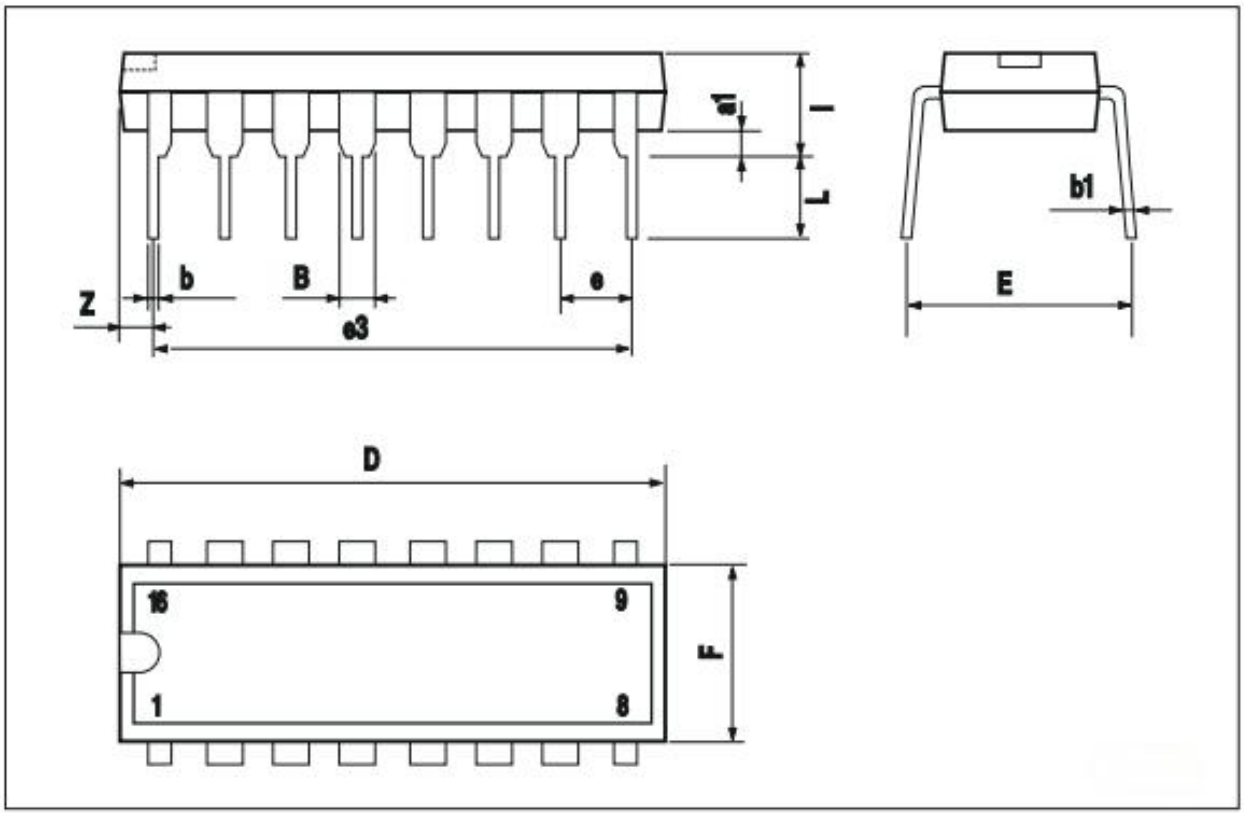
5. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
CD4027ND16ATBE	DIP	16	Tube	25
CD4027NS16ARDQ	SOP	16	Tape & Reel	4000
CD4027TS16ARDQ	TSSOP	16	Tape & Reel	4000

6. Package Information

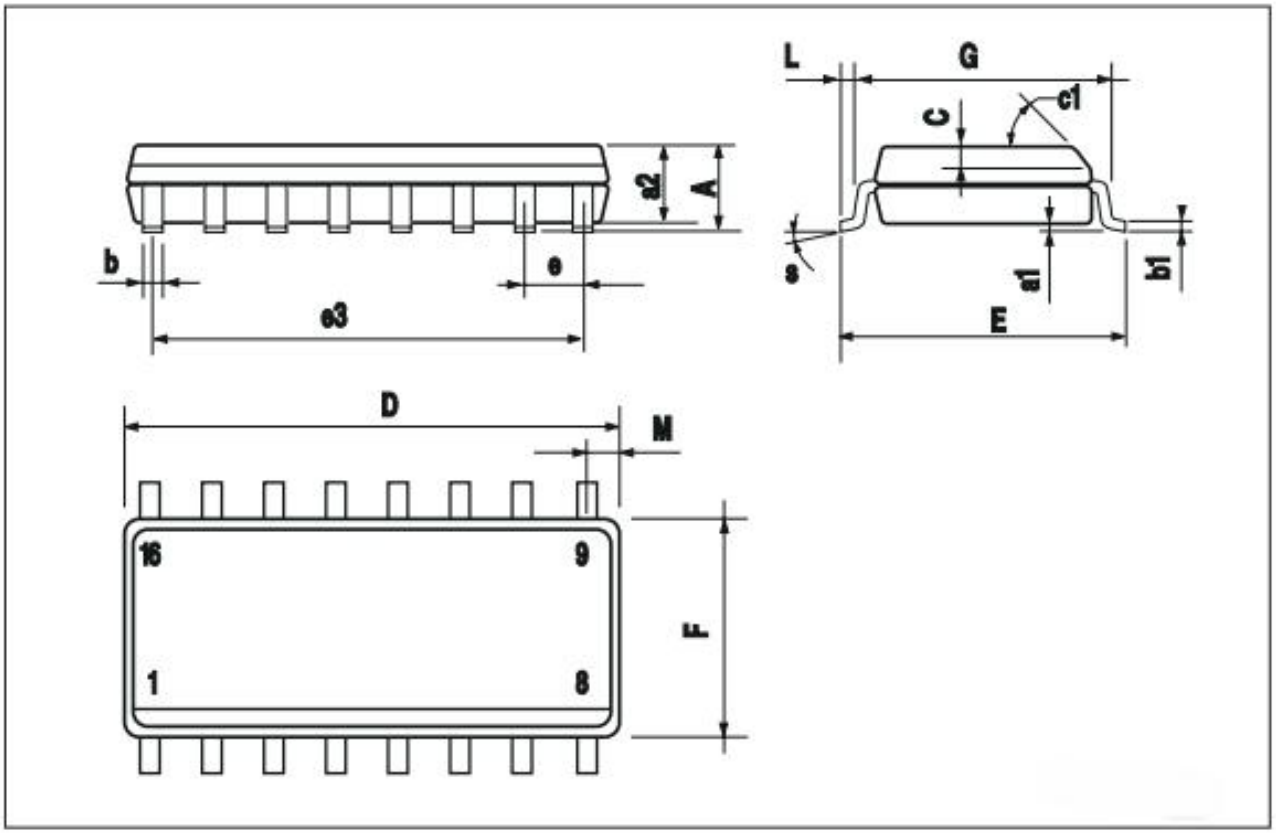
6.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



6.2 SOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



6.3 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030