Programmable Dual Output LCD Bias for Smartphone and Tablets

■ General Description

The OCP2138 is designed to support positive / negative driven TFT-LCD panels up to10" at least (from SFF to MFF like tablets). The two output rails are usually connected to the Source Driver IC. The device uses a single inductor scheme in order to provide the user the smallest solution size possible as well as high efficiency.

It features a highly integrated step-upDC-DC converter with wide input voltage range from 2.7V to 5.5V. It is optimized for products powered by single-cell batteries (Li-Ion, Ni-Li, and Li-Polymer) and symmetrical output currents up to 150mA. An LDO and charge pump generate dual outputs at +5V (default) and -5V (default),whose voltages can be programmed via an I2Ccompatible interface. Optimized step-up, LDO and charge pump converters maximize conversion efficiency, exceeding 87%.

OCP2138 integrates all compensation and soft-start circuitry, which results in a simpler and smaller solution with much fewer external components. High switching frequency (1.2MHz) allows the use of a smaller inductor and capacitor to further reduce the solution size.

The I2C compatible interface allows to control the positive and negative outputs from+4V to +6.5V and -4V to -6.5V, respectively, as well as programming additional registers on the device.

The device is a RoHs compliant 15-Ball1.9mm X 1.1mm X 0.56mm WLCSP package.

■ Features

- Wide 2.7Vto5.5V Operating Input Range
- Dual Output Regulator with Single Inductor
- Programmable Output Voltage Voltages
- Positive Output Voltage Range: +4V to +6.5V (100mV/Step)
- Negative Output Voltage Range: -4V to -6.5V (100mV/Step)
- ±1.5% Output Voltage Accuracy
- Excellent Line Regulation
- Advanced Power-Save Mode for Light Load
- Support I2C Compatible Interface
- Integrated Compensation and Feedback Circuits
- 1uA Shut-Down Supply Current
- Boost Current Mode Operation
- Over Current Protection
- Internal Soft-Start Prevents Inrush Current
- Under Voltage Lock Out
- Thermal Shutdown
- Available in an 15-Ball WLCSP
- -40℃ to +85℃OperatingTemperature Range

■ Applications

- TFT LCD Smart-phones
- TFT LCD Tablets
- General Dual Power Supply Application

■ Pin Configuration

WLCSP-15 (Top View)

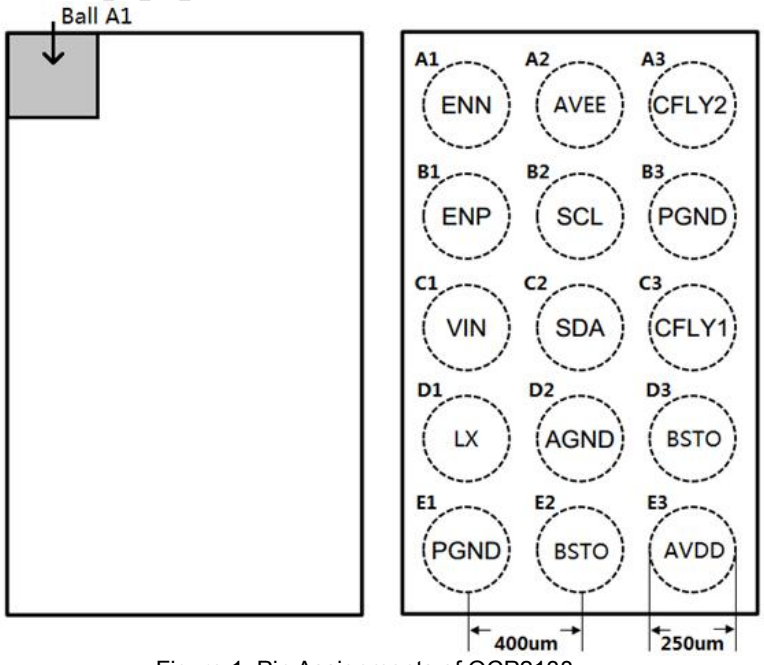


Figure 1, Pin Assignments of OCP2138

Pin Name	Pin No.	I/O	Pin Function
ENN	A1	I	Enable Input for negative output (AVEE). A logic high enable the negative Output, a logic low forces the output into shutdown mode reducing the supply current.
AVEE	A2	O	Charge pump output pin of the negative power.
CFLY2	A3	I/O	Negative charge pump flying capacitor pin.
ENP	B1	I	Enable Input for positive output (AVDD). A logic high enable the negative Output, a logic low forces the output into shutdown mode reducing the supply current.
SCL	B2	I/O	SCL clock input pin of I2C interface.
PGND	B3,E1	P	Power Ground.
VIN	C1	P	Input voltage supply pin. Connect a larger than 10uF capacitor to ground.
SDA	C2	I/O	SDA bi-direction data pin of the I2C interface
CFLY1	C3	I/O	Negative charge pump flying capacitor pin.
LX	D1	I/O	Switch pin of boost converter.
AGND	D2	P	Analog ground.
BSTO	D3,E2	I/O	Boost converter output pin.
AVDD	E3	O	Output pin of the LDO positive voltage.

■ Typical Application Circuit

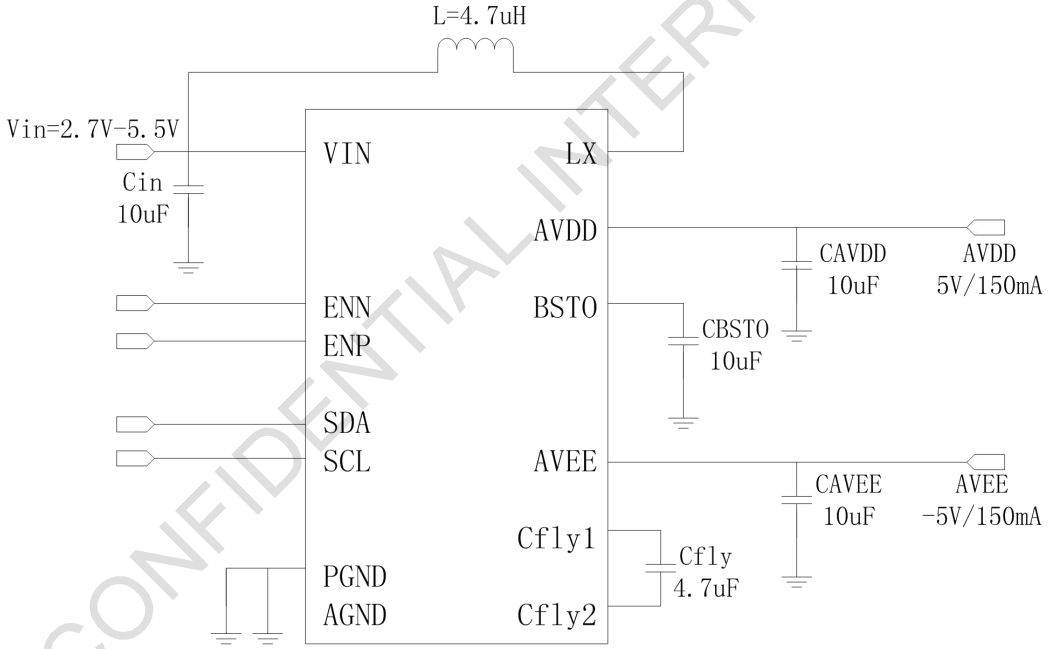


Figure 2, Typical Application Circuit of OCP2138

■ Block Diagram

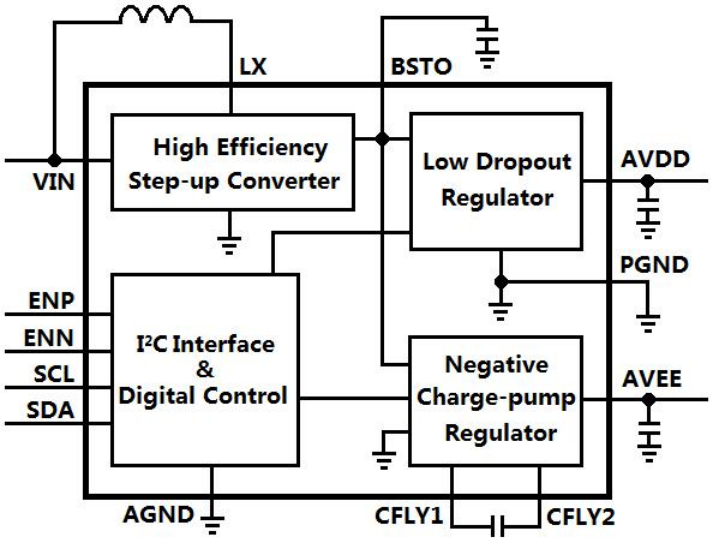


Figure 3, Block Diagram of OCP2138

■ Absolute Maximum Ratings[1] (T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
VIN, CFLY1, BSTO, LX, ENN, ENP, AVDD, SCL, SDA to GND	V_*	-0.3 to 7.0	V
AGND and PGND	GND	-0.3 to 0.3	V
CFLY2, AVEE	V_*	-7.0 to 0.3	V
Package Thermal Resistance, 15-Ball WLCSP	Θ_{JA}	77	℃/W
Power Dissipation[2]	P_D	1.3	W
Lead Temperature (Soldering, 10 Sec.)	T_{LT}	260	℃
Storage Temperature Range	T_S	-55 to +150	℃
Maximum Operating Junction Temperature Range	T_J	-40 to 125	℃

■ Recommended Operating Conditions[3](T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{IN}	Operating	2.7 ~ 5.5	V
Positive Output Voltage	V_{AVDD}	Operating	+4.0 ~ +6.5	V
Negative Output Voltage	V_{AVEE}	Operating	-4.0 ~ -6.5	V
Positive Output Current	I_{AVDD}	Operating	0 ~ 150	mA
Negative Output Current	I_{AVEE}	Operating	0 ~ 150	mA
Inductor	L	Operating	2.2~4.7	uH
Flying Capacitor	C_{FLY}	Operating	4.7	uF
Input Capacitor	C_{IN}	Operating	10	uF
AVDD, AVEE, BSTO Output Capacitor	C_*	Operating	10	uF
Operating Ambient Temperature	T_A	Operating	-40 ~ +85	℃

Notes: 1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J(MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.

■ Electrical Characteristics

(Unless otherwise noted, typical values are at T_A=25℃, V_{IN}=3.7V, ENN=ENP=V_{IN}, V_{AVDD}=5.0V, V_{AVEE}=-5.0V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General Supply						
V_{IN}	Power supply		2.7	-	5.5	V
I_Q	Quiescent Current	I_{OUT}=0mA	-	0.6	1.5	mA
I_{SD}	Shutdown down current	ENP=ENN=0V	-	0.1	-	uA
T_{SS}	Soft-Start Period		-	0.5	-	mS
V_{UVLO}	Input UVLO Threshold	V_{IN} Rising	2.0	2.3	2.5	V
V_{UVH}	Input UVLO Threshold Hysteresis		-	0.20	-	V
Logic Control: ENN, ENP, SCL, SDA						
V_{IH}	High Level Threshold Voltage	V_{EN} Rising	1.4	-	-	V
V_{IL}	Low Level Threshold Voltage		-	-	0.4	V
R_{EN}	ENP and ENN Pull-Down Resistance		-	0.5	-	MΩ
Boost Converter						
I_{LIMIT}	Boost converter current limit		0.9	1.2	1.5	A
f_{LX}	Boost converter switching frequency		1.0	1.2	1.4	MHz
LDO Positive Voltage V_{AVDD}						
V_{AVDD}	Positive output voltage range		4.0	-	6.5	V
V_{AVDDA}	Positive output voltage accuracy		-1.5	-	1.5	%
I_{AVDD}	Positive output current capability		-	150	-	mA
V_{DO}	Dropout Voltage	V_{BSTO}=V_{AVDD}=5.0V, I_{OUT}=150mA	-	150	-	mV
V_{LIP}	Line regulation	V_{IN}=2.7~5.5V, I_{OUT}=40mA	-	0.1	-	%/V
V_{LOP}	Load regulation	△I_{OUT}=150mA	-	1	-	%
Charge Pump Negative Output Voltage V_{AVEE}						
V_{AVEE}	Negative output voltage range		-4.0	-	-6.5	V
V_{AVEEA}	Negative output voltage accuracy		-1.5	-	1.5	%
I_{AVEE}	Negative output current capability		-	150	-	mA
$F_{LX\ CP}$	Charge pump switching frequency		400	600	800	KHz
V_{LIP}	Line regulation	V_{IN}=2.7~5.5V, I_{OUT}=40mA	-	0.1	-	%/V
V_{LOP}	Load regulation	△I_{OUT}=150mA	-	1	-	%
Thermal Shut-down Section[1]						
TSD	Thermal Shut-down Threshold		-	140	-	℃
Thys	Thermal Shut-down Hysteresis		-	20	-	℃

I2C Compatible Timing Specifications (SCL, SDA), see Figure 4						
f_{SCL}	SCL clock frequency	Standard Mode	-	-	100	KHz
		Fast Mode	-	-	400	KHz
t_{LOW}	Low period of the SCL clock	Standard Mode	4.7	-	-	us
		Fast Mode	1.3	-	-	us
t_{HIGH}	High period of the SCL clock	Standard Mode	4.0	-	-	us
		Fast Mode	0.6	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7	-	-	us
		Fast Mode	1.3	-	-	us
$t_{HD,STA}$	Hold time for a repeated START condition	Standard Mode	4.0	-	-	us
		Fast Mode	0.6	-	-	us
$t_{SU,STA}$	Setup time for a repeated START condition	Standard Mode	4.7	-	-	us
		Fast Mode	0.6	-	-	us
$t_{SU,DAT}$	Data setup time	Standard Mode	0.25	-	-	us
		Fast Mode	0.1	-	-	us
$t_{HD,DAT}$	Data hold time	Standard Mode	0.05	-	3.45	us
		Fast Mode	0.05	-	0.9	us
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard Mode	$20+0.1C_B$	-	1000	ns
		Fast Mode	$20+0.1C_B$	-	1000	ns
t_{RCL}	Rise time of SCL signal	Standard Mode	$20+0.1C_B$	-	1000	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
t_{FCL}	Fall time of SCL signal	Standard Mode	$20+0.1C_B$	-	300	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
t_{RDA}	Rise time of SDA signal	Standard Mode	$20+0.1C_B$	-	1000	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
t_{FDA}	Fall time of SDA signal	Standard Mode	$20+0.1C_B$	-	300	ns
		Fast Mode	$20+0.1C_B$	-	300	ns
$t_{SU,STO}$	Setup time for STOP condition	Standard Mode	4.0	-	-	us
		Fast Mode	0.6	-	-	us
C_B	Capacitive load for SCL and SDA		-	-	0.4	nF

Note. 4, OCP2138 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

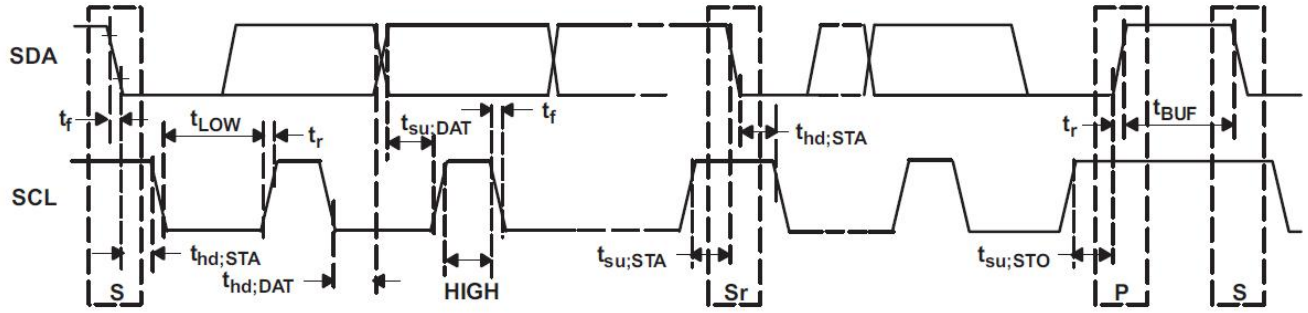
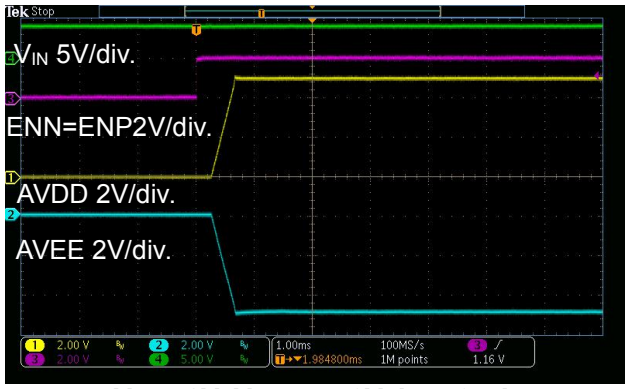


Figure 4,Serial Interface Timing for F/S-Mode I2C

■ Typical Characteristics—OCP2138

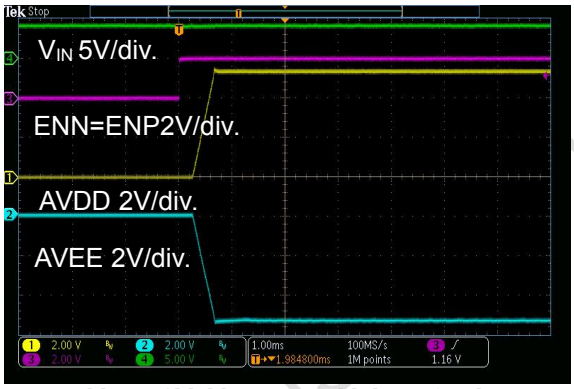
(Unless otherwise noted, typical values are at T_A=25℃, V_{IN}=3.7V, L=4.7uH, C_{IN}=C_{AVDD}=4.7uF,C_{BSTO}=C_{AVEE}=10uF, V_{AVDD}=5.0V, V_{AVEE}=-5.0V, I_{AVDD}=I_{AVEE}=40mA)

ENP=ENN On Sequence



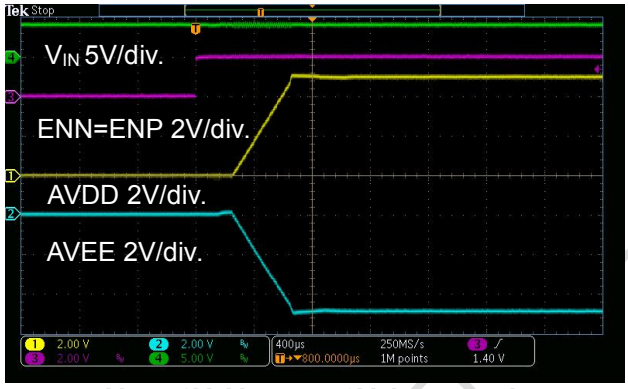
V_{IN}=4.2V, V_{OUT}=+-5.0V, I_{OUT}=0mA

ENP=ENN On Sequence



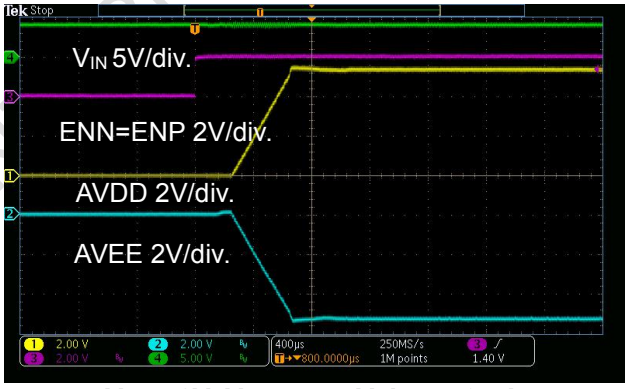
V_{IN}=4.2V, V_{OUT}=+-5.4V, I_{OUT}=0mA

ENP=ENN On Sequence



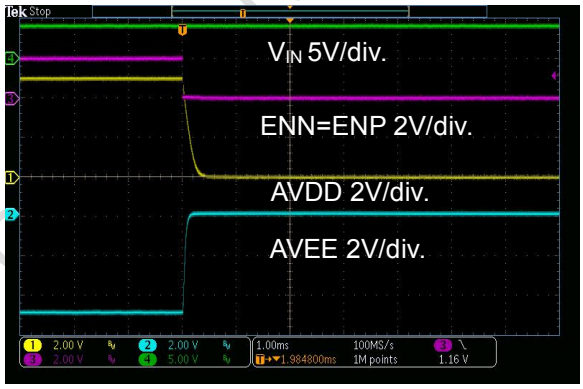
V_{IN}=4.2V, V_{OUT}=+-5.0V, I_{OUT}=40mA

ENP=ENN On Sequence



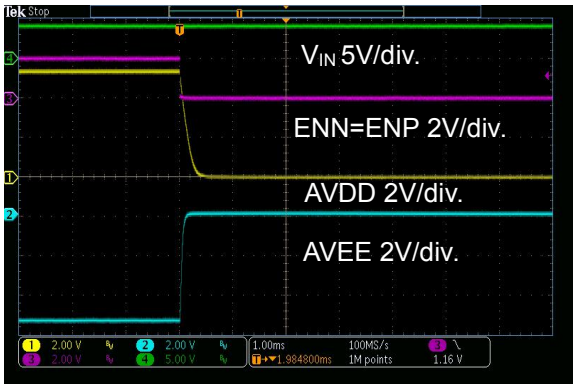
V_{IN}=4.2V, V_{OUT}=+-5.4V, I_{OUT}=40mA

ENP=ENN Off Sequence



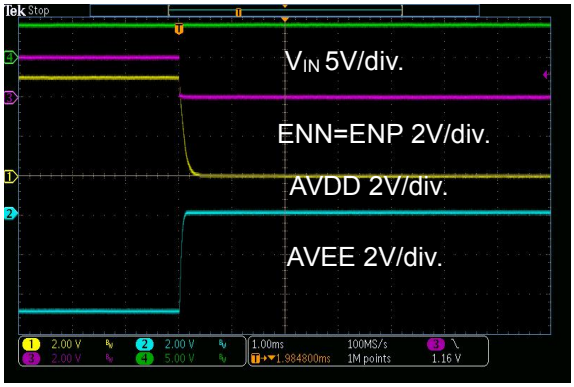
V_{IN}=4.2V, V_{OUT}=+-5.0V, I_{OUT}=0mA

ENP=ENN Off Sequence



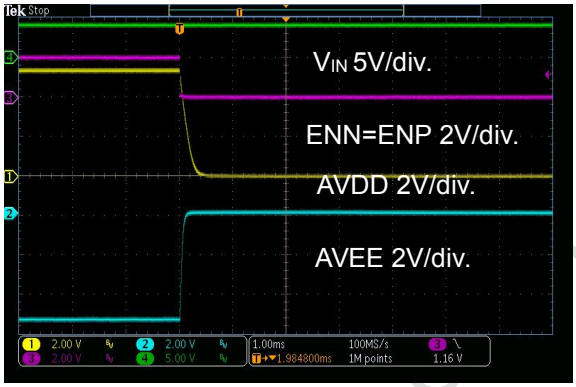
V_{IN}=4.2V, V_{OUT}=+-5.4V, I_{OUT}=0mA

ENP=ENN Off Sequence



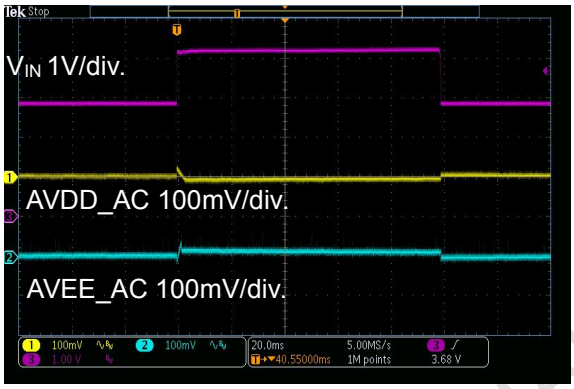
V_{IN}=4.2V, V_{OUT}=+-5.0V, I_{OUT}=40mA

ENP=ENN Off Sequence



V_{IN}=4.2V, V_{OUT}=+-5.4V, I_{OUT}=40mA

Line Transient

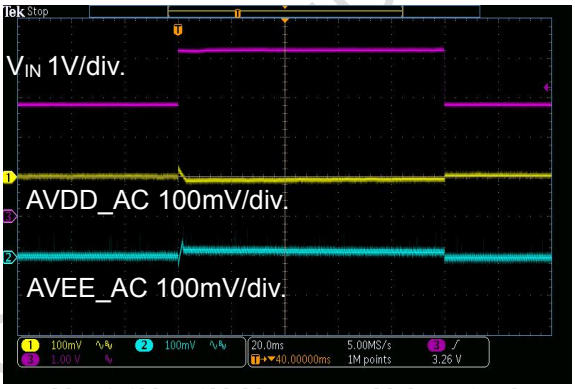


V_{IN}=2.8V~4.2V, V_{OUT}=+-5.0V, I_{OUT}=0mA

Line Transient

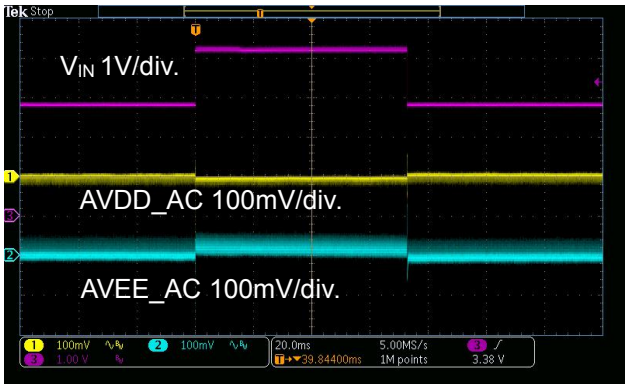
V_{IN}=2.8V~4.2V, V_{OUT}=+-5.0V, I_{OUT}=40mA

Line Transient



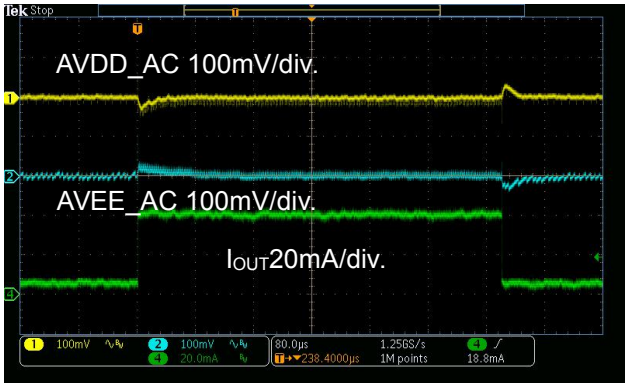
V_{IN}=2.8V~4.2V, V_{OUT}=+-5.4V, I_{OUT}=0mA

Line Transient



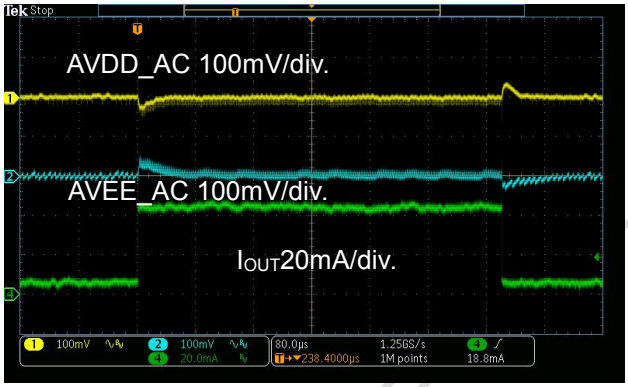
V_{IN}=2.8V~4.2V, V_{OUT}=+-5.4V, I_{OUT}=40mA

Load Transient



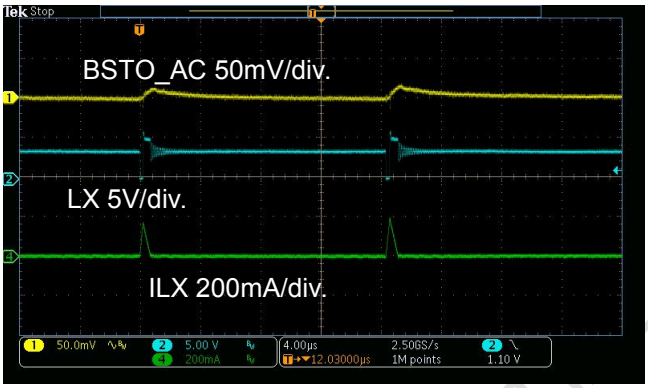
V_{IN}=4.2V, V_{OUT}=+-5.0V, I_{OUT}=5mA to 40mA

Load Transient



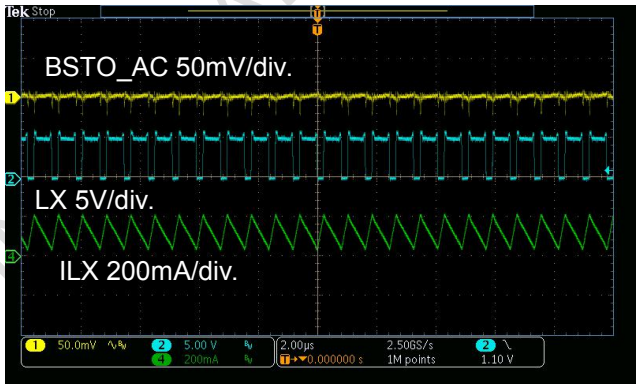
V_{IN}=4.2V, V_{OUT}=+-5.4V, I_{OUT}=5mA to 40mA

BOOST CONVERTER LIGHT LOAD

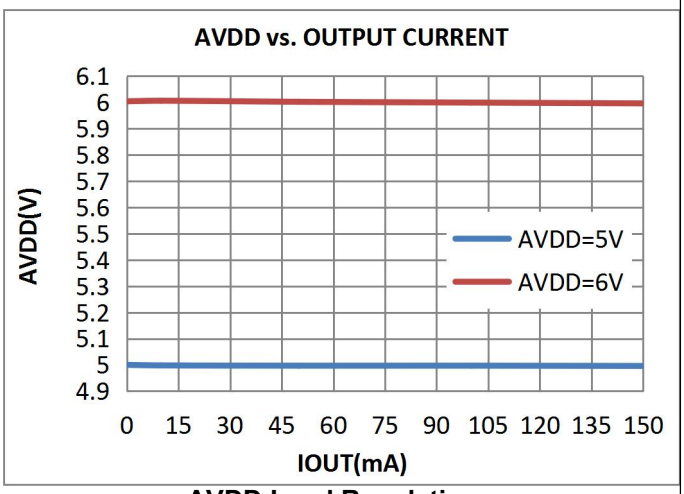


Boost Converter Light Load (1mA)

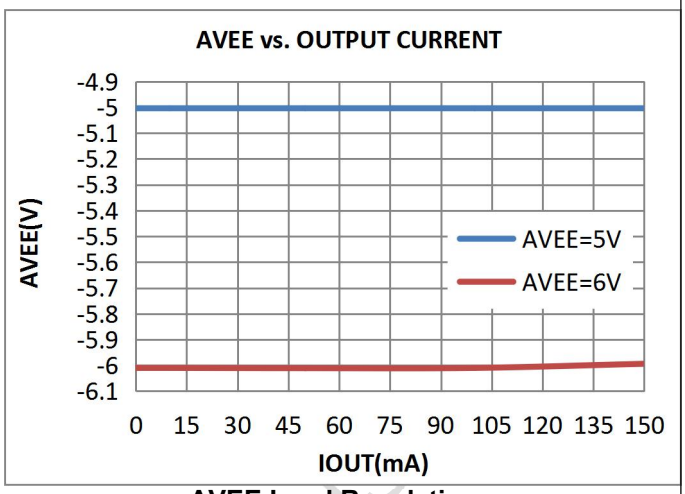
BOOST CONVERTER HEAVY LOAD



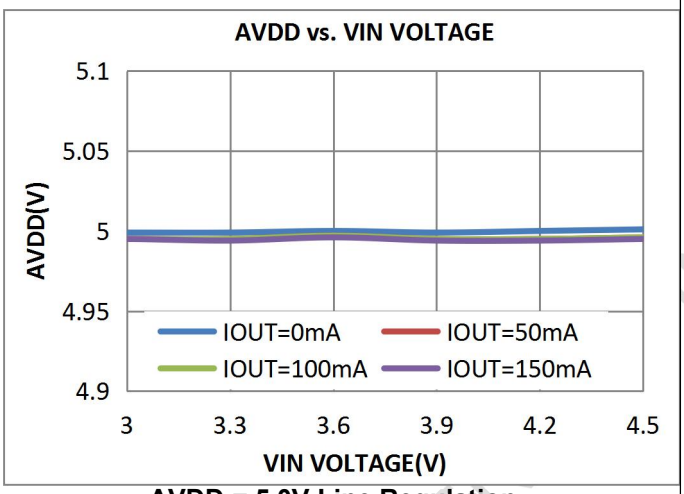
Boost Converter Heavy Load (80mA)



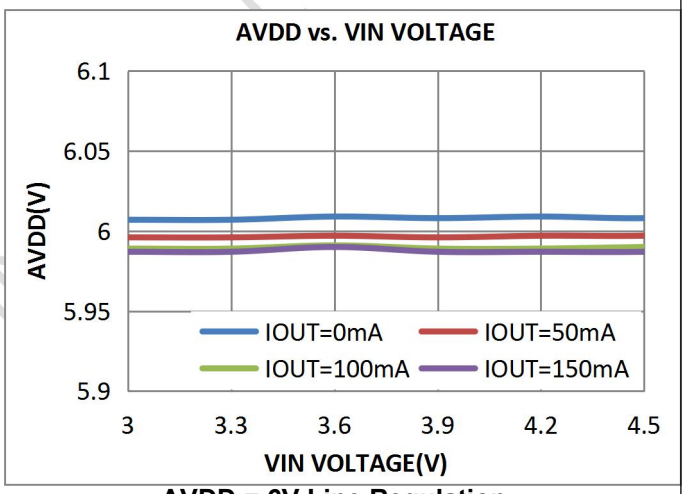
AVDD Load Regulation



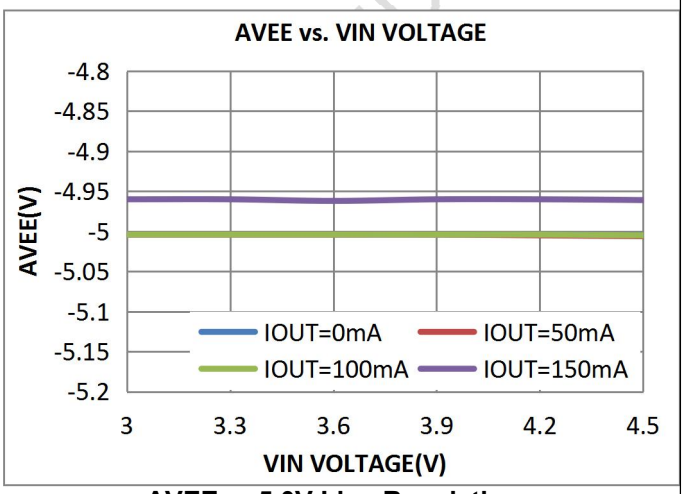
AVEE Load Regulation



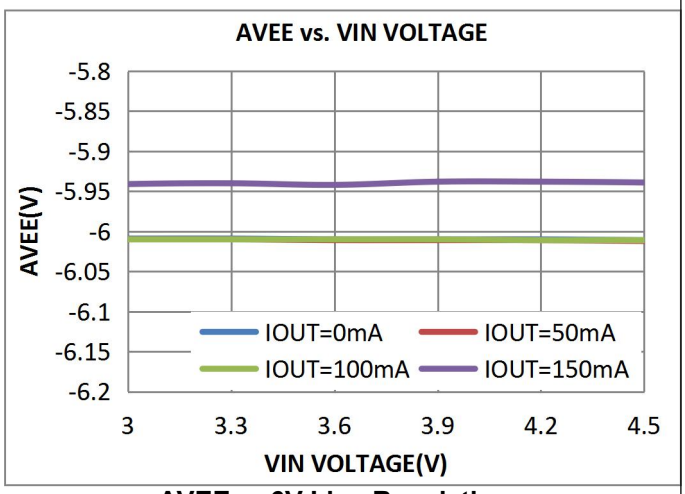
AVDD = 5.0V Line Regulation



AVDD = 6V Line Regulation



AVEE = -5.0V Line Regulation



AVEE = -6V Line Regulation

■ Functional Description

The OCP2138 is designed to support positive / negative driven TFT-LCD panels up to 10" at least (from SFF to MFF like tablets). The two output rails are usually connected to the Source Driver IC. The device uses a single inductor scheme in order to provide the user the smallest solution size possible as well as high efficiency. It features a highly integrated step-up DC-DC converter with wide input voltage range from 2.7V to 5.5V. It is optimized for products powered by single-cell batteries (Li-Ion, Ni-Li, Li-Polymer) and symmetrical output currents up to 150mA. An LDO and charge pump generate dual outputs at +5V (default) and -5V (default), whose voltages can be programmed via an I2C compatible interface. Optimized step-up, LDO and charge pump converters maximize conversion efficiency, exceeding 87%.

OCP2138 integrates all compensation and soft-start circuitry, which results in a simpler and smaller solution with much fewer external components. High switching frequency (1.2MHz) allows the use of a smaller inductor and capacitor to further reduce the solution size.

The I2C compatible interface allows to control the positive and negative outputs from +4.0V to +6.5V and -4.0V to -6.5V, respectively, as well as programming additional registers on the device.

Under Voltage Lock Out:

The OCP2138 integrates an Under-voltage Lockout block (or UVLO) that enables the device once the voltage on VIN pin exceeds the UVLO_rising threshold of 2.5 V maximum. No output voltage will however be generated as long as the enable signals are not pulled HIGH. The device, as well as all converters (boost converter, LDO, CPN), will be disabled as soon as the VIN voltage falls below the UVLO_falling threshold. The UVLO_falling threshold is designed in a way that the OCP2138 will continue operating as long as VIN stays above 2.3 V. This guarantees a proper operation even in the event of extensive line transients when the battery gets suddenly heavily loaded.

Boost Converter

Boost Converter Operation:

The synchronous boost converter uses a current mode topology and operates at a quasi-fixed frequency of typically 1.2 MHz, allowing chip inductors such as 2.2µH or 4.7µH to be used. The converter is internally compensated and provides a regulated output voltage automatically adjusted depending on the programmed VAVDD and VAVEE voltages. The boost operates either in continuous conduction mode (CCM) or Pulse Frequency

Modulation mode (PFM), depending on the load current in order to provide the highest efficiency possible.

Power Up and Soft Start (Boost Converter):

The step-up converter operates when the enable signal, ENN or ENP, is pulled high and VIN voltage is greater than UVLO. If the enable signal is already high when VIN reaches the UVLO threshold, the step-up converter will start switching immediately. An integrated soft-start circuit controls excessive inrush current from the battery during startup.

Power Down:

The boost converter stops switching when VIN reaches the UVLO_falling threshold or when both output rails are disabled, if VIN is still above the UVLO.

Isolation (Boost Converter):

The boost converter output (BSTO) is fully isolated from the input signal VIN.

Output Voltage (Boost Converter):

The output voltage of the boost converter is automatically adjusted depending on the programmed V_{AVDD} and V_{AVEE} voltages.

Advanced Power Save Mode for Light Load Efficiency and PFM:

The OCP2138 device integrates a power save mode to improve efficiency at light load. In power save mode the converter stops switching when the inductor current reaches 0A. The device resumes its switching activity with one or several pulses once the VBSTO voltage falls below its regulation level, and goes again into power save mode once the inductor current reaches 0A. Each pulse maintains the same duty ratio, but the frequency of these pulses varies according to the output load. This operating mode is also known as Pulse Frequency Modulation or PFM.

LDO Regulator

LDO Operation:

The Low Dropout regulator (or LDO) generates the positive voltage rail V_{AVDD} by regulating down the output voltage of the boost converter (V_{BSTO}). Its inherent PSRR helps filtering the output ripple of the boost converter in order to provide on AVDD pin a clean voltage, e.g. to supply the source driver IC of the display.

Power Up and Soft Start (LDO):

The LDO starts operating as soon as the ENP signal is pulled HIGH, VIN voltage is above the UVLO (under voltage lockout) threshold and the boost converter has reached its Power Good threshold. In the case where the enable signal is already HIGH when VIN reaches the UVLO_rising threshold, the boost converter will start first and the LDO will start when the boost converter has reached its target voltage. The LDO integrates a soft-start that slowly ramps up its output voltage VAVDD within 500µs typically.

Power Down and Discharge (LDO):

The LDO stops operating when VIN reaches the UVLO_falling threshold or when the ENP is pulled LOW. The positive rail can be actively discharged to GND during power-down.

Isolation (LDO):

The LDO is isolating the V_{AVDD} rail from VBSTO (boost converter output) as long as the rail is not enabled in order to ensure flexible startup like VAVEE before VAVDD.

Setting the Output Voltage (LDO):

The output voltage of the LDO is programmable via a two-wire interface with 5 bits, from 4.0V to 6.5V with 100mV steps.

Output Capacitor Selection (LDO):

The LDO is designed to operate with a 10µF minimum ceramic output capacitor.

Charge Pump Negative Converter

CPN Operation:

The negative charge pump (or CPN) generates the negative voltage rail VAVEE by inverting and regulating the output voltage of the boost converter (VBSTO). The converter uses 4 switches and an external flying capacitor to generate the negative rail. Two of the switches are turned on in the first phase to charge the flying capacitor up to VBSTO, and in the second phase they are turned-off and the two others turn on to pump the energy negatively out of the AVEE capacitor.

Power Up and Soft Start (CPN):

The CPN starts operating as soon as the ENN signal is pulled HIGH, that VIN voltage is above the UVLO (under voltage lockout) threshold and that the boost converter has reached its Power Good threshold. In the case where the enable signal is already HIGH when VIN reaches the UVLO_rising threshold, the boost converter will start first and the CPN will start when the boost converter has reached its target voltage. The CPN integrates a soft-start that slowly ramps up its output voltage VAVEE within 500µs typically.

Power Down and Discharge (CPN):

The CPN stops operating when VIN reaches the UVLO_falling threshold or when the ENN is pulled LOW The negative rail can be actively discharged to GND during power-down.

Isolation (CPN):

The CPN is isolating the VAVEE rail from VBSTO (boost converter output) as long as the rail is not enabled in order to ensure flexible startup like VAVDD before VAVEE.

Setting the Output Voltage (CPN):

The output voltage of the CPN is programmable via a two-wire interface with 5 bits, from -4.0V to -6.5V with 100mV steps.

Output Capacitor Selection (CPN):

The CPN is designed to operate with a 10μF minimum ceramic output capacitor.

Flying Capacitor Selection (CPN):

The CPN needs an external flying capacitor. The minimum value for Smartphone application is 2.2μF and 4.7μF for Tablet application. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance. Therefore, a minimum capacitance of 1μF and 2.2μFrespectively for Smartphone and Tablet applications must be achieved by the capacitor at a DC bias voltage of $|V_{AVEE}|$ + 500 mV. For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on BSTO pin.

Thermal Shutdown:

The OCP2138 contains an internal thermal sensor that limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +140°C (typ), the thermal sensor shuts down the device, turning off the DC-DC converter to allow the die to cool. After the die temperature falls by 20°C (typ), the device restarts, using the soft-start sequence.

■ Appendix I2C Interface

I2C Serial Interface Description:

The OCP2138 supports the I2C compatible interface and the data transmission protocol in two modes: standard mode and the fast mode. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master; the devices that are controlled by the master are slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The OCP2138 operates as a slave on the I2C bus. Connections to the bus are made via the open-drain I/O lines SDA and SDL.

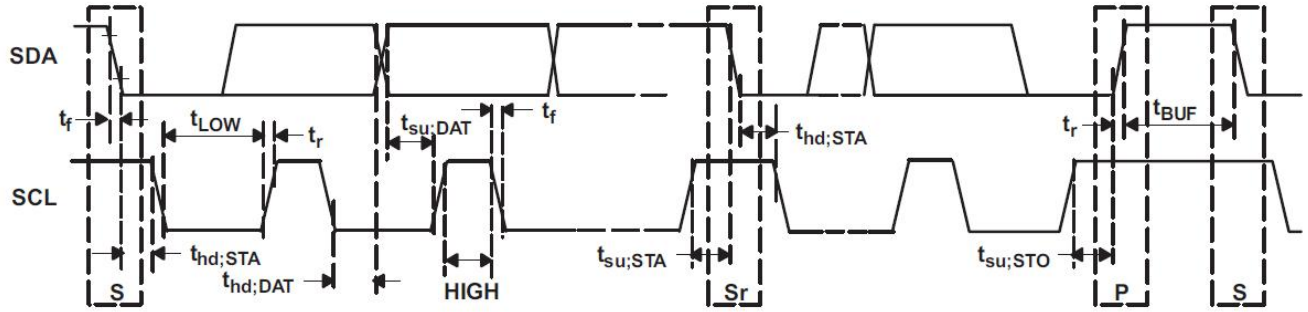


Figure 5, Serial Interface Timing for F/S-Mode I2C

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals. Accordingly, the following bus conditions have been defined:

Bus Not Busy:

Both data and clock lines remain HIGH.

Start Data Transfer:

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines a START condition.

Stop Data Transfer:

A change in the state of the data line, from LOW to HIGH, while the clock is HIGH defines a STOP condition.

Data Valid:

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise, and each receiver acknowledges with a ninth-bit. Within the I2C bus specifications, a standard mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The OCP2138works in the two modes.

Acknowledge:

Each receiving device, when accessed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Depending upon the state of the R/W bit, two types of data transfer are possible:
1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The OCP2138 can operate in the following two modes:
1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 4 for Interface). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7- OCP2138 address followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the OCP2138 acknowledges the slave address + write bit, the master transmits a register address to theOCP2138. This sets the register pointer on the OCP2138. The master may then transmit zero or more bytes of data, with the OCP2138 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.
2. Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the OCP2138 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit OCP2138 address followed by the direction bit (R/W),which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The OCP2138 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The OCP2138 must receive a “not acknowledge” to end a read.
The 7-bit slave device address is 0111110 binary (or 3Eh).

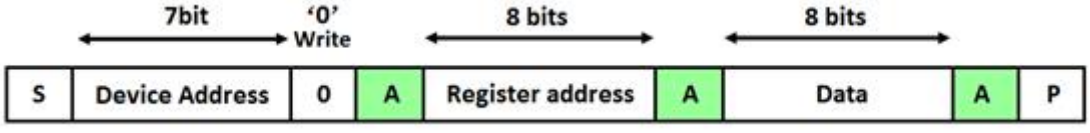


Figure 6, I2C Serial Interface Write – Slave Receiver Mode

Where
S = START condition
P = STOP condition
Device Address = 0111110(7bits, MSB first)
Register Address = Reg0 – Reg1 address(8bits)
Data = data to read or write(8bits)
1 = read Command bit
0 = write Command bit
A = acknowledge (SDA low)
A* = not acknowledge (SDA high)

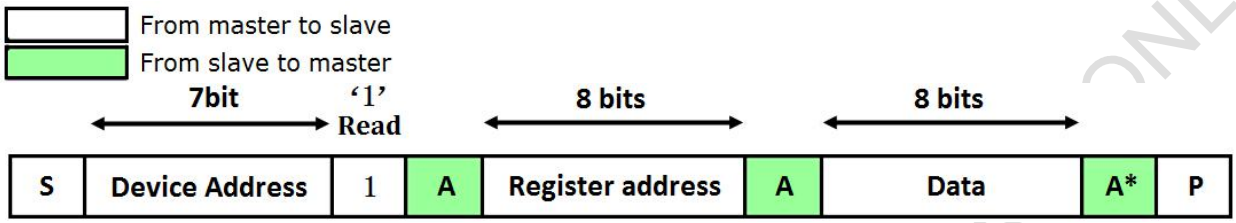


Figure 7, I2C Serial Interface Read – Slave Transmitter Mode

Address Byte:

The address byte is the first byte received following the START condition from the master device. The first seven bits (MSBs) of the slave address are factory preset to 0111110(3Eh).

Serial Data-Words	Address Byte							
Serial Data Bits	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Input Register	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Function	0	1	1	1	1	1	0	R/W

Table 1, Address Byte Code

The last bit of the address byte (R/W) defines the operation to be performed. When set to a "1", a read operation is selected; when set to a "0", a write operation is selected. Following the START condition, theOCP2138monitors the SDA bus and checks the device type identifier being transmitted. Upon receiving the 0111110 code, and the R/W bit, the slave device outputs an acknowledge signal on the SDA line.

Command Address	Description	Default	D7	D6	D5	D4	D3	D2	D1	D0
00H	Positive Output AVDD Voltage	0AH	RSVD			AVDD[4:0]				
01H	Negative Output AVEE Voltage	0AH	RSVD			AVEE[4:0]				
03H	Controller	33H	RSVD			RSVD				
04H	Device ID	03H	Read Only							

Address	D7	D6	D5	D4	D3	D2	D1	D0
03h	0	0	1	1	0	0	1	1
Controller	Read only	Read &write Default:0 Reserved	Read &write Default:1 Reserved	Read &write Default:1 Reserved	Read only	Read only	1:Discharge Default 1 0:no discharge	1:Discharge Default1 0:no discharge

I2C Serial Bus Register Map:

The device has two registers, Reg0 to Reg1. Each register includes one data byte (8 bits) that can be written or read via the I2C interface.

AVDD-00h	AVDD(V)	AVEE-01h	AVEE(V)
00h	4.0	00h	-4.0
01h	4.1	01h	-4.1
02h	4.2	02h	-4.2
03h	4.3	03h	-4.3
04h	4.4	04h	-4.4
05h	4.5	05h	-4.5
06h	4.6	06h	-4.6
07h	4.7	07h	-4.7
08h	4.8	08h	-4.8
09h	4.9	09h	-4.9
0Ah	5.0	0Ah	-5.0
0Bh	5.1	0Bh	-5.1
0Ch	5.2	0Ch	-5.2
0Dh	5.3	0Dh	-5.3
0Eh	5.4	0Eh	-5.4
0Fh	5.5	0Fh	-5.5
10h	5.6	10h	-5.6
11h	5.7	11h	-5.7
12h	5.8	12h	-5.8
13h	5.9	13h	-5.9
14h	6.0	14h	-6.0
15h	6.1	15h	-6.1
16h	6.2	16h	-6.2
17h	6.3	17h	-6.3
18h	6.4	18h	-6.4
19h	6.5	19h	-6.5

■ Application Information

Recommended Application Circuit:

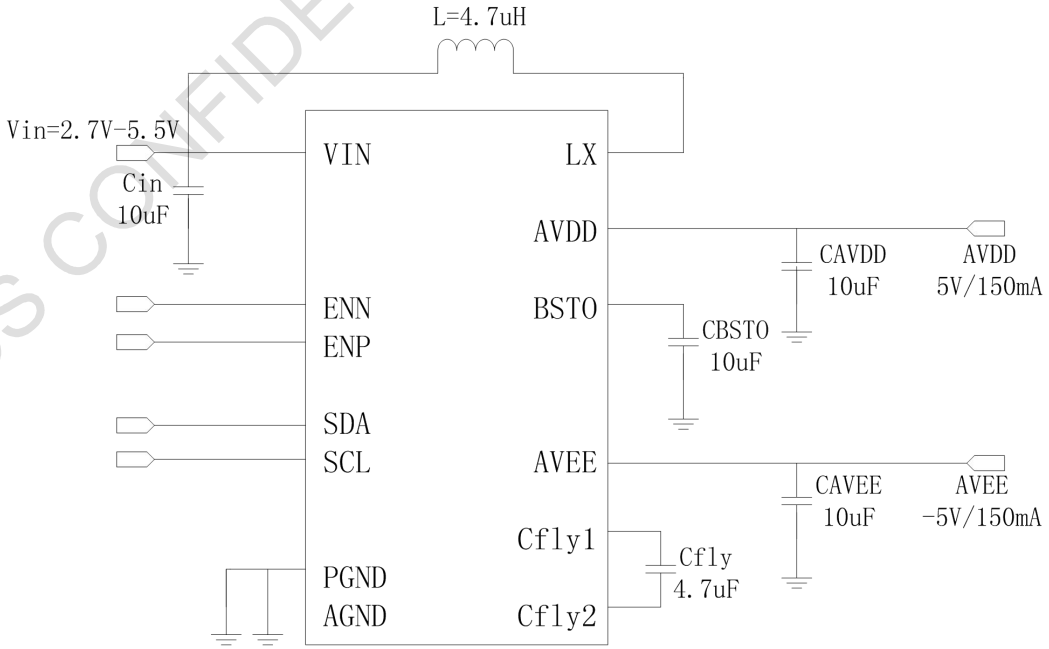


Figure 8, Typical Smartphone Application Circuit of OCP2138

Capacitor Selection:

Small size X5R or X7R ceramic capacitors are recommended for the OCP2138 application.10μF capacitors are suggested for the input VIN and AVDD. 10uF capacitors are for the outputs BSTO and AVEE. The input capacitor should be placed as close as possible to the input pin and the PGND pin of the OCP2138. For better input voltage filtering, this value can be increased. For the output capacitors, higher capacitor values can be used to improve the load transient response. For higher output current up to 150mA, the AVDD and AVEE output capacitors can be increased to 10μF.

The capacitor datasheet determines what value of capacitor is required to guarantee a minimum capacitance value for a given bias voltage and over operating temperature.

Capacitor(uF)	Supplier	Component Code	EIA Size	Voltage Rating(V)	Comments
4.7	Murata	GRM188R61C475KAAD	0603	16	C_{FLY}
10	Murata	GRM219R61C106KA73	0603	16	C_{IN}, C_{AVDD},
10	Murata	GRM219R61C106KA73	0603	16	C_{BSTO}, C_{AVEE}

Table 2, Input And Output Capacitor Selection

Inductor Selection:

Saturation current: the inductor must handle the maximum peak current {I_{L_SAT}> I_{LXPEAK}, or I_{L_SAT}> [I_{LIM_min} + ΔI_L] as conservative approach}

DC Resistance: the lower the DCR, the lower the losses

Inductor value: in order to keep the ratio I_{OUT} / ΔI_L low enough for proper sensing operation purpose, it is recommended to use a 4.7μH inductor for Smartphone applications (a 2.2μH might however be used, but the efficiency might be lower than with 4.7μH at light output loads) and for Tablet applications, 4.7μH are recommended.

L(uH)	Supplier	Component Code	EIA Size	DCR TYP(mΩ)	I_{SAT}(A)
2.2	Murata	LQM2HPN2R2MG0	1008	80	1.3
2.2	Murata	LQM21PN2R2NGC	0805	250	0.8
4.7	Murata	LQM21PN4R7MGR	0805	230	0.8

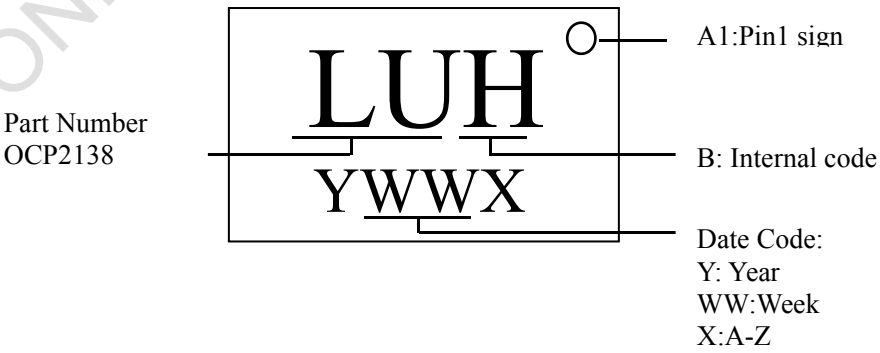
Table 3, Inductor Selection

■ Ordering Information

Part Number	Driver Capability	Package Type	Package Qty	Temperature	Eco Plan	Lead/Ball Finish
OCP2138WPAD	+150/-150mA	15-Ball WLCSP	3000pcs	-40～85℃	Green	Su/Ag/Cu

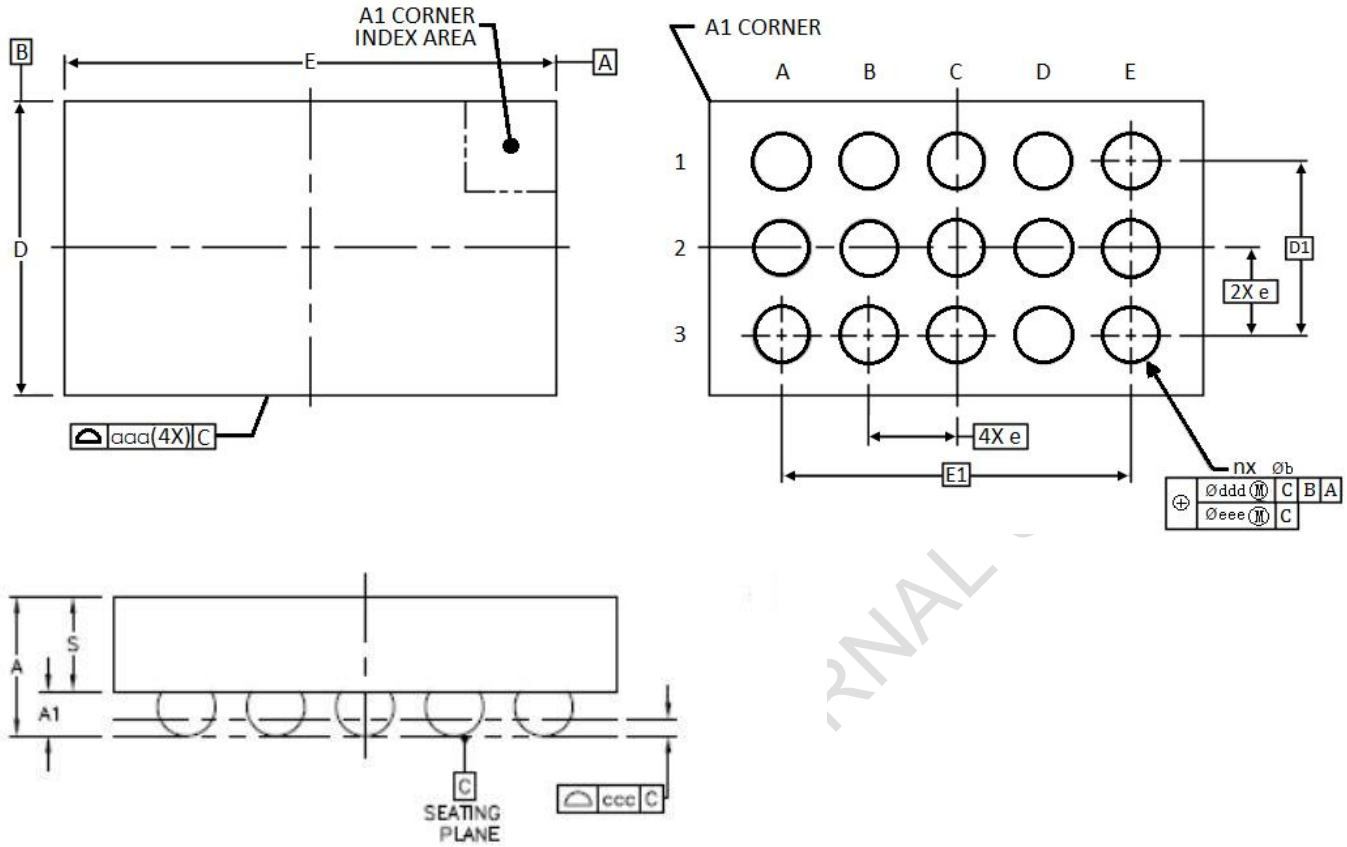
■ Marking Information

15-Ball WLCSP



■ Package Information

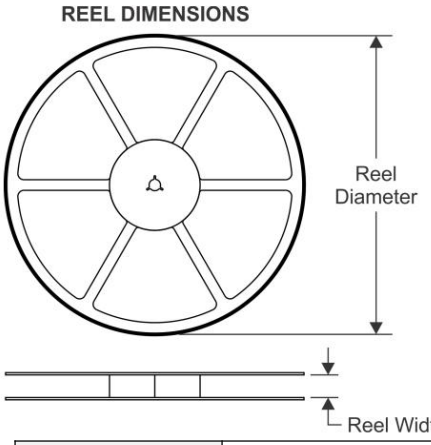
15-Ball WLCSP

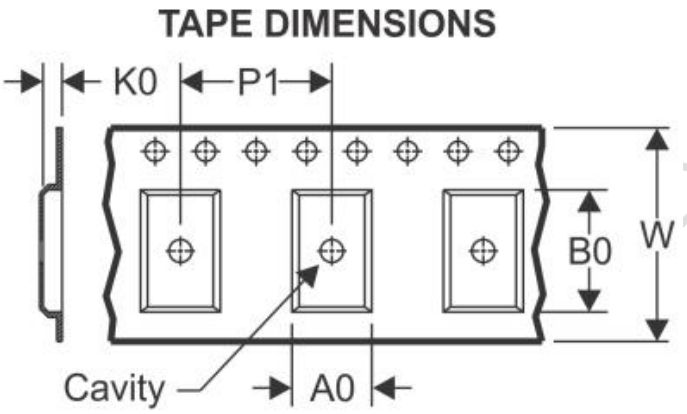


		SYMBOL	COMMON DIMENSIONS
TOTAL THICKNESS		A	0.559 ± 0.039
WAFER THICKNESS		S	0.395 ± 0.016
STAND OFF		A1	0.164 ± 0.025
PACKAGE SIZE	X	E	1.97
	Y	D	1.17
EDGE BALL CENTER TO CENTER	X	E1	1.6 BSC
	Y	D1	0.8 BSC
PITCH		e	0.4 BSC
BALL DIAMETER			0.208 ±30
BALL/BUMP WIDTH		b	0.208 ±30
BALL/BUMP COUNT		n	15

■ Packing Information

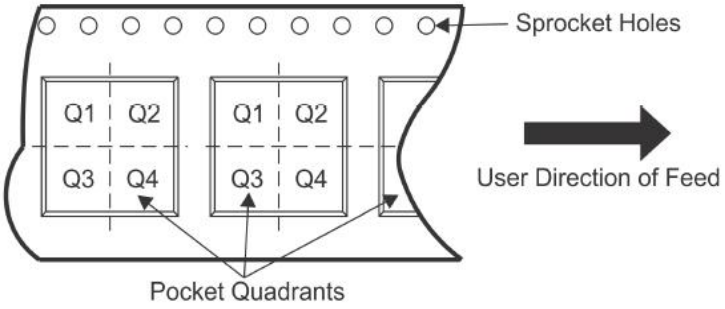
15-Ball WLCSP





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package tape	Package Drawing	MSL	SPQ	Reel Diameter (mm)	Reel Width W1(mm)
15-Ball WLCSP (WLCSP15)	LUH	Level-1-260C	3000	180	8.4
A0 (mm)	**B0 (mm)**	**K0 (mm)**	**P1 (mm)**	**W (mm)**	**PIN A1 Quadrant**
1.4	2.2	0.77	4.0	8.0	Q1

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