

Description

The SXJ30N65D protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, low operating voltage. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.

General Features

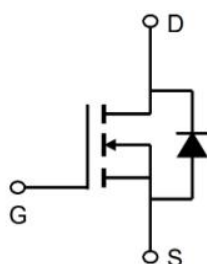
$V_{DS} = 650V$ (Type: 740V) $IDM = 30A$

$R_{DS(ON)} < 340m\Omega$ @ $V_{GS}=10V$

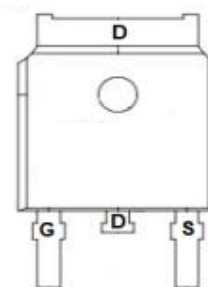
Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



TO-252-3L



Absolute Maximum Ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0V$)	650	V
I_D	Continuous Drain Current	14	A
I_{DM}	Pulsed Drain Current (note1)	30	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	250	mJ
P_D	Power Dissipation ($T_c = 25^{\circ}C$)	25.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^{\circ}C$
R_{thJC}	Thermal Resistance, Junction-to-Case	1.2	$^{\circ}C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62	$^{\circ}C/W$

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V _{GS} =0V, I _D =250uA	650	740	--	V
ΔBV _{DSS} / ΔT _J	Breakdown voltage temperature coefficient	I _D =250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V _{DS} =650V, V _{GS} =0V	--	--	1	uA
		V _{DS} =520V, T _C =125°C	--	--	50	uA
IGSS	Gate to source leakage current, forward	V _{GS} =30V, V _{DS} =0V	--	--	100	nA
	Gate to source leakage current, reverse	V _{GS} =-30V, V _{DS} =0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V _{DS} =V _{GS} , I _D =250uA	2.5	3.3	4.5	V
RDS(ON)	Drain to source on state resistance	V _{GS} =10V, I _D =3.2A	--	280	340	mΩ
Ciss	Input capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	--	781	--	pF
Coss	Output capacitance		--	30.3	--	
Crss	Reverse transfer capacitance		--	1.47	--	
td(on)	Turn on delay time	V _{DS} =400V, I _D =7A, R _G =4.7Ω , V _{GS} =10V	--	6.2	--	ns
tr	Rising time		--	21	--	
td(off)	Turn off delay time		--	28.8	--	
tf	Fall time		--	22.4	--	
Q _g	Total gate charge	V _{DS} =400V, V _{GS} =10V, I _D =7A	--	2.77	--	nC
Q _{gs}	Gate-source charge		--	5.8	--	
Q _{gd}	Gate-drain charge		--	20.4	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	14	A
ISM	Pulsed source current		--	--	44	A
VSD	Diode forward voltage drop.	I _S =7A, V _{GS} =0V	--	0.7	1.5	V
T _{rr}	Reverse recovery time	I _S =7A, V _{GS} =0V, V _{DD} =400V, di/dt=100A/us,	--	218	--	ns
Q _{rr}	Reverse recovery Charge		--	1.1	--	uC

Note :

- 1、The data tested by surface mounted on a 1 inch2 FR-4 board with 20Z copper.
- 2、The EAS data shows Max. rating . L=0.5mH, IAS =7A, VDD =50V, RG=25Ω
- 3、The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD≤ BVDSS, Starting at TJ =25°C
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

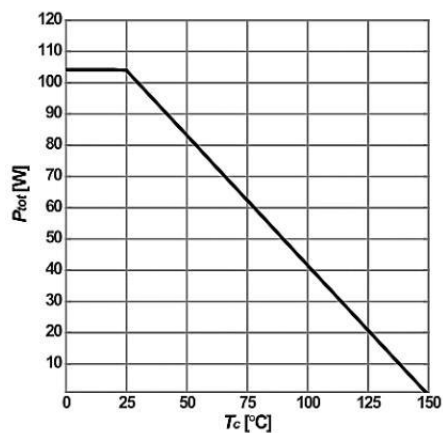


Figure1: Power dissipation (Non FullPAK)

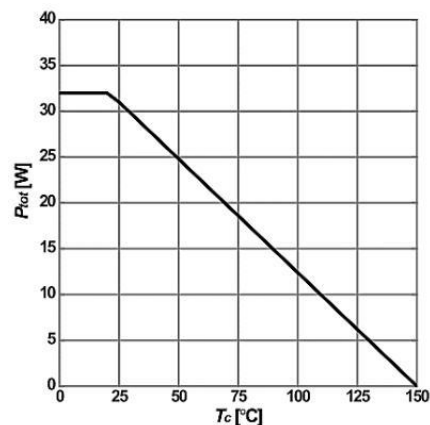


Figure2: Power dissipation (FullPAK)

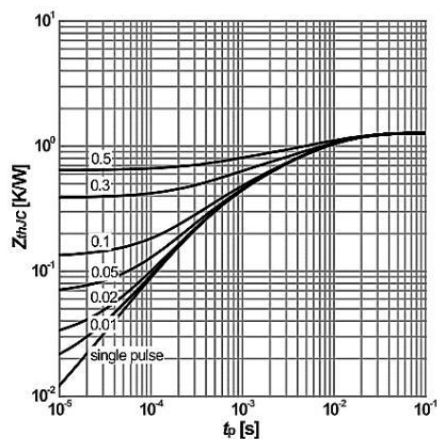


Figure3:Max. transient thermal impedance
zn. $c=f(t_p)$; parameter: $D=t/T$

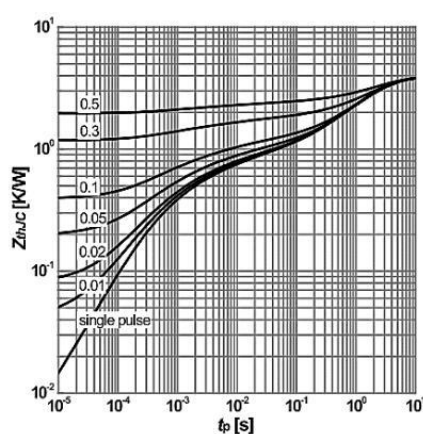


Figure4:Max. transient thermal impedance
zn. $c=f(t_p)$; parameter: $D=t/T$

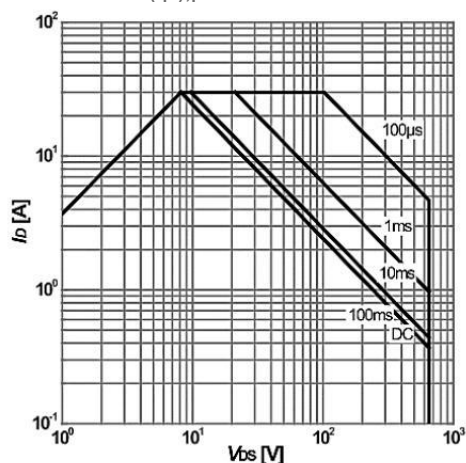


Figure5: Safe operating area (Non FullPAK)
 $o=f(v_{os})$; $T=25^\circ\text{C}$; $D=0$; parameter: t_b

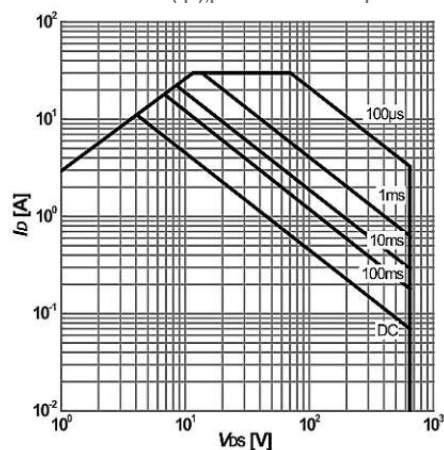


Figure6: Safe operating area (FullPAK)
 $o=f(v_{os})$; $T=25^\circ\text{C}$; $D=0$; parameter: t_b

Typical Characteristics

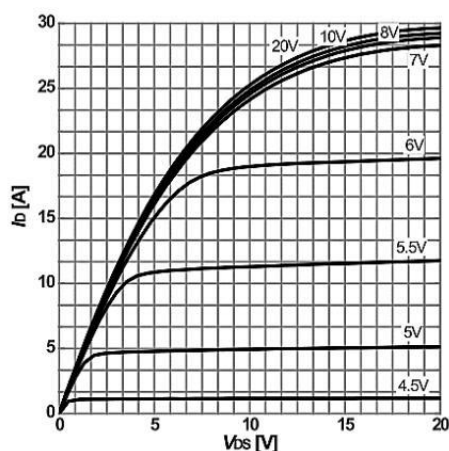


Figure 7: Typ. output characteristics

$I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

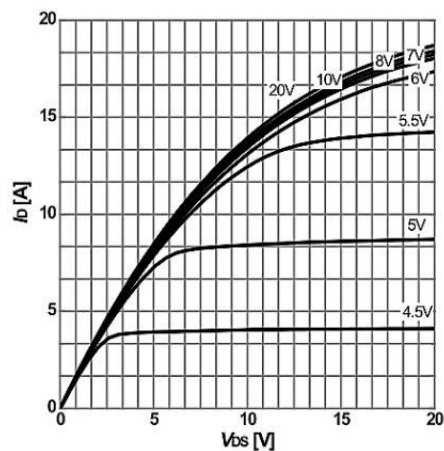


Figure 8: Typ. output characteristics

$I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

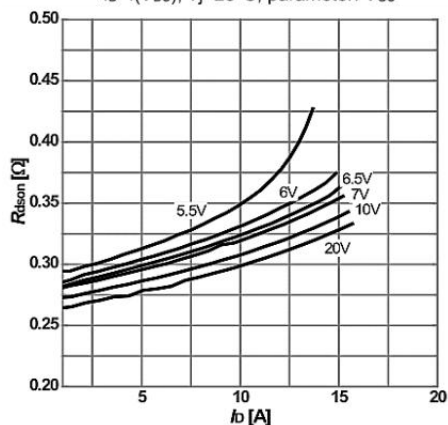


Figure 9: Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

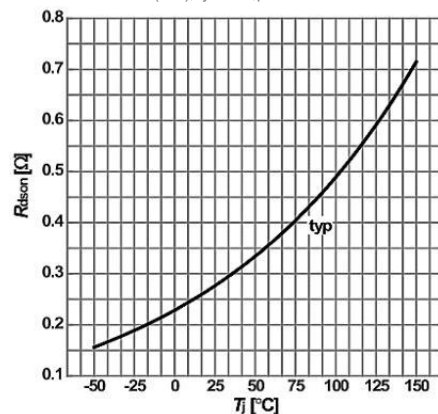


Figure 10: drain-source on-state resistance

$R_{DS(on)} = f(T_J); I_D = 3.2\text{A}; V_{GS} = 10\text{V}$

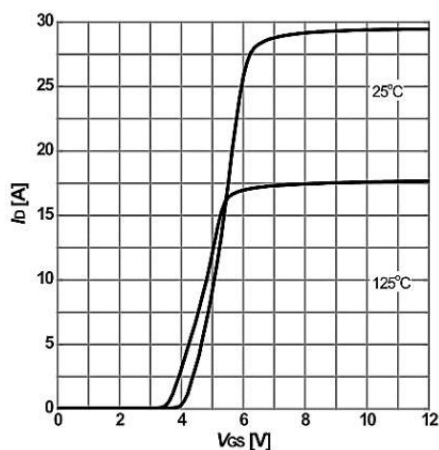


Figure 11: Type. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 20\text{V}; \text{parameter: } T$

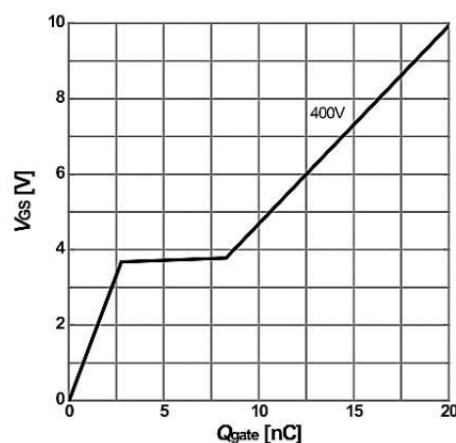
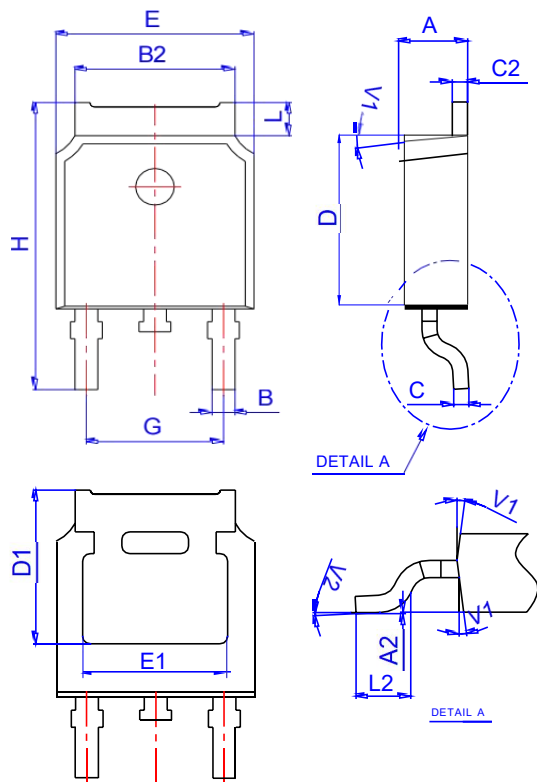


Figure 12: Type. gate charge

$V_{GS} = f(Q_{gate}); I_D = 3.2\text{A pulsed}; V_{DS} = 480\text{V}$

Package Mechanical Data:TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-252-3L		2500