

**Description**

The SX5N50D uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as high EAS. This device is suitable for use as a Battery protection or in other Switching application.

**General Features**

$V_{DS} = 500V$   $I_D = 5 A$

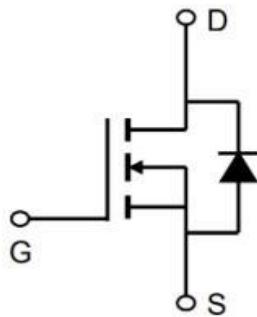
$R_{DS(ON)} < 1.6\Omega$  @  $V_{GS}=10V$

**Application**

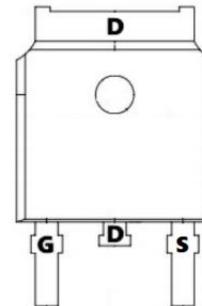
Switch Mode Power Supply (SMPS)

Uninterruptible Power Supply (UPS)

Power Factor Correction (PFC)



TO-252-3L

**Absolute Maximum Ratings** ( $T_c=25^\circ C$  unless otherwise specified)

Symbol	Parameter	Max.		Units
		TO-252		
$V_{DSS}$	Drain-Source Voltage	500		V
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$I_D$	Continuous Drain Current	$T_c = 25^\circ C$	5	A
		$T_c = 100^\circ C$	3.4	A
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	20		A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>	90		mJ
$P_D$	Power Dissipation	$T_c = 25^\circ C$	45	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.8	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		60	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

**Electrical Characteristics** ( $T_c=25^\circ\text{C}$  unless otherwise specified)

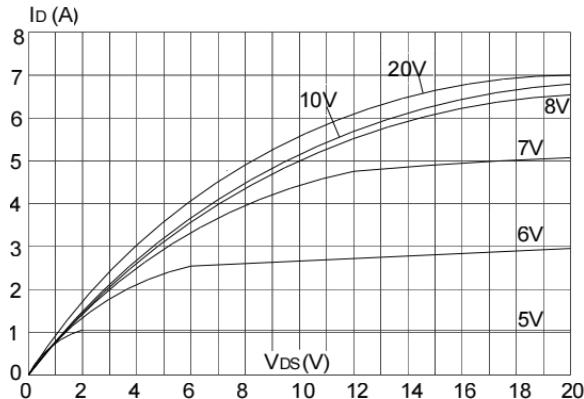
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	500	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 500\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Body Leakage Current	$V_{\text{GS}} = \pm 30\text{V}$	-	-	$\pm 100$	nA
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2	3	4	V
$R_{\text{DS}(\text{on})}$	Static Drain-Source On-Resistance note3	$V_{\text{GS}} = 10\text{V}, I_D = 2.5\text{A}$	-	1.35	1.6	$\Omega$
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0\text{MHz}$	-	462	-	pF
$C_{\text{oss}}$	Output Capacitance		-	54.2	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	8.8	-	pF
$Q_g$	Total Gate Charge	$V_{\text{DD}} = 400\text{V}, I_D = 5\text{A}, V_{\text{GS}} = 10\text{V}$	-	13.5	-	nC
$Q_{\text{gs}}$	Gate-Source Charge		-	2	-	nC
$Q_{\text{gd}}$	Gate-Drain("Miller") Charge		-	6	-	nC
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}} = 250\text{V}, I_D = 5\text{A}, R_G = 25\Omega$	-	10	-	ns
$t_r$	Turn-On Rise Time		-	25	-	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		-	40	-	ns
$t_f$	Turn-Off Fall Time		-	52	-	ns
$I_s$	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	A
$I_{\text{SM}}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
$V_{\text{SD}}$	Drain to Source Diode Forward Voltage	$V_{\text{GS}} = 0\text{V}, I_{\text{SD}} = 5\text{A}, T_J = 25^\circ\text{C}$	-	-	1.4	V
$t_{\text{rr}}$	Reverse Recovery Time	$V_{\text{GS}} = 0\text{V}, I_s = 5\text{A}, \frac{di}{dt} = 100\text{A}/\mu\text{s}$	-	220	-	ns
$Q_{\text{rr}}$	Reverse Recovery Charge		-	3	-	$\mu\text{C}$

Notes:

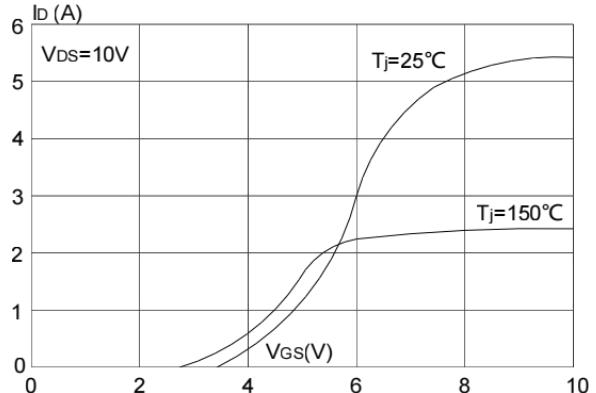
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{\text{AS}} = 3\text{A}, V_{\text{DD}} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 1\%$

## Typical Characteristics

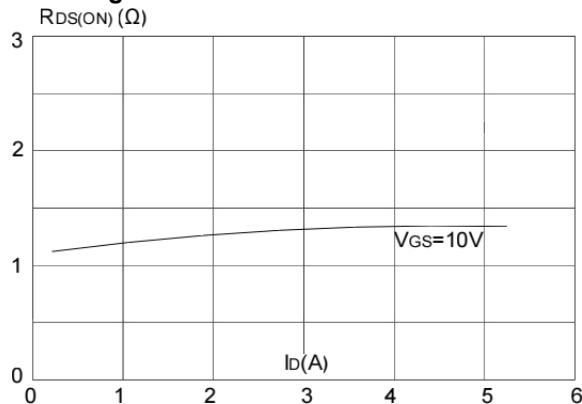
**Figure 1:** Output Characteristics



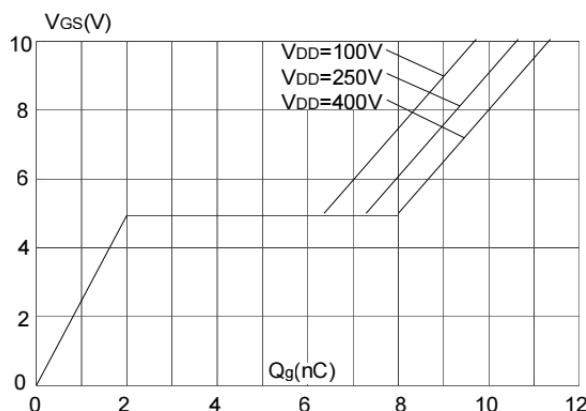
**Figure 2:** Typical Transfer Characteristics



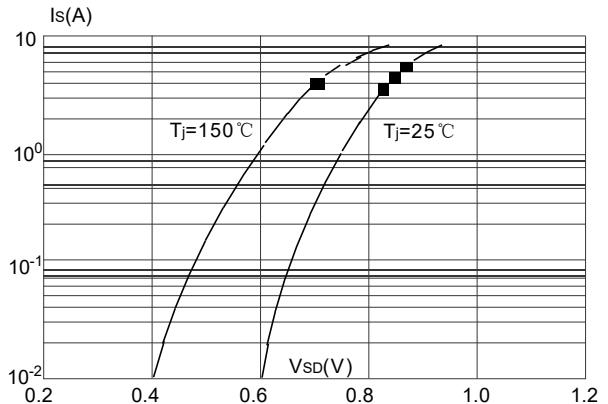
**Figure 3:** On-resistance vs. Drain Current



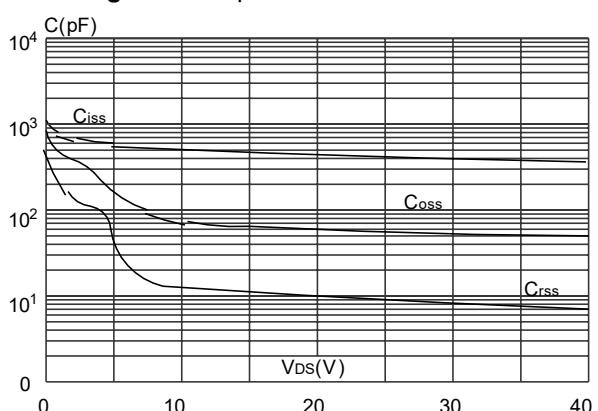
**Figure 5:** Gate Charge Characteristics



**Figure 4:** Body Diode Characteristics

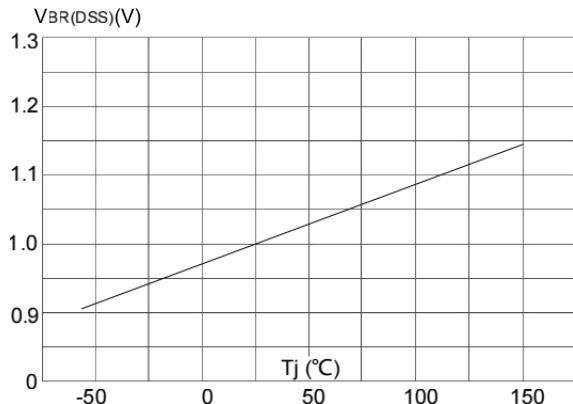


**Figure 6:** Capacitance Characteristics

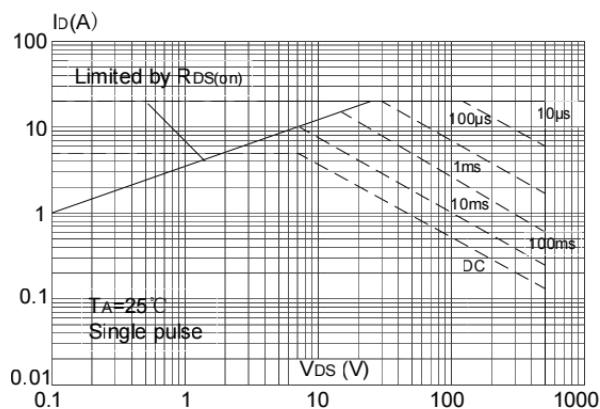


## Typical Characteristics

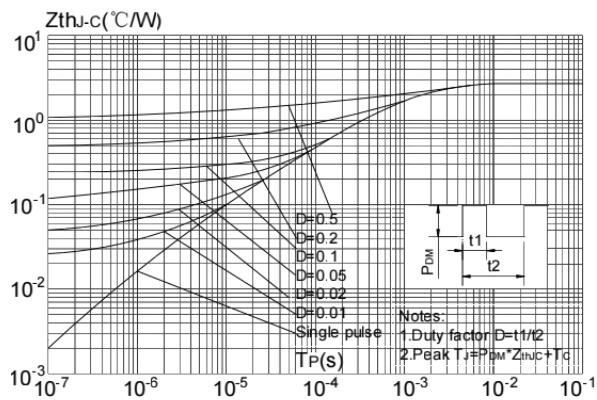
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



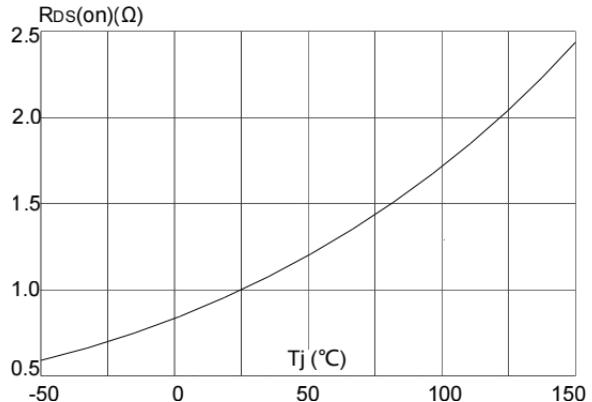
**Figure 9:** Maximum Safe Operating Area



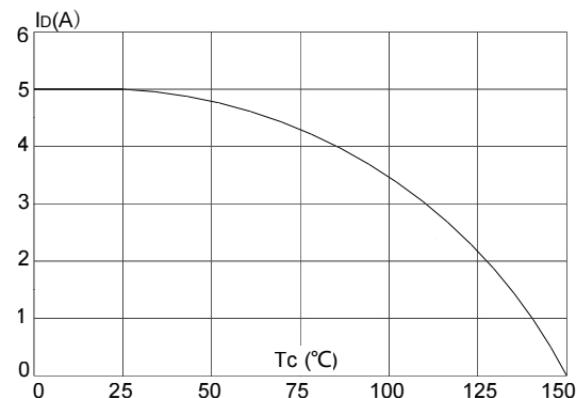
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



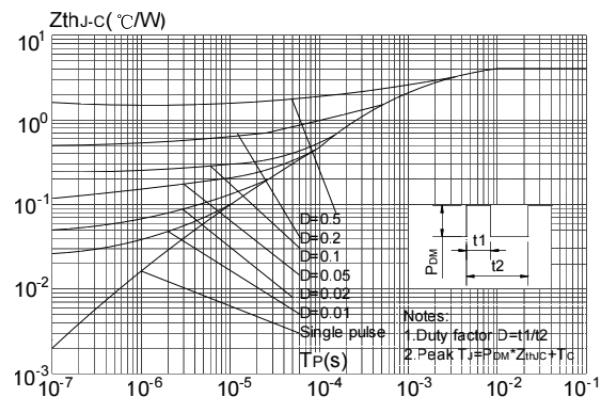
**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.12:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



### Typical Characteristics

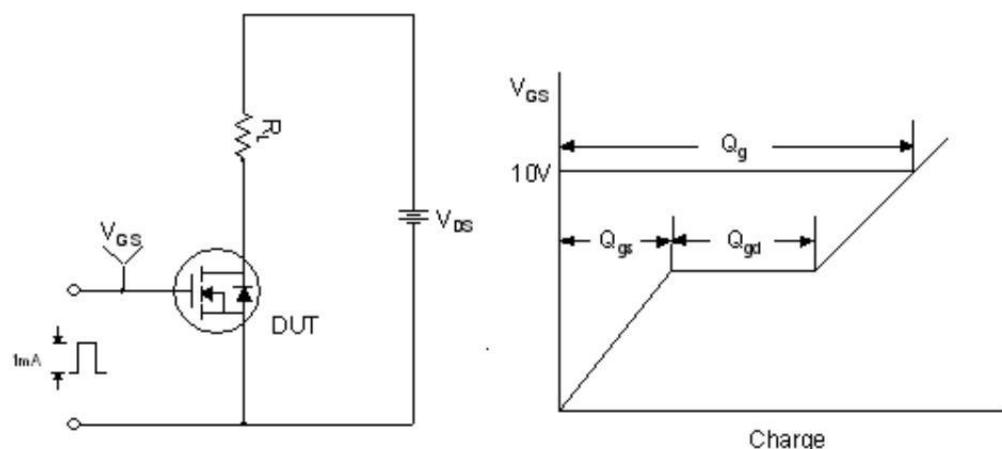


Figure 13. Gate Charge Test Circuit & Waveform

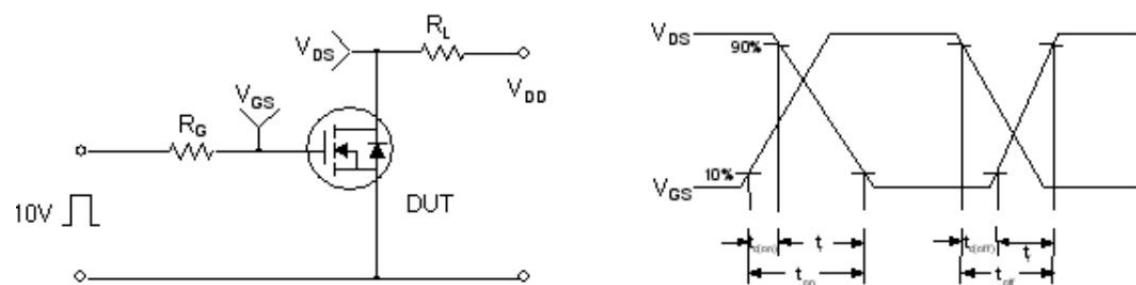


Figure 14. Resistive Switching Test Circuit & Waveforms

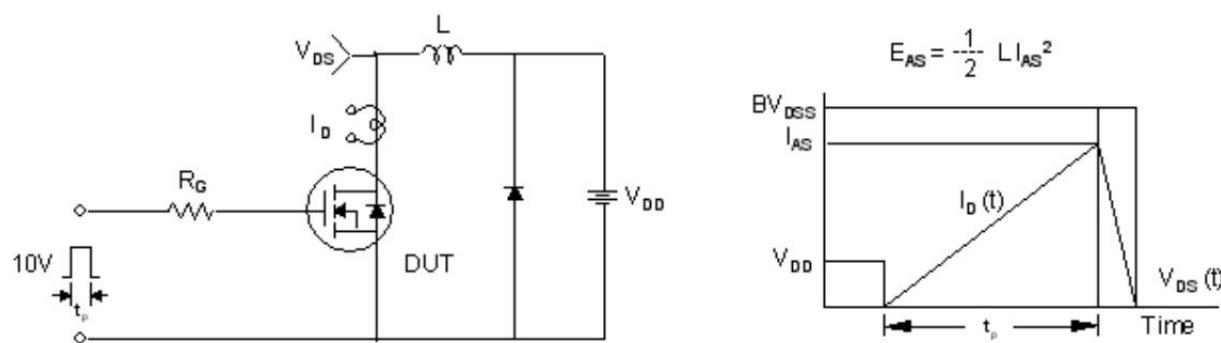


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

## Typical Characteristics

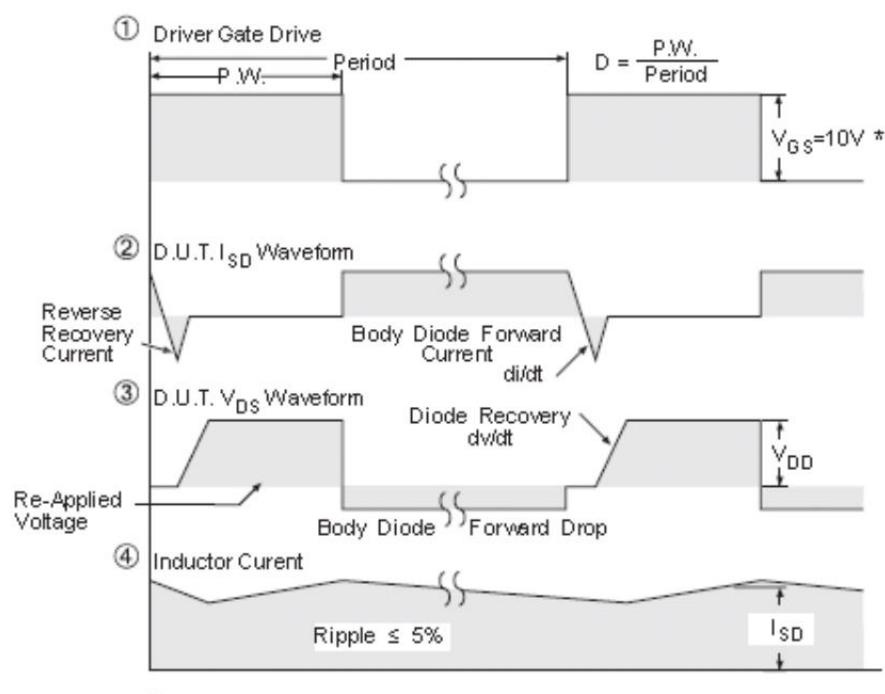
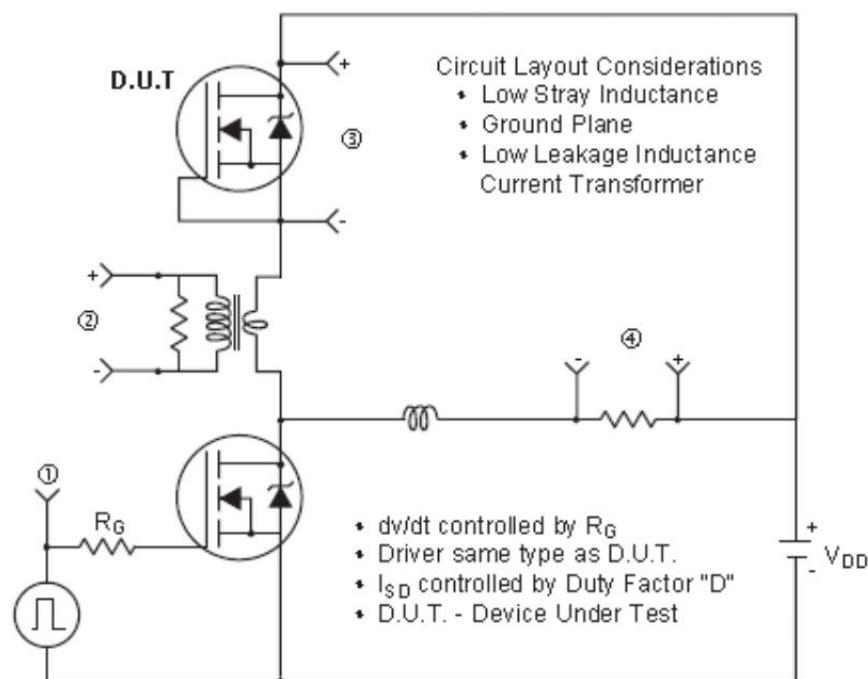
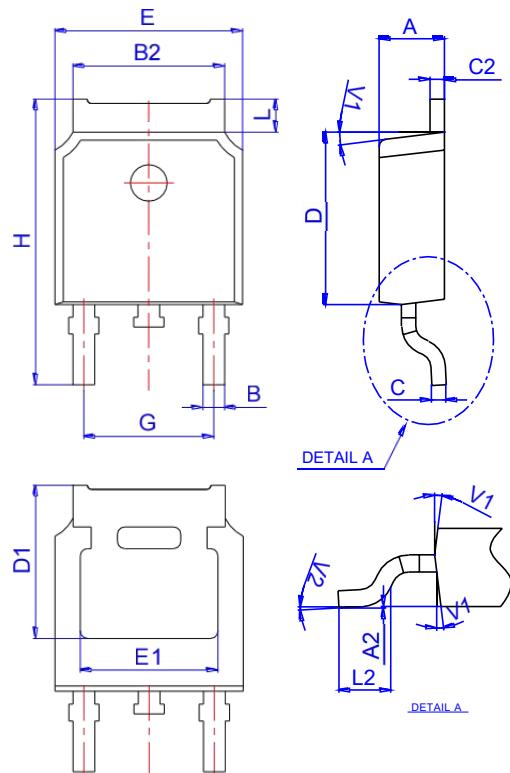


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)

## Package Mechanical Data : TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-252-3L		2500