

HN1J02FU-VB Datasheet

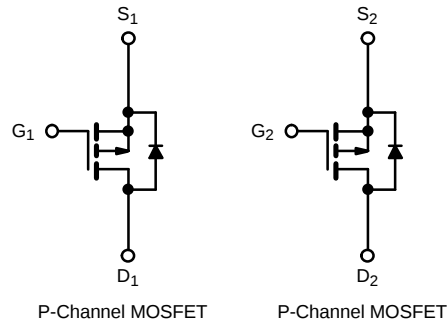
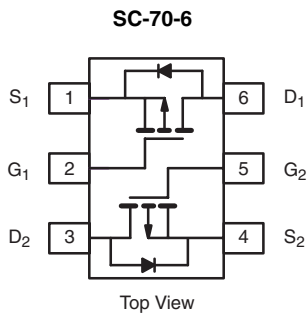
Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 20	0.155 at $V_{GS} = - 4.5V$	- 1.8	2.7 nC
	0.235 at $V_{GS} = - 2.5 V$	- 1.5	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT


ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$)	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	- 1.8	A
	$T_C = 70\text{ }^{\circ}\text{C}$		- 1.5	
	$T_A = 25\text{ }^{\circ}\text{C}$		- 1.6 ^{b, c}	
	$T_A = 70\text{ }^{\circ}\text{C}$		- 1.1 ^{b, c}	
Pulsed Drain Current		I_{DM}	- 2.5	
Continuous Source-Drain Diode Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_S	- 1.17	W
	$T_A = 25\text{ }^{\circ}\text{C}$		- 0.95 ^{b, c}	
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	1.4	
	$T_C = 70\text{ }^{\circ}\text{C}$		0.9	
	$T_A = 25\text{ }^{\circ}\text{C}$		1.14 ^{b, c}	
	$T_A = 70\text{ }^{\circ}\text{C}$		0.73 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 5\text{ s}$	R_{thJA}	93	110	$^{\circ}\text{C/W}$
Maximum Junction-to-Foot	Steady State	R_{thJF}	75	90	

Notes:

 a. $T_C = 25\text{ }^{\circ}\text{C}$.

b. Surface mounted on 1" x 1" FR4 board.

 c. $t = 5\text{ s}$.

 d. Maximum under steady state conditions is 150 $^{\circ}\text{C/W}$.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 17		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			3.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.5		- 1.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5V	- 8			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5V, I _D = - 2.5 A		0.155		Ω
		V _{GS} = - 2.5 V, I _D = - 1 A		0.235		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 2.6 A		5		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		210		pF
Output Capacitance	C _{oss}			45		
Reverse Transfer Capacitance	C _{rss}			33		
Total Gate Charge	Q _g	V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 2.6 A		5.2	8	nC
				2.7	4	
Gate-Source Charge	Q _{gs}	V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 2.6 A		0.94		
Gate-Drain Charge	Q _{gd}			1.3		
Gate Resistance	R _g	f = 1 MHz	2	7	14	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 7.1 Ω I _D ≅ - 2.1 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		39	59	ns
Rise Time	t _r			25	38	
Turn-Off Delay Time	t _{d(off)}			13	20	
Fall Time	t _f			9	18	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 7.1 Ω I _D ≅ - 2.1 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		5	10	
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			14	21	
Fall Time	t _f			7	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		1.17		A
Pulse Diode Forward Current	I _{SM}			8		
Body Diode Voltage	V _{SD}	I _S = - 2.1 A, V _{GS} = 0 V		0.85	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 2.1 A, dI/dt = 100 A/μs, T _J = 25 °C		13	20	ns
Body Diode Reverse Recovery Charge	Q _{rr}			6	12	nC
Reverse Recovery Fall Time	t _a			9		ns
Reverse Recovery Rise Time	t _b			4		

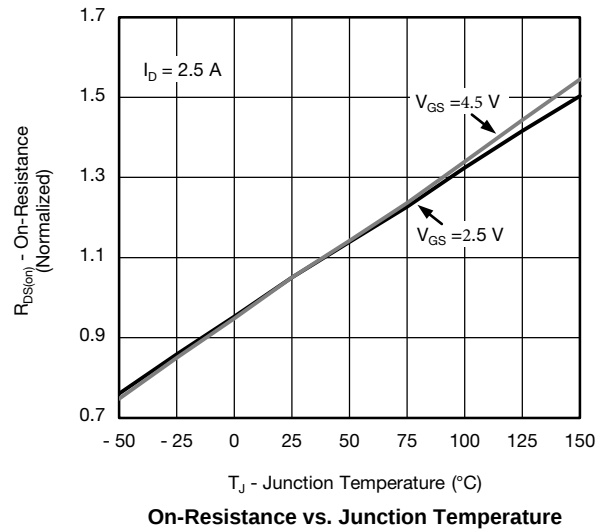
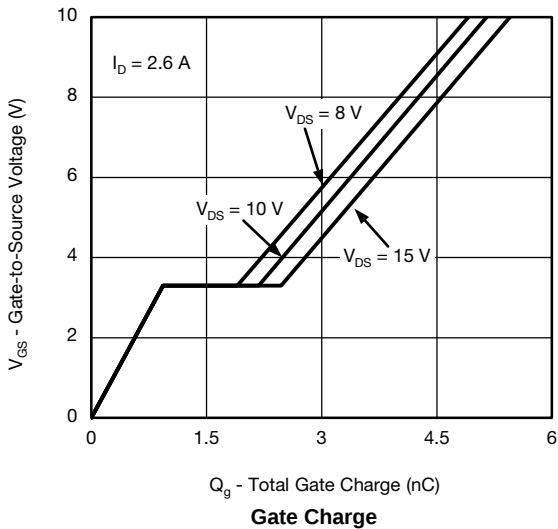
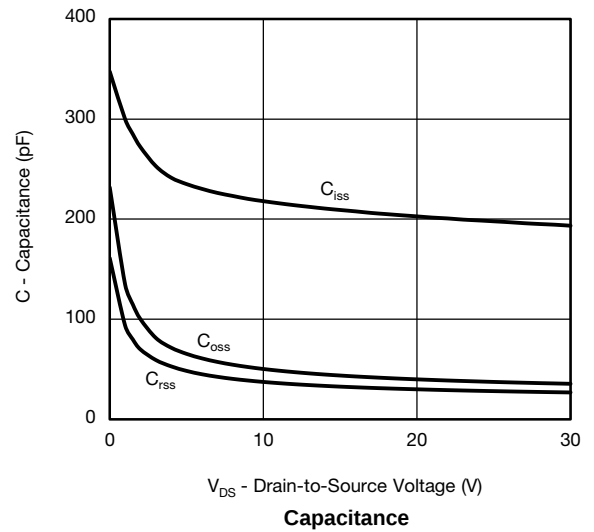
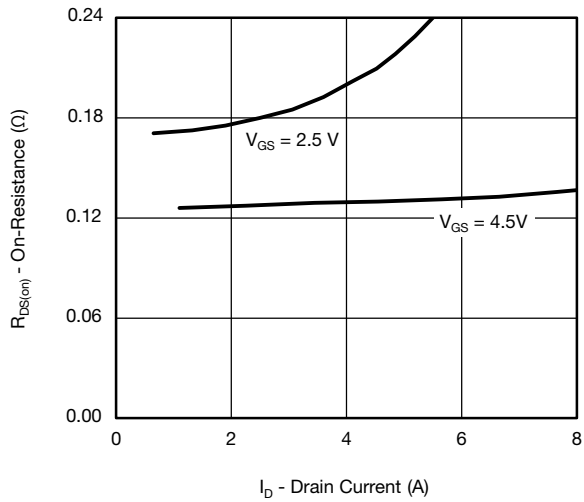
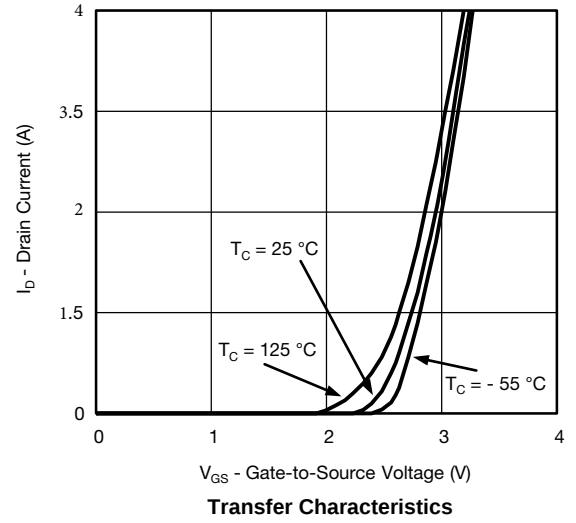
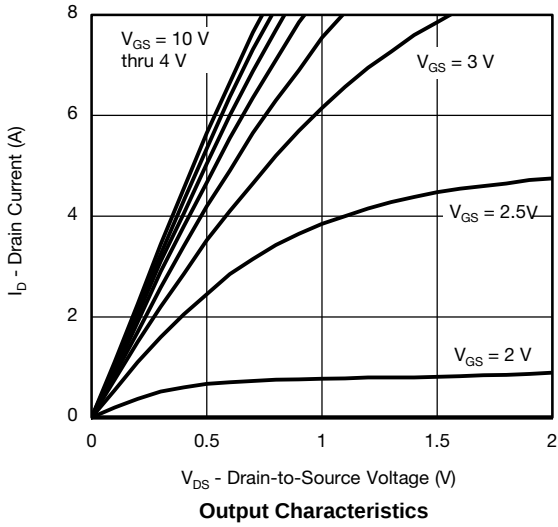
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

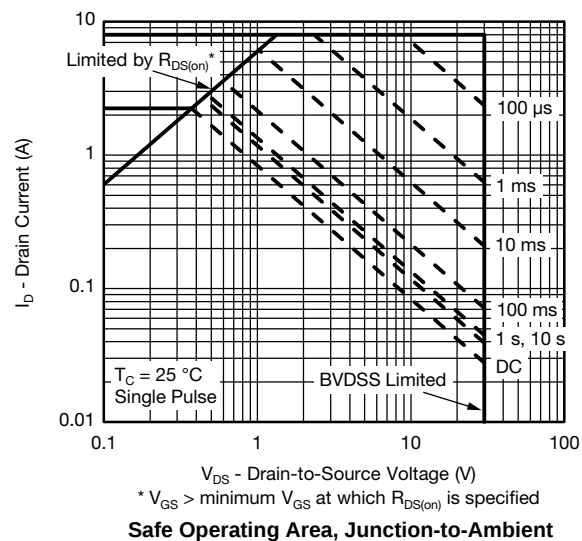
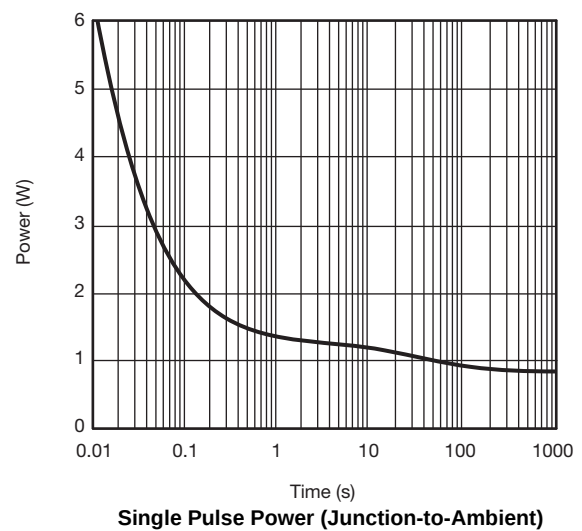
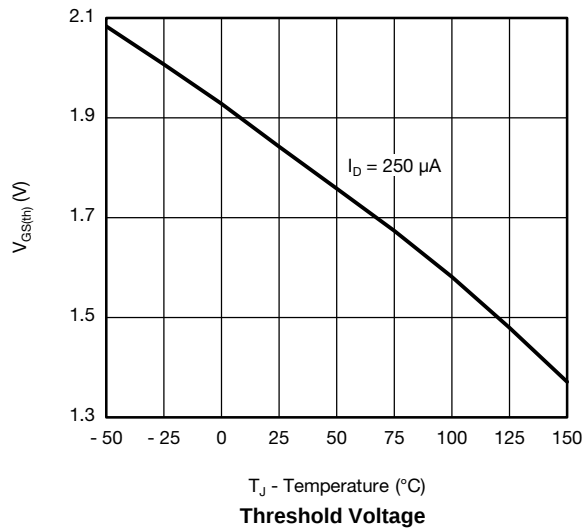
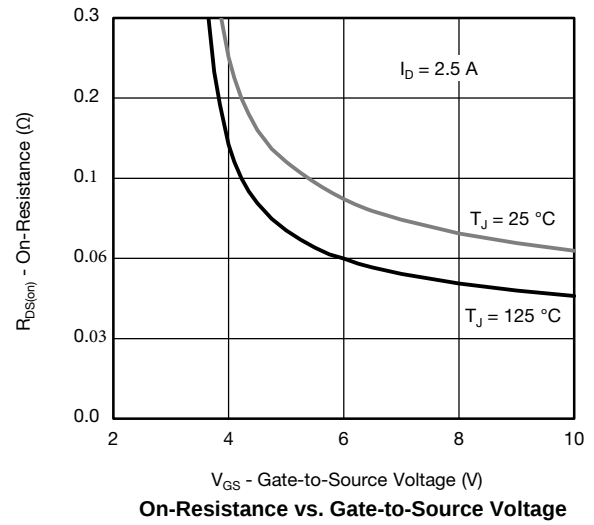
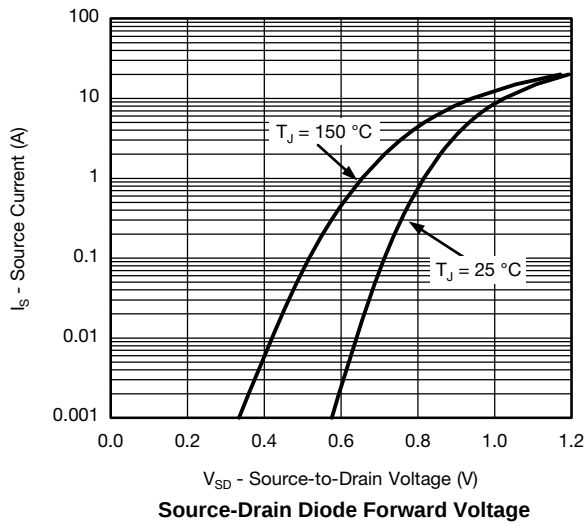
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

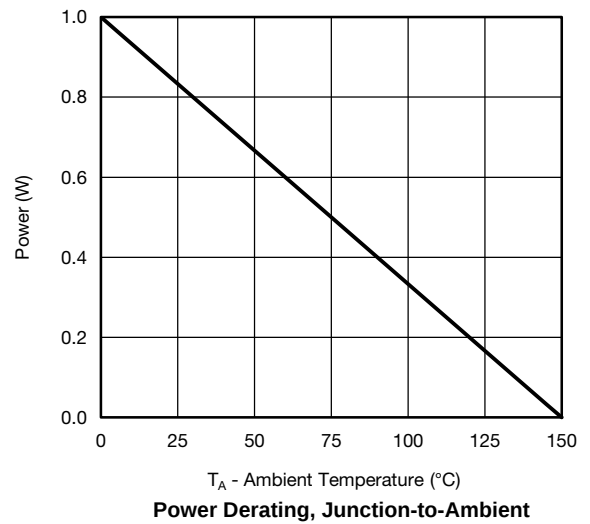
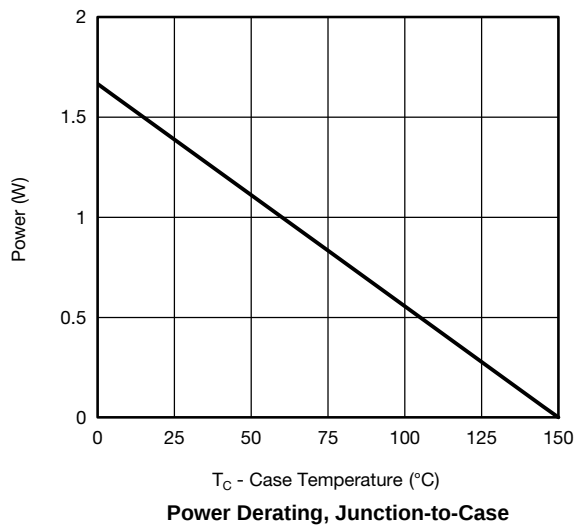
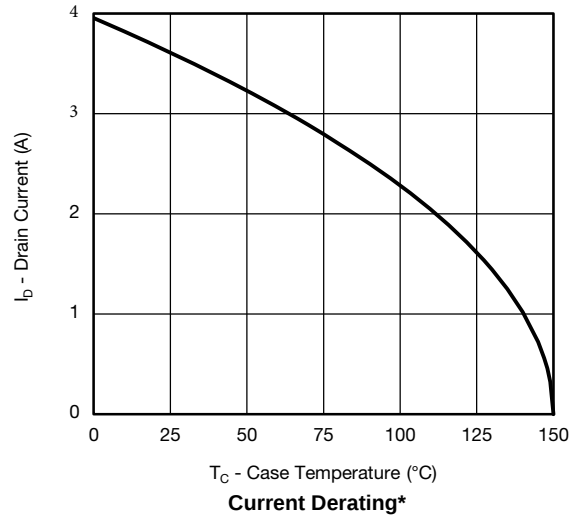
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



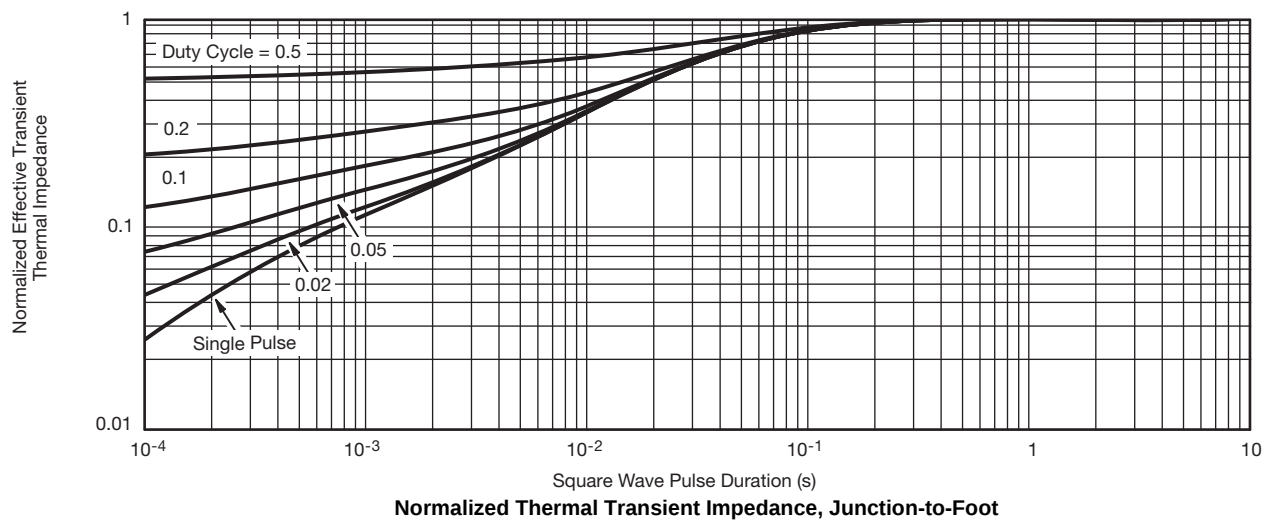
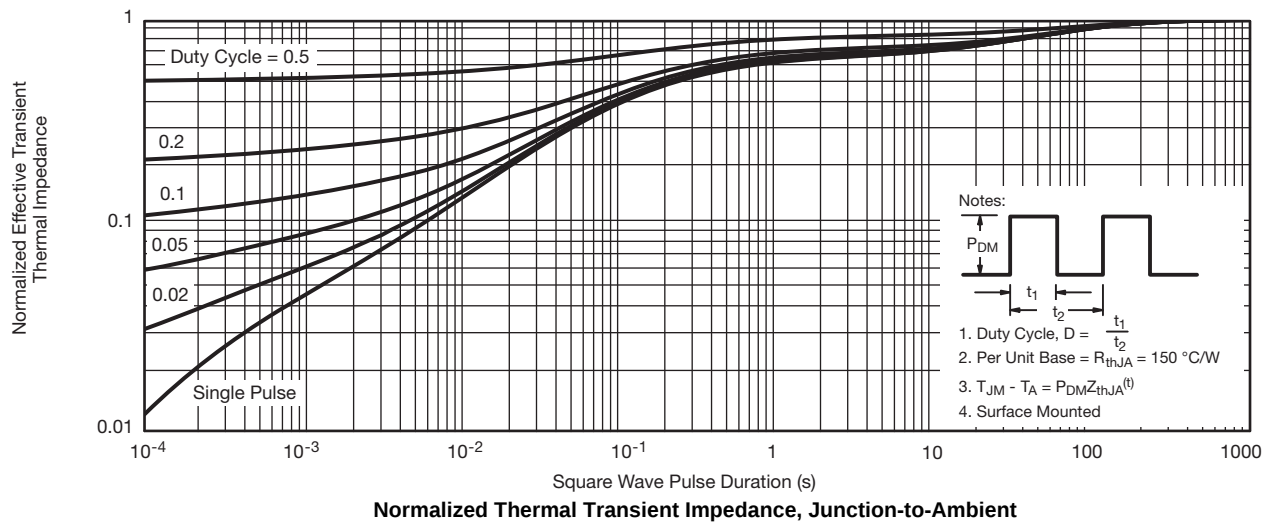
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* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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