Description

The SXJ50N65D protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, low operating voltage. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.

General Features

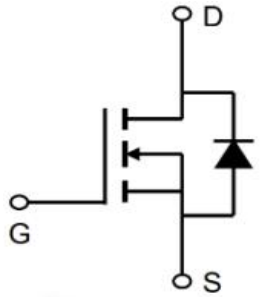
V_{DS} = 650V （Type：740V） IDM =50A

$R_{DS(ON)}$ < 190mΩ @ V_{GS}=10V

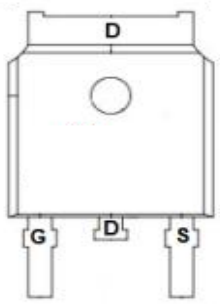
Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



TO-252-3L



Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	650	V
ID	Continuous Drain Current	21	A
IDM	Pulsed Drain Current (note1)	50	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	500	mJ
P_D	Power Dissipation (T_C = 25ºC)	151	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	0.82	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	62	ºC/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650	740	--	V
ΔBV_{DSS} / ΔTJ	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		V_{DS}=520V, T_C=125°C	--	--	50	uA
IGSS	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2.5	3.3	4.5	V
RDS(ON)	Drain to source on state resistance	V_{GS}=10V, I_D =3.2A	--	150	190	mΩ
Ciss	Input capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz	--	1510	--	pF
Coss	Output capacitance		--	65	--	
Crss	Reverse transfer capacitance		--	2.4	--	
td(on)	Turn on delay time	V_{DS}=400V, I_D=13A, R_G=4.7Ω , V_{GS}=13V	--	10	--	ns
tr	Rising time		--	19.8	--	
td(off)	Turn off delay time		--	45.4	--	
t_f	Fall time		--	41.4	--	
Q_g	Total gate charge	V_{DS}=480V, V_{GS}=10V, I_D=11A	--	7.27		nC
Q_{gs}	Gate-source charge		--	17.4	--	
Q_{gd}	Gate-drain charge		--	43.9	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	21	A
ISM	Pulsed source current		--	--	63	A
VSD	Diode forward voltage drop.	I_S=7.3A, V_{GS}=0V	--	0.812	1.5	V
T_{rr}	Reverse recovery time	I_S=11A, V_{GS}=0V, Vdd=400V, dI_F/dt=100A/us,	--	288	--	ns
Qrr	Reverse recovery Charge		--	3.66	--	uC

Note：

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . L=0.5mH, IAS =7A, VDD =50V, RG=25Ω

3、The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD≤ BVDSS, Starting at TJ =25℃

4、The power dissipation is limited by 150℃junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

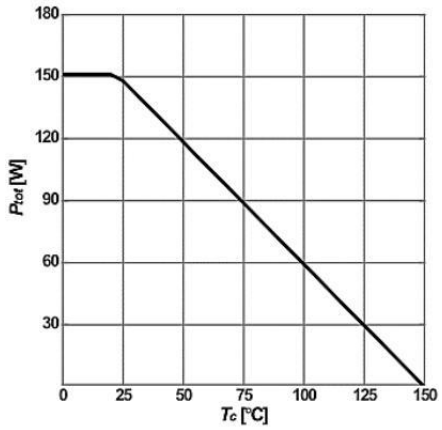


Figure1: Power dissipation (Non FullPAK)

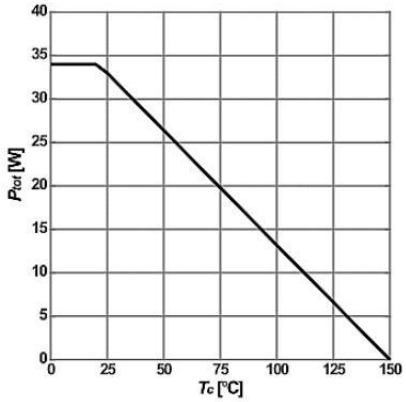


Figure2: Power dissipation (FullPAK)

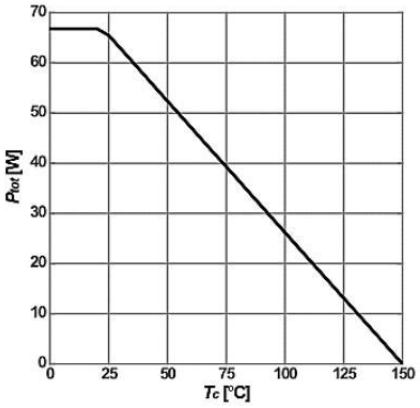


Figure3: Power dissipation
pot=f(TC)

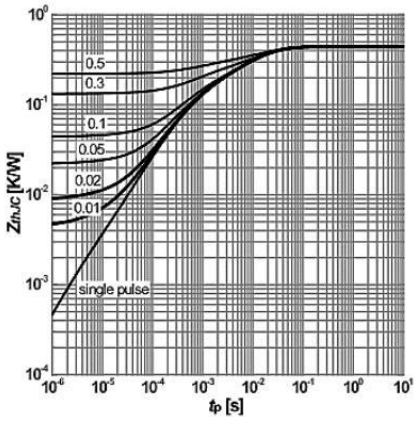


Figure4:Max. transient thermal impedance
zn. c=f(tp);parameter:D=t pT

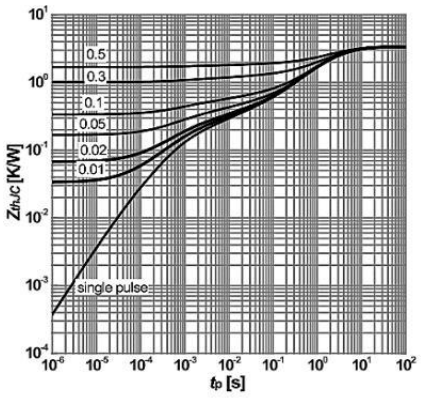


Figure5: Max. transient thermal impedance
zinJ C=f(tp); parameter:D=tp/T

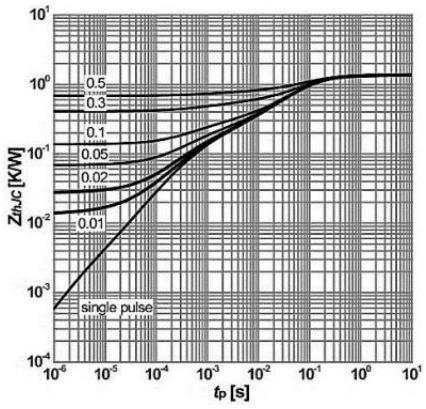


Figure6: Max. transient thermal impedance
zinJ C=f(tp); parameter:D=tp/T

Typical Characteristics

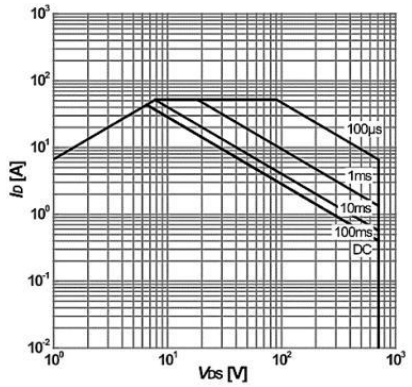


Figure 7: Safe operating area (Non FullPAK)
lo=f(vos);T=25c;D=0;parameter:t,

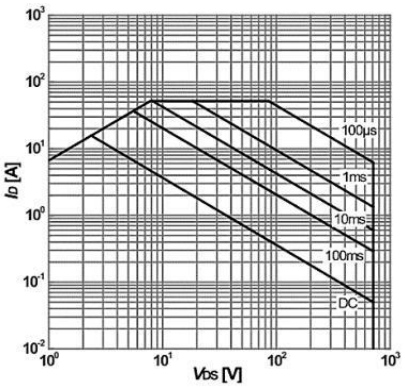


Figure8 : Safe operating area (Non FullPAK)
lo=f(vos);T=25c;D=0;parameter:t,

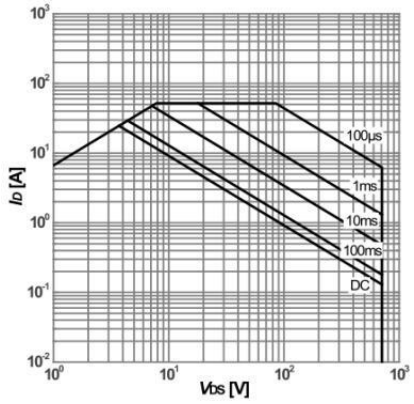


Figure9 : TSafe operating area (FullPAK-TO220A)
ROS(on)=f(o);ᒧ=25"c;parameter: vos

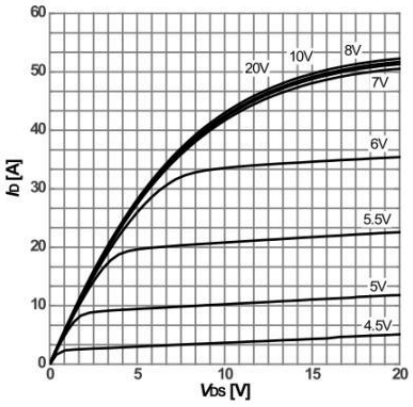


Figure 10: Typ. output characteristics
ROS(on)=f(T);lo=3.2A;vas=10v

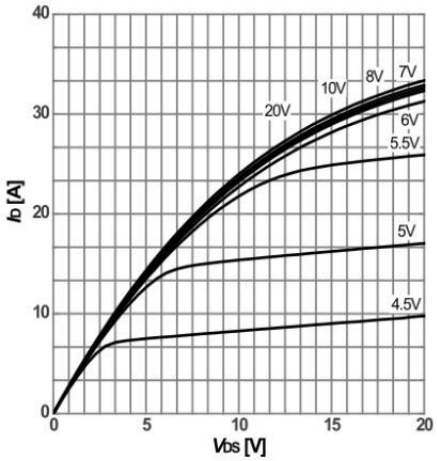


Figure 11: Typ. output characteristics
lo=f(vos);T-125c;parameter: ves

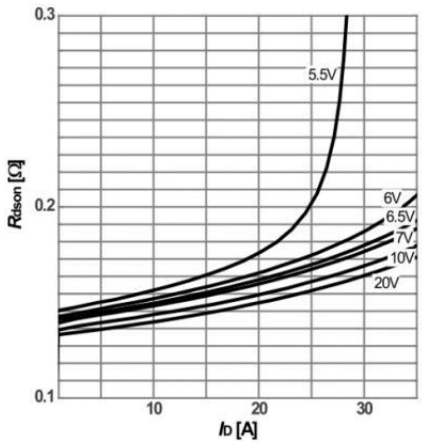
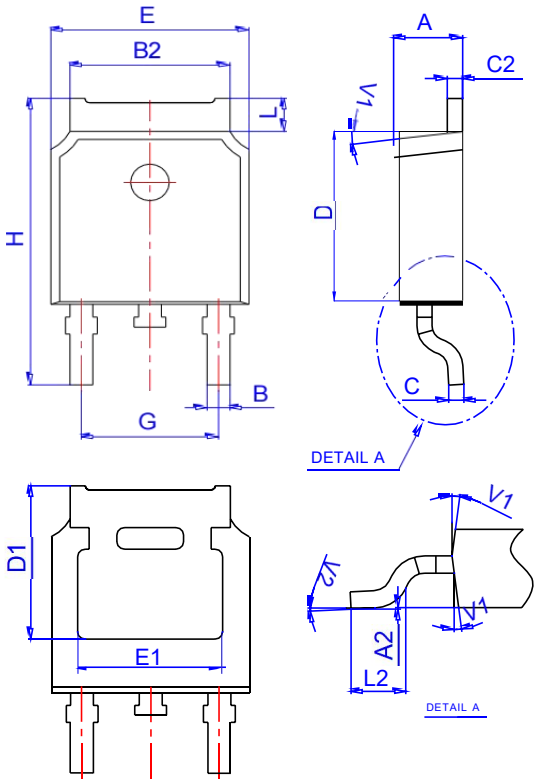


Figure 12: Type. gate charge
ROS(on)=f(/o);T=25c;parameter :vas

Package Mechanical Data:TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-252-3L		2500