

General Description

These N-channel Logic Level MOSFETS has been especially tailored to minimize the on-state resistance and yet maintains superior switching performance these devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required

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Features

- $V_{DS(V)} = 40V$
- $I_D = 6A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 29m\Omega$ ($V_{GS}=10V$)
- $R_{DS(ON)} < 36m\Omega$ ($V_{GS}=4.5V$)
- Low gate charge
- RoHS compliant
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

Applications

- Inverter
- Power suppliers

MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous (Note 1a)	6	A
	-Pulsed	20	
E_{AS}	Drain-Source Avalanche Energy (Note 3)	26	mJ
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Characteristics

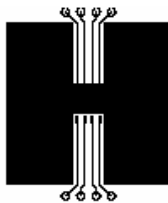
$R_{\theta JA}$	Thermal Resistance-Single operation, Junction to Ambient (Note 1a)	81	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance-Single operation, Junction to Ambient (Note 1b)	135	
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	40	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

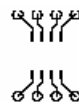
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		33		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}$, $V_{GS} = 0\text{V}$			1	μA
		$T_J = 55^\circ\text{C}$			10	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$			± 100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-4.6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 6\text{A}$		21	29	m Ω
		$V_{GS} = 4.5\text{V}$, $I_D = 4.5\text{A}$		26	36	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}$, $I_D = 6\text{A}$		22		S
C_{iss}	Input Capacitance	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		715	955	pF
C_{oss}	Output Capacitance			105	140	pF
C_{rss}	Reverse Transfer Capacitance			60	90	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		1.1		Ω
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}$, $I_D = 1\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$		9	18	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	37	ns
t_f	Fall Time			3	6	ns
Q_g	Total Gate Charge	$V_{DS} = 20\text{V}$, $I_D = 6\text{A}$, $V_{GS} = 5\text{V}$		7.7	11	nC
Q_{gs}	Gate to Source Gate Charge			2.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.8		nC
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = 6\text{A}$ (note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time (note 3)	$I_F = 6\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$		17	26	ns
Q_{rr}	Reverse Recovery Charge			7	11	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) $81^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper



b) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1:1 on letter size paper

2: Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$.

3: Starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $I_{AS} = 7.3\text{A}$, $V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

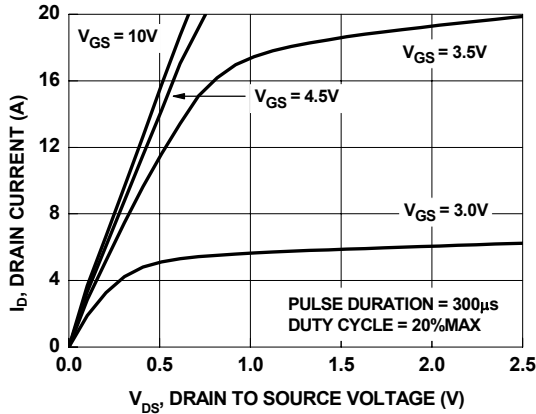


Figure 1. On Region Characteristics

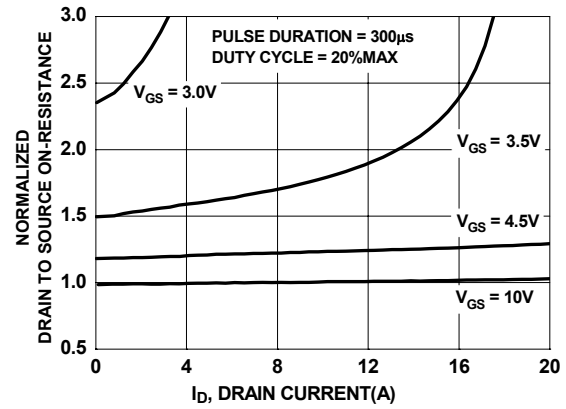


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

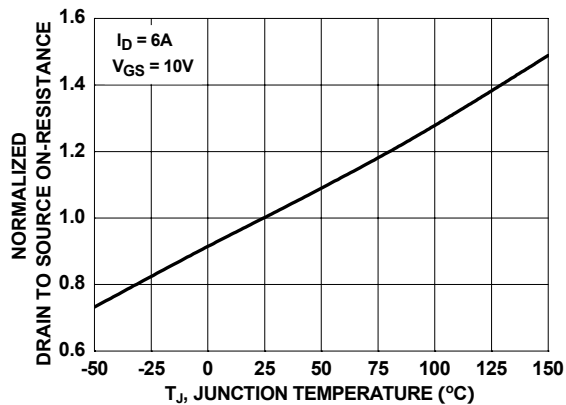


Figure 3. Normalized On Resistance vs Junction Temperature

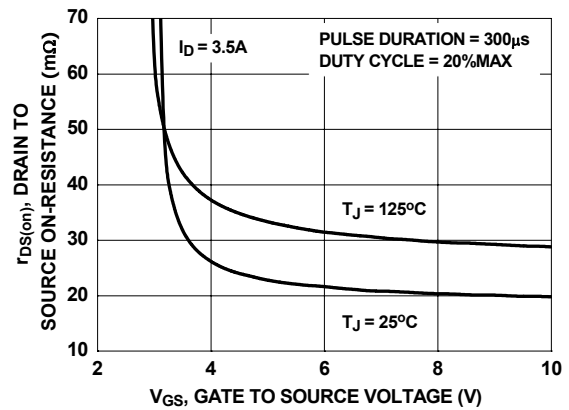


Figure 4. On-Resistance vs Gate to Source Voltage

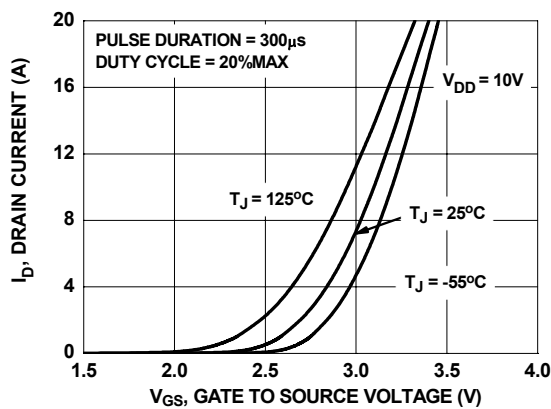


Figure 5. Transfer Characteristics

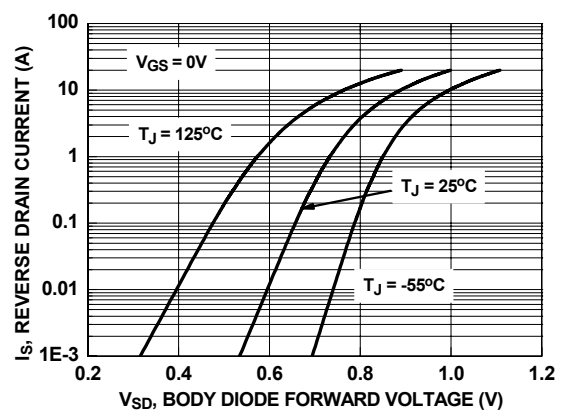


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

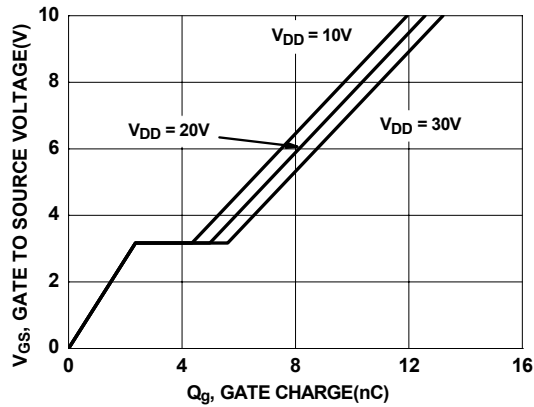


Figure 7. Gate Charge Characteristics

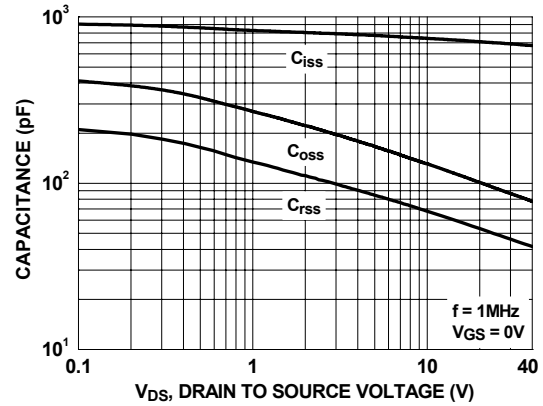


Figure 8. Capacitance vs Drain to Source Voltage

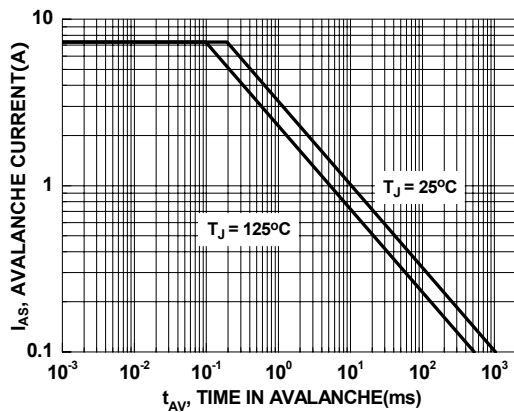


Figure 9. Unclamped Inductive Switching Capability

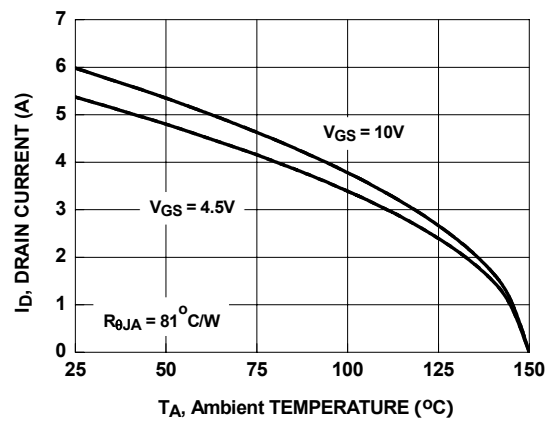


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

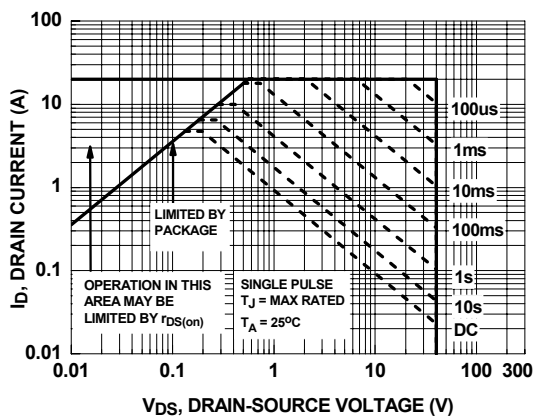


Figure 11. Forward Bias Safe Operating Area

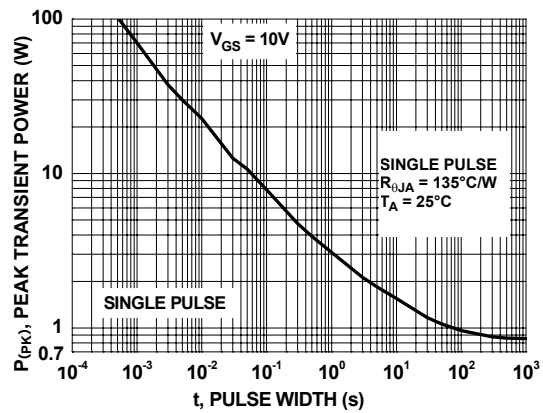
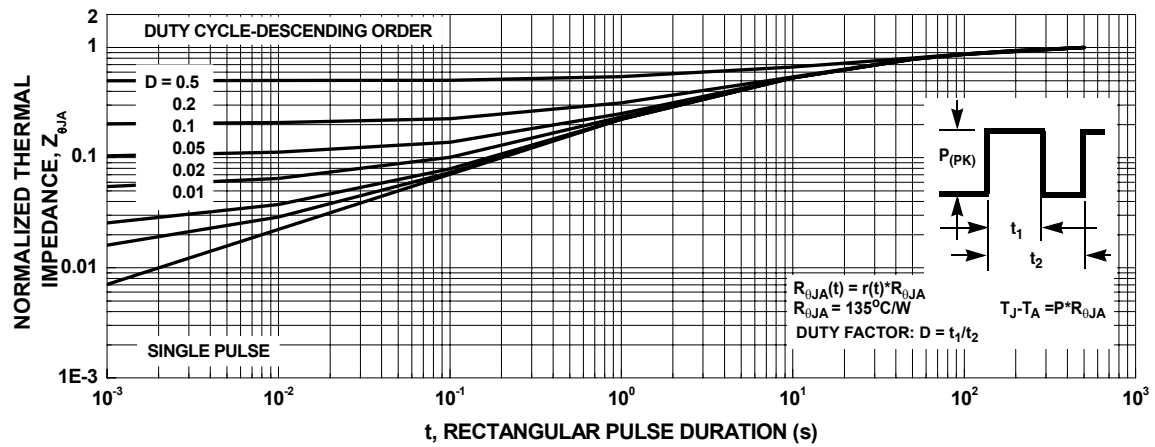


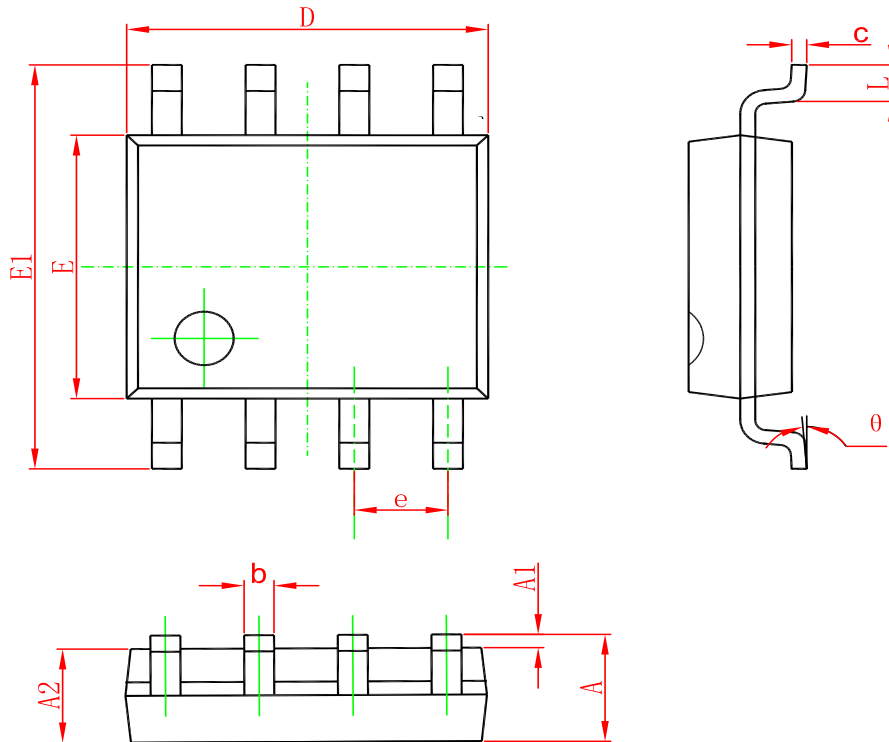
Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



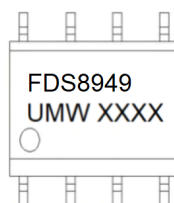
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDS8949	SOP-8	3000	Tape and reel