

## P-Channel Enhancement-Mode Vertical DMOS FET

### Features

- High Input Impedance and High Gain
- Low-Power Drive Requirement
- Ease of Paralleling
- Low  $C_{ISS}$  and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- Free from Secondary Breakdown

### Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Analog Switches
- Power Management
- Telecommunication Switches

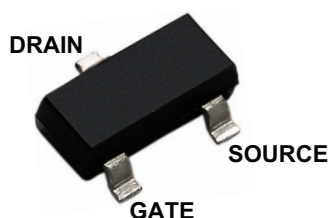
### General Description

The TP5335 is a low-threshold, Enhancement-mode (normally-off) transistor that utilizes an advanced vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. The characteristic of all MOS structures is that this device is free from thermal runaway and thermally induced secondary breakdown.

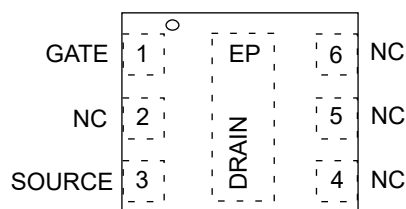
Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Type

**3-lead SOT-23**  
(Top view)



**6-lead DFN**  
(Top view)



See [Table 2-1](#) for pin information.

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings<sup>(†)</sup>

Drain-to-Source Voltage .....	$BV_{DSS}$
Drain-to-Gate Voltage .....	$BV_{DGS}$
Gate-to-Source Voltage .....	$\pm 20V$
Junction Temperature, $T_J$ .....	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, $T_S$ .....	$-55^{\circ}C$ to $+150^{\circ}C$
ESD Protection (HBM) TP5335MF-G	
Drain-to-Source .....	$\pm 6$ kV
Gate-to-Drain .....	$+500V$
Gate-to-Source .....	$<\pm 250V$
ESD Protection (CDM) TP5335MF-G .....	1 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS – COMMERCIAL

**Electrical Specifications:**  $T_A = T_J = 25^{\circ}C$  unless otherwise specified. All DC parameters are 100% tested at  $25^{\circ}C$  unless otherwise stated. (Pulse test: 300  $\mu s$  pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	$BV_{DSS}$	-350	—	—	V	$V_{GS} = 0V$ , $I_D = -100 \mu A$
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	-2.4	V	$V_{DS} = V_{GS}$ , $I_D = -1$ mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/ $^{\circ}C$	$V_{DS} = V_{GS}$ , $I_D = -1$ mA ( <b>Note 1</b> )
Gate Body Leakage	$I_{GSS}$	—	—	-100	nA	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$
Zero-Gate Voltage Drain Current	$I_{DSS}$	—	—	-10	$\mu A$	$V_{DS} = \text{Maximum rating}$ , $V_{GS} = 0V$
		—	—	-1	mA	$V_{DS} = \text{Maximum rating}$ , $V_{GS} = 0V$ , $T_A = 125^{\circ}C$ ( <b>Note 1</b> )
On-State Drain Current	$I_{D(ON)}$	-200	—	—	mA	$V_{GS} = -4.5V$ , $V_{DS} = -25V$
		-400	—	—	mA	$V_{GS} = -10V$ , $V_{DS} = -25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	75	$\Omega$	$V_{GS} = -4.5V$ , $I_D = -150$ mA
		—	—	30	$\Omega$	$V_{GS} = -10V$ , $I_D = -200$ mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.7	%/ $^{\circ}C$	$V_{GS} = -10V$ , $I_D = -200$ mA ( <b>Note 1</b> )

**Note 1:** Specification is obtained by characterization and is not 100% tested.

### DC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE

**Electrical Specifications:** Boldface specification limits apply over the full operating temperature range of  $T_A = T_J = -55^{\circ}C$ ,  $25^{\circ}C$ , and  $150^{\circ}C$  unless otherwise specified. Non-boldfaced specification limits apply only to  $T_A = T_J = 25^{\circ}C$  unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise specified. (Pulse test: 300  $\mu s$  pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	$BV_{DSS}$	<b>-350</b>	—	—	V	$V_{GS} = 0V$ , $I_D = -100 \mu A$

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## DC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE (CONTINUED)

**Electrical Specifications:** Boldface specification limits apply over the full operating temperature range of  $T_A = T_J = -55^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ , and  $150^{\circ}\text{C}$  unless otherwise specified. Non-boldfaced specification limits apply only to  $T_A = T_J = 25^{\circ}\text{C}$  unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise specified. (Pulse test: 300  $\mu\text{s}$  pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	<b>-2.4</b>	V	$V_{DS} = V_{GS}$ , $I_D = -1\text{ mA}$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	3.3	—	mV/ $^{\circ}\text{C}$	$V_{DS} = V_{GS}$ , $I_D = -1\text{ mA}$ (Note 1)
Gate Body Leakage	$I_{GSS}$	—	—	-100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
		—	—	<b>-220</b>	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
Zero-Gate Voltage Drain Current	$I_{DSS}$	—	—	-10	$\mu\text{A}$	$V_{DS} = \text{Maximum rating}$ , $V_{GS} = 0\text{V}$
		—	—	<b>-1</b>	mA	$V_{DS} = \text{Maximum rating}$ , $V_{GS} = 0\text{V}$
On-State Drain Current	$I_{D(ON)}$	<b>-200</b>	—	—	mA	$V_{GS} = -4.5\text{V}$ , $V_{DS} = -25\text{V}$
		-400	—	—	mA	$V_{GS} = -10\text{V}$ , $V_{DS} = -25\text{V}$
		<b>-375</b>	—	—	mA	$V_{GS} = -10\text{V}$ , $V_{DS} = -25\text{V}$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	<b>75</b>	$\Omega$	$V_{GS} = -4.5\text{V}$ , $I_D = -150\text{ mA}$
		—	—	30	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -200\text{ mA}$
		—	—	<b>70</b>	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -200\text{ mA}$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	1	—	%/ $^{\circ}\text{C}$	$V_{GS} = -10\text{V}$ , $I_D = -200\text{ mA}$ (Note 1)

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## AC ELECTRICAL CHARACTERISTICS – COMMERCIAL

**Electrical Specifications:**  $T_A = T_J = 25^{\circ}\text{C}$  unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G <sub>FS</sub>	125	—	—	mmho	V <sub>DS</sub> = -25V, I <sub>D</sub> = -200 mA
Input Capacitance	C <sub>ISS</sub>	—	—	110	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V, f = 1 MHz
Common Source Output Capacitance	C <sub>OSS</sub>	—	—	60	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	—	22	pF	
Turn-On Delay Time	t <sub>d(ON)</sub>	—	—	20	ns	V <sub>DD</sub> = -25V, I <sub>D</sub> = -150 mA, R <sub>GEN</sub> = 25Ω
Rise Time	t <sub>r</sub>	—	—	15	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	—	—	25	ns	
Fall Time	t <sub>f</sub>	—	—	25	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V <sub>SD</sub>	—	—	-1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -200 mA (Note 1)
Reverse Recovery Time	t <sub>rr</sub>	—	800	—	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -200 mA

**Note 1:** All DC parameters are 100% tested at  $25^{\circ}\text{C}$  unless otherwise stated. (Pulse test: 300  $\mu\text{s}$  pulse, 2% duty cycle.)

## AC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE

**Electrical Specifications:**  $T_A = T_J = 25^\circ\text{C}$  unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G <sub>FS</sub>	—	285	—	mmho	V <sub>DS</sub> = -25V, I <sub>D</sub> = -200 mA
Input Capacitance	C <sub>ISS</sub>	—	80	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V, f = 1 MHz
Common Source Output Capacitance	C <sub>OSS</sub>	—	12	—	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	2	—	pF	
Turn-On Delay Time	t <sub>d(ON)</sub>	—	7.6	—	ns	V <sub>DD</sub> = -25V, I <sub>D</sub> = -150 mA, R <sub>GEN</sub> = 25Ω
Rise Time	t <sub>r</sub>	—	3	—	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	—	19	—	ns	
Fall Time	t <sub>f</sub>	—	10	—	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V <sub>SD</sub>	—	—	-1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -200 mA (Note 1)
Reverse Recovery Time	t <sub>rr</sub>	—	450	—	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -200 mA

**Note 1:** 100% Production Tested at  $T_A = T_J = (-55^\circ\text{C}, 25^\circ\text{C}, \text{ and } 150^\circ\text{C})$ .

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Junction Temperature	$T_J$	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	$T_S$	-55	—	+150	$^\circ\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
3-lead SOT-23	$\theta_{JA}$	—	203	—	$^\circ\text{C/W}$	
6-lead DFN	$\theta_{JA}$	—	102	—	$^\circ\text{C/W}$	

## THERMAL CHARACTERISTICS

Package	$I_D$ ( <b>Note 1</b> ) (Continuous) (mA)	$I_D$ (Pulsed) (mA)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	$I_{DR}$ ( <b>Note 1</b> ) (mA)	$I_{DRM}$ (mA)
3-lead SOT-23	-85	-400	0.36	-85	-400

**Note 1:**  $I_D$  (continuous) is limited by maximum  $T_J$ .

## 2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in TP5335 SOT-23. Refer to [Package Type](#) for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number 3-Lead SOT-23	Pin Number 6-Lead DFN	Pin Name	Description
1	1	Gate	Gate
2	3	Source	Source
—	2	NC	Not Connected
3	4, 5, 6	NC	Not Connected. It is recommended to connect to drain.
—	EP	Drain	Drain

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 illustrates the switching waveforms and test circuit for TP5335.

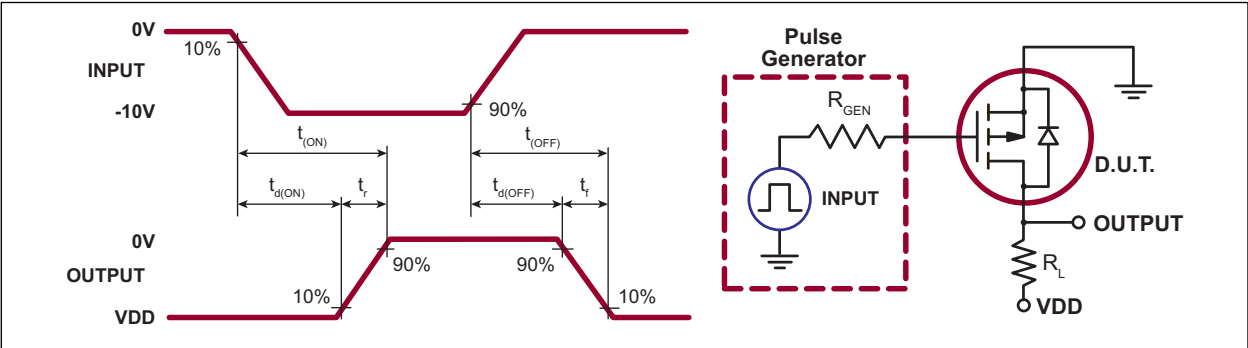


FIGURE 3-1: Switching Waveforms and Test Circuit.

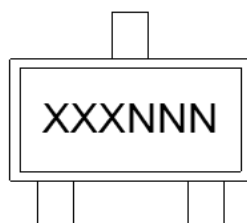
TABLE 3-1: PRODUCT SUMMARY

$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (Maximum) ( $\Omega$ )	$V_{GS(th)}$ (Maximum) (V)
-350	30	-2.4

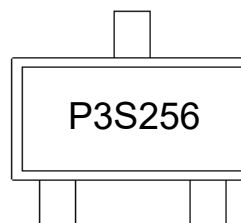
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

3-Lead SOT-23  
(2.90 mm x 1.30 mm)



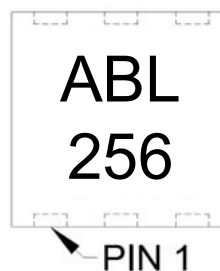
Example



6-Lead DFN  
(2 mm x 2 mm)



Example

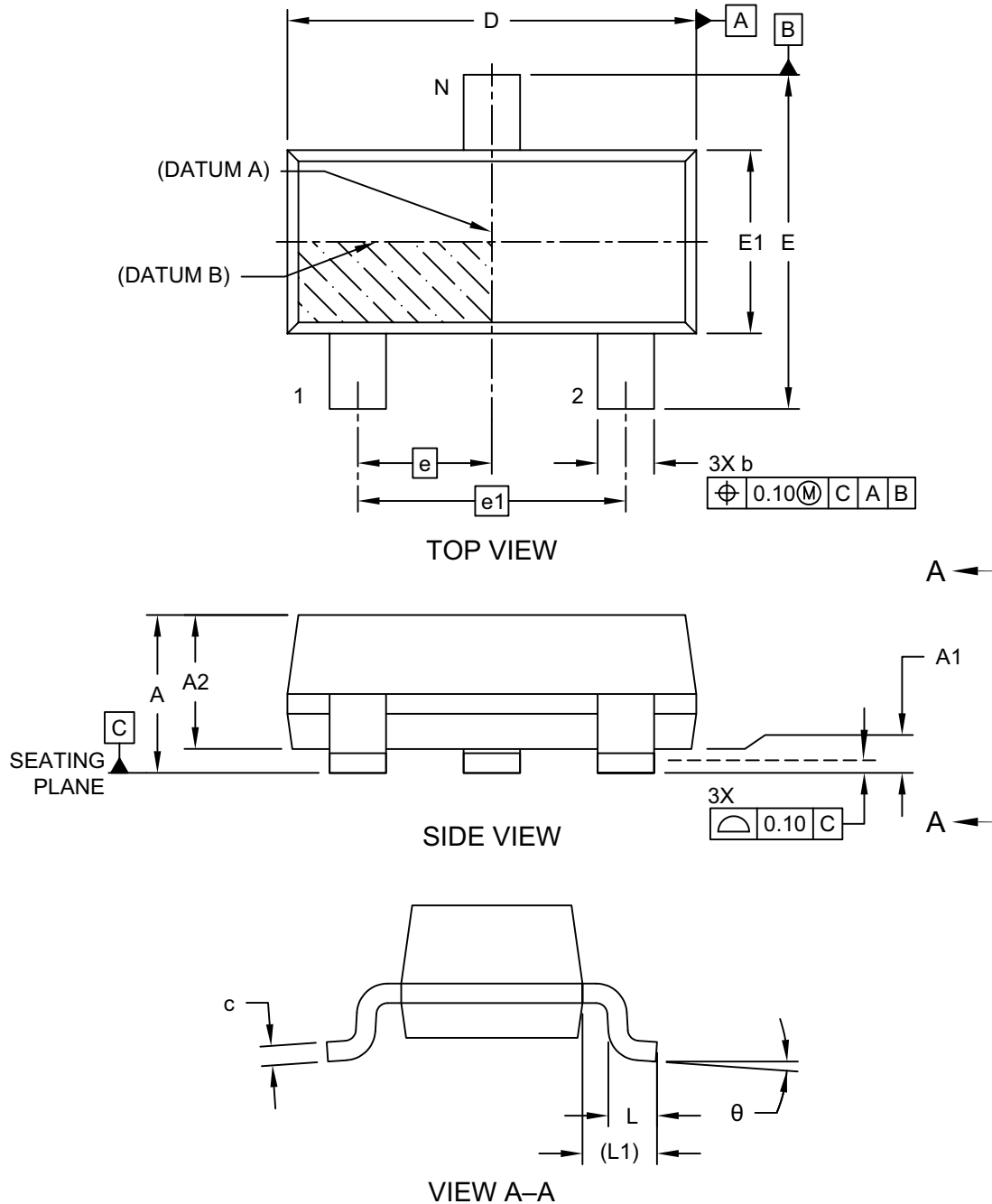


<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

## 3-Lead Small Outline Transistor (C6X) - [SOT-23] Supertex Legacy Package (K1/T)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

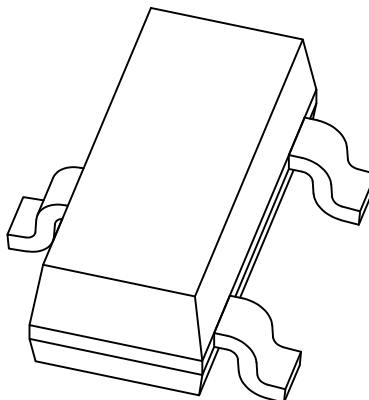


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### 3-Lead Small Outline Transistor (C6X) - [SOT-23] Supertex Legacy Package (K1/T)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



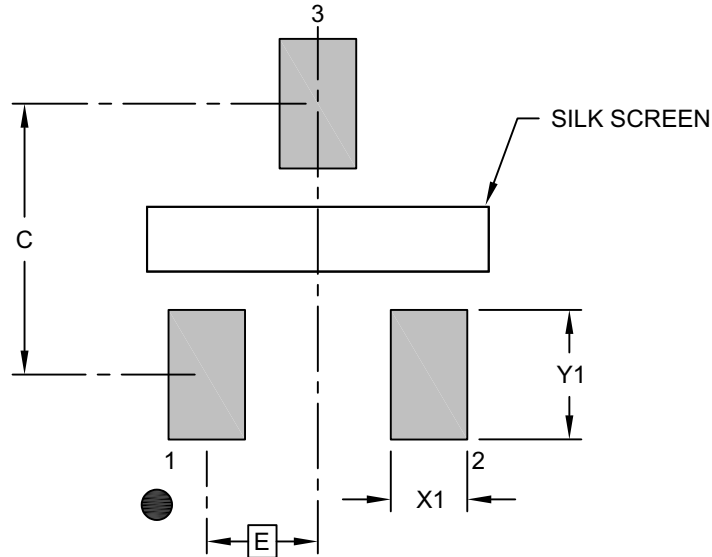
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	3		
Pitch	e	0.95 BSC		
Overall Pitch	e1	1.90 BSC		
Overall Height	A	0.89	–	1.12
Standoff	A1	0.01	–	0.10
Molded Package Thickness	A2	0.88	0.95	1.02
Overall Length	D	2.80	2.90	3.04
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.20	1.30	1.40
Terminal Width	b	0.30	–	0.50
Terminal Thickness	c	0.08	–	0.20
Terminal Length	L	0.20	0.50	0.60
Footprint	L1	0.54 REF		
Foot Angle	θ	0°	–	8°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

## 3-Lead Small Outline Transistor (C6X) - [SOT-23] Supertex Legacy Package (K1/T)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.30	
Contact Pad Width (X3)	X1			0.65
Contact Pad Length (X3)	Y1			1.10

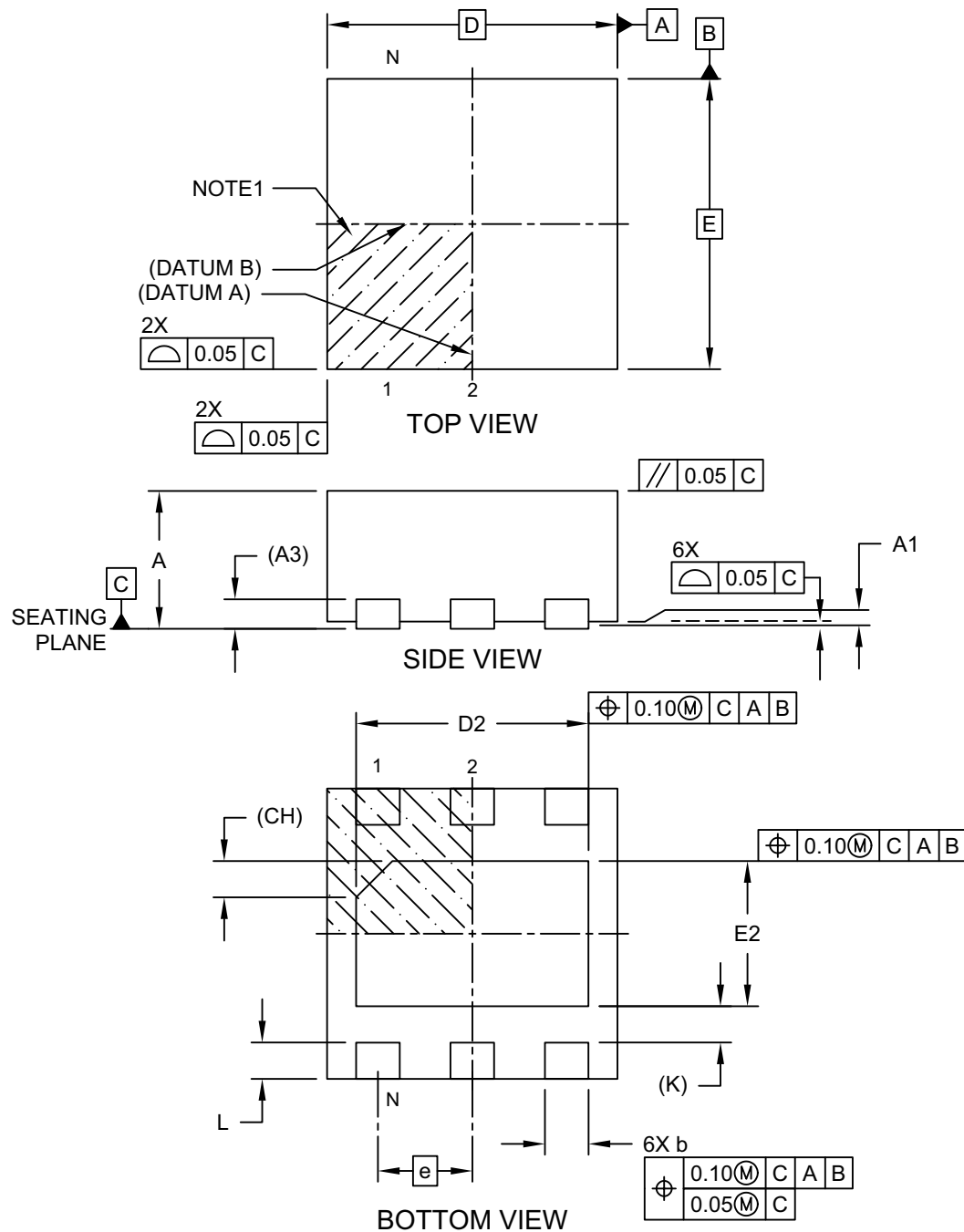
#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-19458 Rev A

## 6-Lead Plastic Dual Flat, No Lead Package (7AX) - 2x2x0.9 mm Body [DFN]

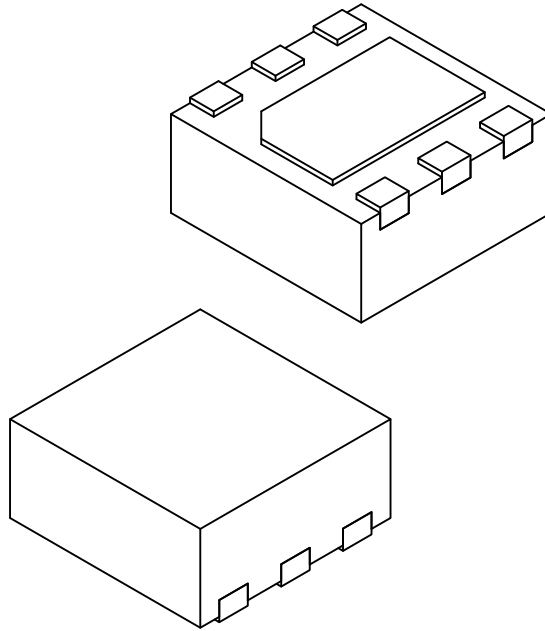
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-120-7AX Rev D Sheet 1 of 2

## 6-Lead Plastic Dual Flat, No Lead Package (7AX) - 2x2x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.87	0.95
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	2.00 BSC		
Exposed Pad Length	D2	1.50	1.60	1.70
Overall Width	E	2.00 BSC		
Exposed Pad Width	E2	0.90	1.00	1.10
Chamfer	CH	0.25 REF		
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.20	0.25	0.30
Terminal-to-Exposed-Pad	K	0.25 REF		

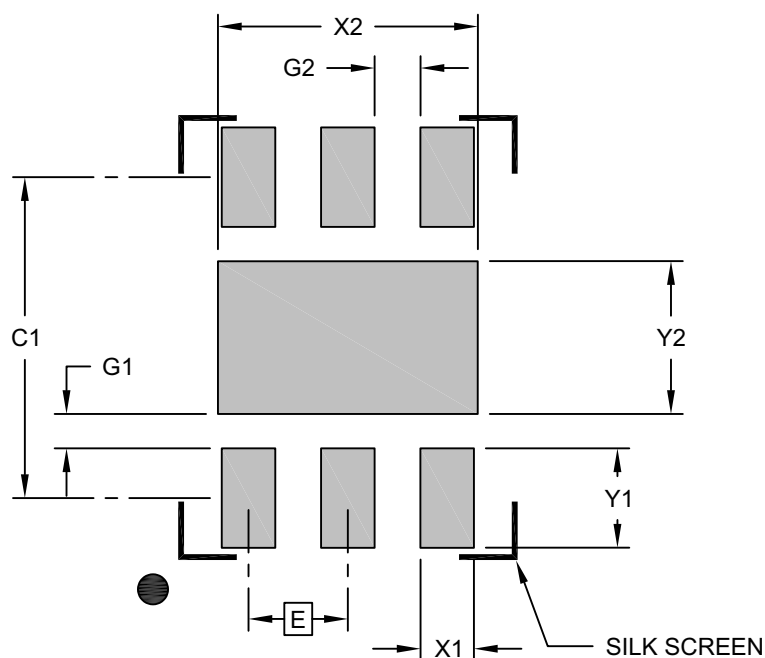
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120-7AX Rev D Sheet 2 of 2

## 6-Lead Plastic Dual Flat, No Lead Package (7AX) - 2x2x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		0.65 BSC		
Center Pad Width	X2				1.70
Center Pad Length	Y2				1.00
Contact Pad Spacing	C1			1.70	
Contact Pad Width (X6)	X1				0.35
Contact Pad Length (X6)	Y1				0.65
Contact Pad to Center Pad (X6)	G1		0.20		
Contact Pad to Contact Pad (X4)	G2		0.25		

#### Notes:

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2120-7AX Rev D

NOTES:

## APPENDIX A: REVISION HISTORY

### Revision E (April 2023)

- Added package 6-lead DFN and related information throughout the document.
- Made minor text changes throughout the document.

### Revision D (March 2022)

- Updated tables [DC Electrical Characteristics – Automotive](#) and [AC Electrical Characteristics – Automotive](#).
- Updated [Section 4.1 "Package Marking Information"](#).
- Updated [Product Identification System](#) format.
- Updated legal and contact information.

### Revision C (June 2020)

- Added automotive specifications to the Electrical Characteristics section.
- Added automotive specifications to the Product Identification System section.
- Made minor text changes throughout the document.

### Revision B (February 2020)

- Revised the order of pins in the Pin Function Table.
- Revised the Electrical Specifications and included notes in the DC Electrical Characteristics and AC Electrical Characteristics tables.
- Made minor text changes throughout the document.

### Revision A (December 2018)

- Converted Supertex Doc# DSFP-TP5335 to Microchip DS20005704A.
- Made minor text changes throughout the document.

NOTES:



## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	<u>-X</u>	<u>-XXX</u>
Device	Package	Environmental	Qualification
<div> <div> <b>Device:</b> TP5335: P-Channel Enhancement-Mode Vertical DMOS FET </div> <div> <b>Package:</b> K1 = 3-lead SOT-23 MF = 6-lead DFN </div> <div> <b>Environmental:</b> G = Lead (Pb)-free/RoHS-compliant Package </div> <div> <b>Media Type:</b> (Blank) = 3000/Reel for a K1 Package = 3000/Reel for a MF Package </div> <div> <b>Qualification:</b> (Blank) = Standard Part VAO = Automotive AEC-Q100 Qualified </div> </div>			
<b>Examples:</b> <div> a) TP5335K1-G: P-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-23, 3000/Reel </div> <div> b) TP5335K1-G-VAO: P-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-23, 3000/Reel, Automotive Qualified </div> <div> c) TP5335MF-G-VAO: P-Channel Enhancement-Mode Vertical DMOS FET, 6-lead DFN, 3000/Reel, Automotive Qualified </div>			

NOTES:

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**Note the following details of the code protection feature on Microchip products:**

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
  - Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
  - Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
  - Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.
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