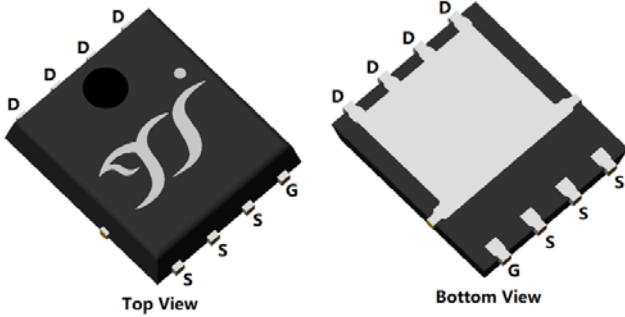
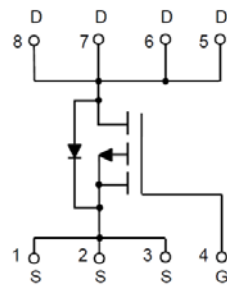


P-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L



Product Summary

- V_{DS} -30V
- I_D -70A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <5.5mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <9.5mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery management
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 25	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	-70	A
	$T_C=100^\circ\text{C}$		-44	
Pulsed Drain Current ^A		I_{DM}	-280	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	89	W
	$T_C=100^\circ\text{C}$		36	
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	7.4	W
Single Pulse Avalanche Energy ^B		E_{AS}	360	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	1.4	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient ^C		$R_{\theta JA}$	17	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG70P03A	F1	YJG70P03A	5000	10000	100000	13" reel



YJG70P03A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V	T _J =25°C		-1	μA
			T _J =55°C		-5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±25V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D =-20A		4.0	5.5	mΩ
		V _{GS} = -4.5V, I _D =-20A		6.0	9.5	
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V			-1.2	V
Maximum Body-Diode Continuous Current	I _S				-70	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHZ		6464		pF
Output Capacitance	C _{oss}			779		
Reverse Transfer Capacitance	C _{rss}			477		
Gate Resistance	R _g	Drain open, f=1Mhz		6.5		Ω
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-20A		111.7		nC
Gate-Source Charge	Q _{gs}			21.1		
Gate-Drain Charge	Q _{gd}			22.9		
Reverse Recovery Charge	Q _{rr}	I _F =-15A, di/dt=-100A/us		8.5		
Reverse Recovery Time	t _{rr}			24		
Turn-on Delay Time	t _{D(on)}	V _{GS} = -10V, V _{DD} = -15V, R _G =3Ω, R _L = 0.75Ω		15		ns
Turn-on Rise Time	t _r			75		
Turn-off Delay Time	t _{D(off)}			130		
Turn-off fall Time	t _f			80		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. T_J=25°C, V_{DD}=-25V, V_G=-10V, L=2mH, I_{AS}=-19A.

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the soldermounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

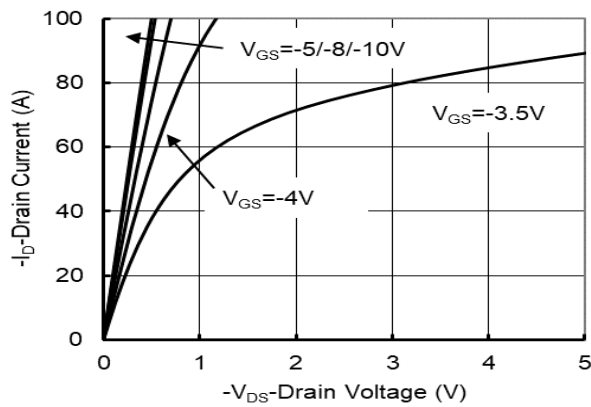


Figure1. Output Characteristics

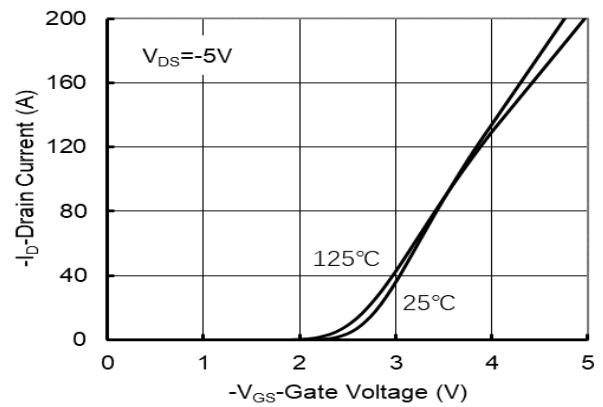


Figure2. Transfer Characteristics

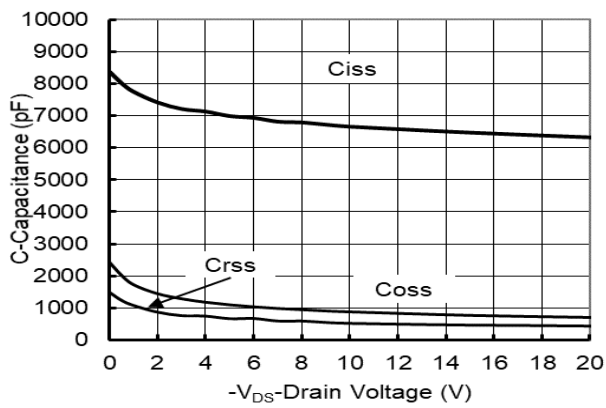


Figure3. Capacitance Characteristics

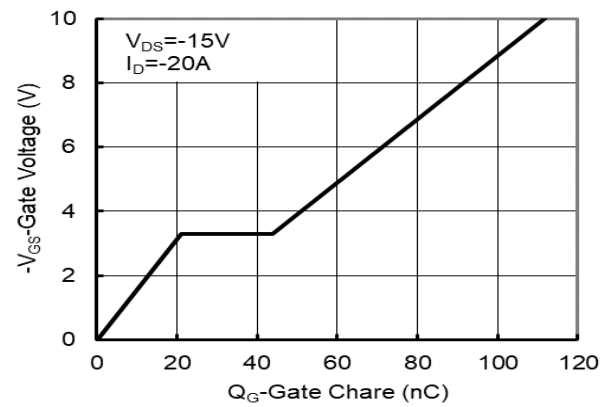


Figure4. Gate Charge

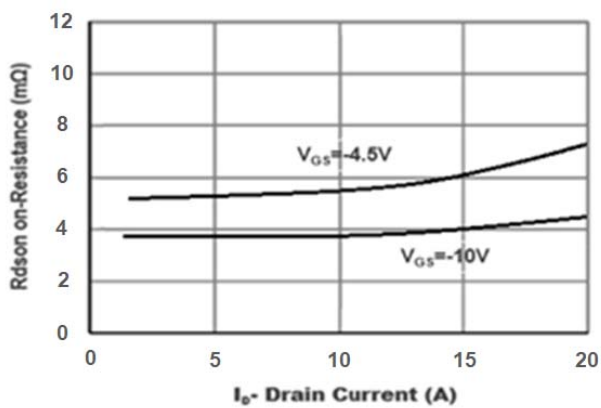


Figure5. Drain-Source on Resistance

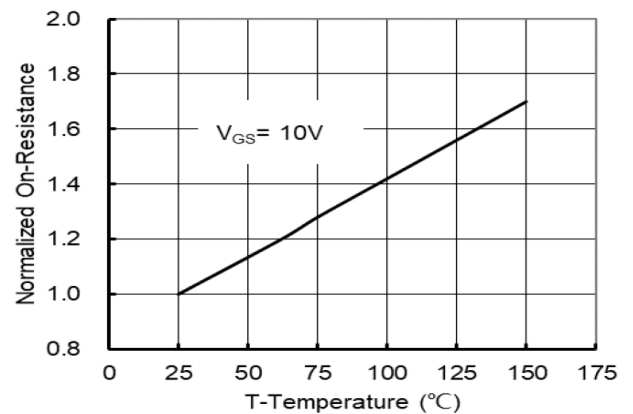


Figure6. Drain-Source on Resistance



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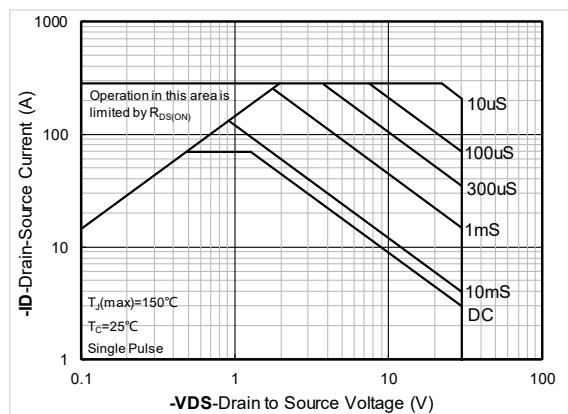


Figure7. Safe Operation Area

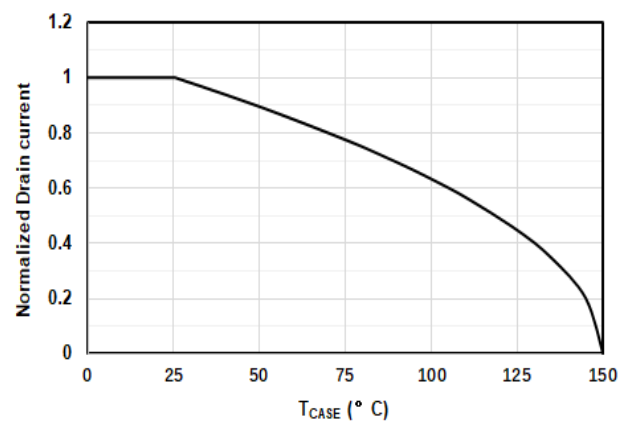


Figure8. Drain current vs. Case Temperature

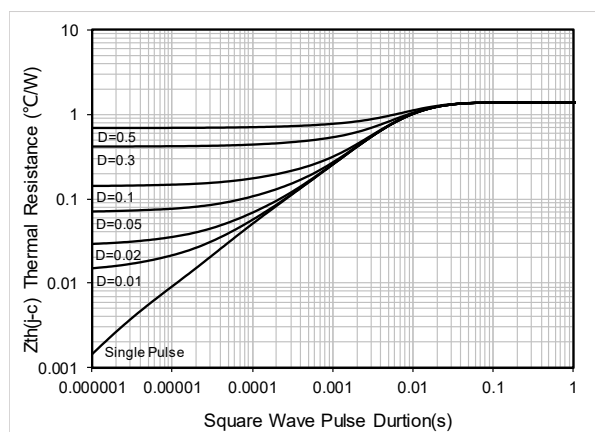
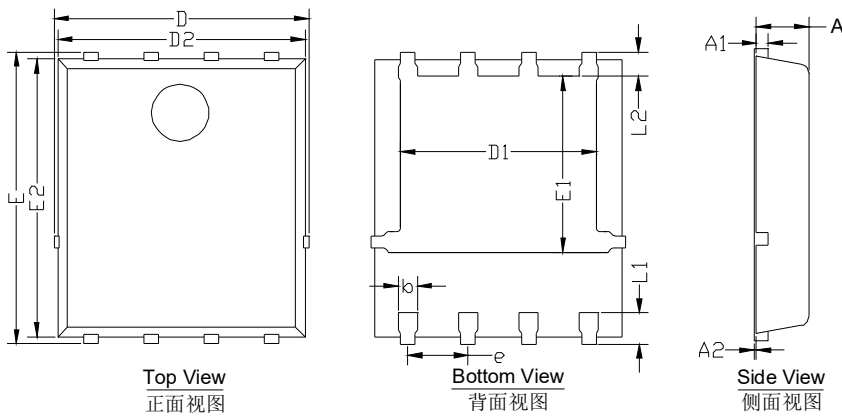


Figure9. Normalized Maximum Transient Thermal Impedance



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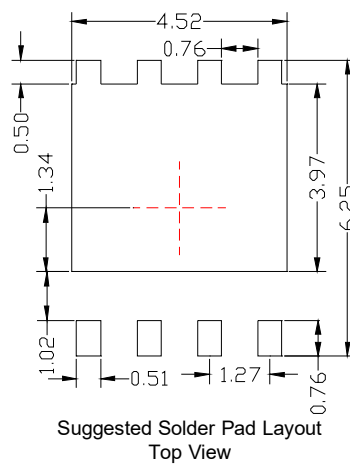
■ PDFN5060-8L Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.





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