

# VC9321A

P-Channel Enhancement Mode MOSFET

- Features

VDS	VGS	RDSon TYP	ID
-20V	$\pm 8V$	420mR@-4V5	
		600mR@-2V5	-0.67A
		900mR@-1V8	

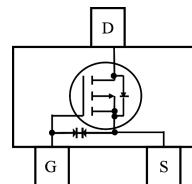
- General Description

This device is a P-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

- Applications

- Load switch;
- Level shift;
- Cell Phone

- Pin Configuration(SOT723 Top View)



- Absolute Maximum Ratings @ TA = 25°C unless otherwise specified

Parameter	Symbol	Ratings		Unit
Drain-Source Voltage	V <sub>DS</sub>	-20		V
Gate-Source Voltage	V <sub>GS</sub>			
Drain Current (Note 1)	I <sub>D</sub>	-0.67	-1.35	A
Pulsed				
Power Dissipation Derating above T <sub>A</sub> = 25°C (Note 1)	P <sub>d</sub>	175		mW
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150		°C

Note1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inches. The rating is for each chip in the package.

- Electrical Characteristics @ TA = 25°C unless otherwise specified

Parameter (Note 2)	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250uA	-20	--	--	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V	--	--	1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = $\pm 8V$ , V <sub>DS</sub> = 0V	--	--	$\pm 10$	uA
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250uA	-0.35	-0.60	-1	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	I <sub>D</sub> = -0.55A, V <sub>GS</sub> = -4.5V	--	420	750	mR
		I <sub>D</sub> = -0.35A, V <sub>GS</sub> = -2.5V	--	600	1000	
		I <sub>D</sub> = -0.25A, V <sub>GS</sub> = -1.8V	--	900	2000	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -6V, R <sub>L</sub> = 6R, I <sub>D</sub> = -1A, V <sub>GEN</sub> = -4.5V, R <sub>G</sub> = 6R	--	10	--	ns
Turn-On Rise Time	t <sub>r</sub>		--	62	--	
Turn-Off Delay Time	t <sub>d(off)</sub>		--	19	--	
Turn-Off Fall Time	t <sub>f</sub>		--	18	--	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -6V, V <sub>GS</sub> = 0V, f = 200KHz	--	50	--	pF
Output Capacitance	C <sub>oss</sub>		--	15	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	15	--	
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -0.1A	--	-0.8	-1.2	V

Note2. Short duration test pulse used to minimize self-heating effect.

- Typical Performance Characteristics

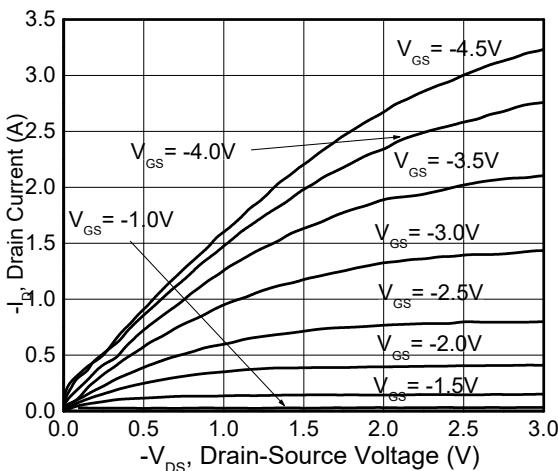


Fig1. Output Characteristics

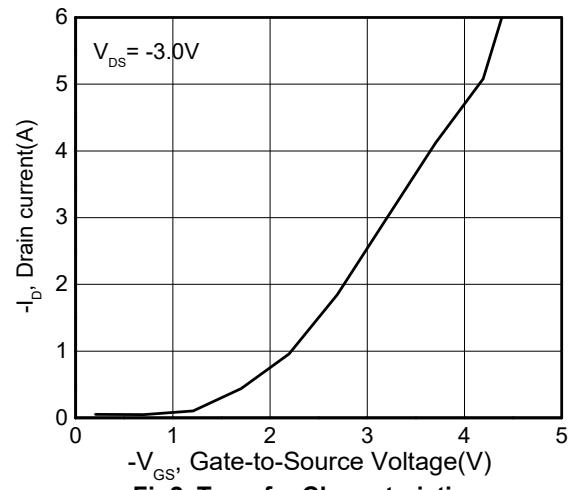


Fig2. Transfer Characteristics

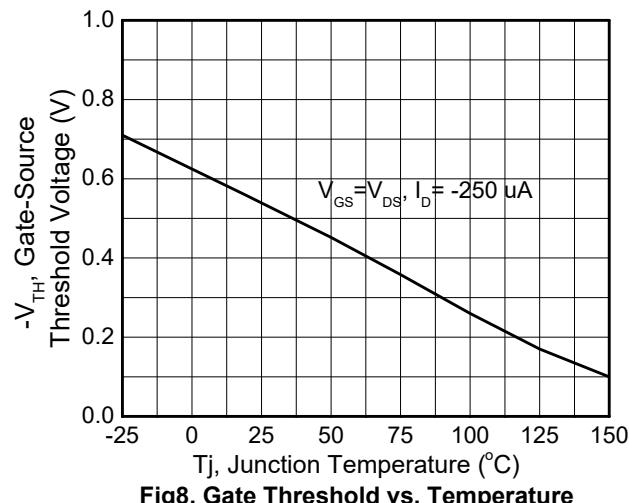


Fig3. Gate Threshold vs. Temperature

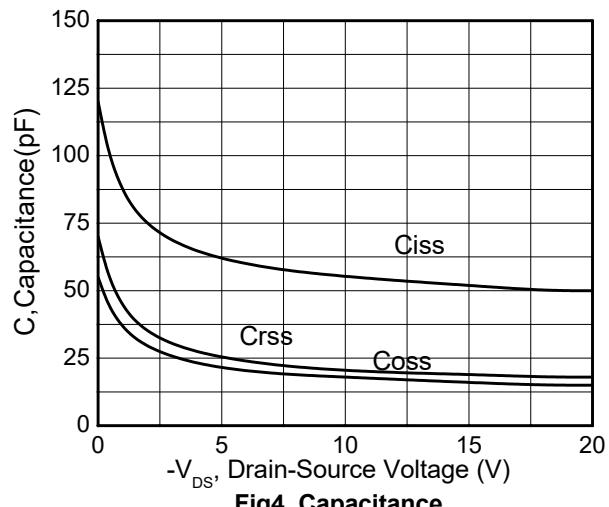


Fig4. Capacitance

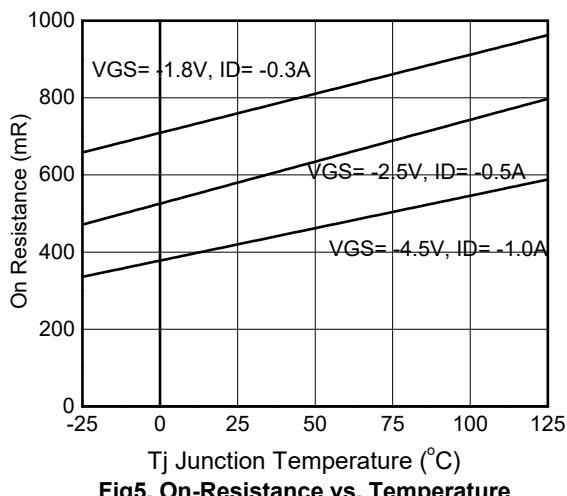


Fig5. On-Resistance vs. Temperature

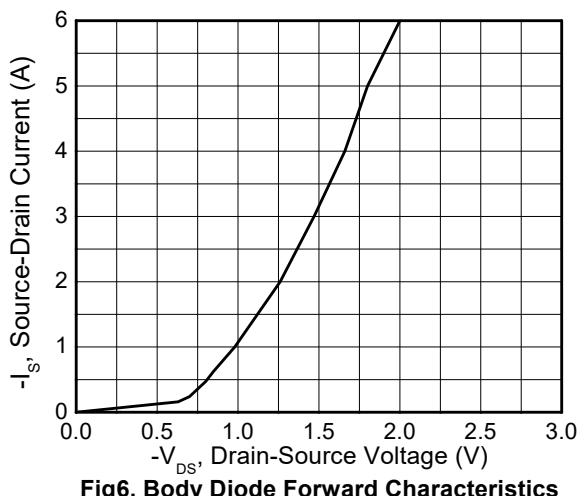
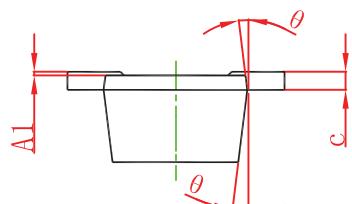
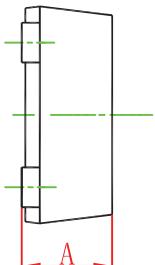
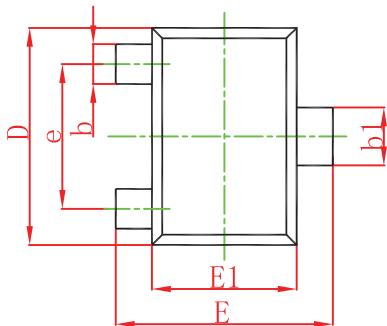


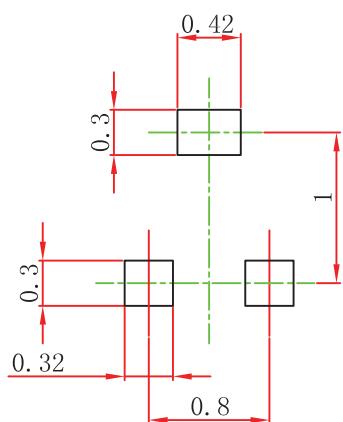
Fig6. Body Diode Forward Characteristics

### SOT-723 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.430	0.500	0.017	0.020
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
b1	0.270	0.370	0.011	0.015
c	0.080	0.150	0.003	0.006
D	1.150	1.250	0.045	0.049
E	1.150	1.250	0.045	0.049
E1	0.750	0.850	0.030	0.033
e	0.800TYP.		0.031TYP.	
θ	7° REF.		7° REF.	

### SOT-723 Suggested Pad Layout



Note:  
 1. Controlling dimension:in millimeters.  
 2. General tolerance: $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.



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