12-Bit, 10.25 GSPS, JESD204B, RF Analog-to-Digital Converter

Preliminary Technical Data

AD9213

FEATURES

High instantaneous dynamic range
- **Noise spectral density 154 dBFS/Hz**
- **SFDR 68 dBc (1 GHz, −1 dBFS)**

Low power consumption: 5.1 W at 10 GSPS
Integrated input buffer (6.5 GHz input bandwidth)
- **1.4 V p-p full-scale input with RIN = 50 Ω**
- **Overvoltage protection**

16-lane JESD204B output (up to 16 Gbps line rate)
Multichip sync capable with 1 sample accuracy
- **DDC NCO synchronization included**

Fast overrange detection for efficient AGC
Integrated DDC
- **Selectable decimation factors**
- **16-profile settings for fast frequency hopping**

Optional on-chip PLL clock multiplier
On-chip temperature sensor
On-chip negative voltage generators
Low CER <1e−16
12 mm × 12 mm BGA

GENERAL DESCRIPTION

The AD9213 is a single 12-bit, 10.25 GSPS, RF analog-to-digital converter (ADC) with a 6.5 GHz input bandwidth. The AD9213 has been optimized to support high dynamic range frequency and time domain applications requiring wide instantaneous bandwidth and low code error rates (CER). The AD9213 features a 16-lane JESD204B interface to support its maximum bandwidth capability.

The AD9213 achieves industry leading dynamic range and linearity performance while consuming only 5 W. Based on an interleaved pipeline architecture, the AD9213 features a proprietary calibration and randomization technique that suppresses interleaving spurious artifacts into its noise floor. The excellent linearity performance of the AD9213 under low level signal conditions is preserved by a combination of on-chip dithering and calibration resulting in excellent windowed spurious free performance (<−95 dBFS) over a wide range of input signal conditions.

Applications requiring less instantaneous bandwidth can benefit from the on-chip digital signal processing (DSP) capability of the AD9213 that reduces the output data rate along with the number of JESD204b lanes required to support it. The DSP path includes a digital downconverter (DDC) with a 48-bit, numerically controlled oscillator (NCO) followed by an I and Q digital decimator stage allowing for selectable decimation rates that are factors of two or three. For fast frequency hopping applications, the AD9213 NCO supports up to 16-profile settings with separate trigger input allowing for wide surveillance frequency coverage but at a reduced JESD204B lane count.

The AD9213 also supports sample accurate multichip synchronization that also includes synchronization of the NCOs. The AD9213 will be offered in a 192 flip-chip ball grid array (FcBGA) package. The AD9213 is specified over a junction temperature range of −10°C to +115°C.

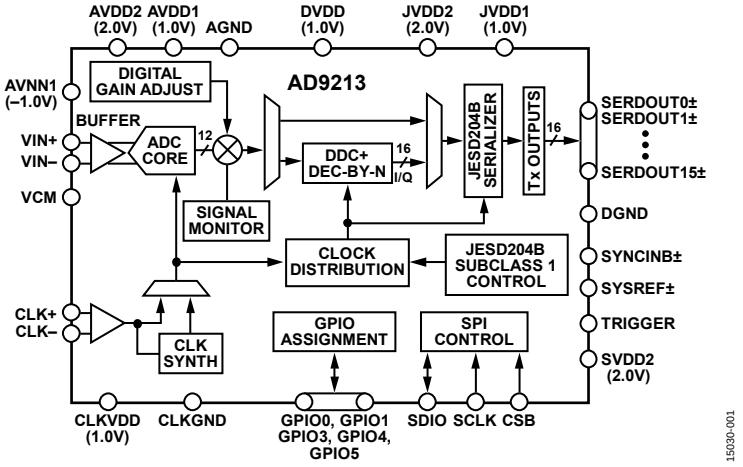

Figure 1.

Rev. PrF **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

SPECIFICATIONS

DC SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, AIN = −1.0 dBFS.

Table 1.

Parameter	Test Conditions/ Comments	Temperature[1]	AD9213-6G Min	AD9213-6G Typ	AD9213-6G Max	AD9213-10G Min	AD9213-10G Typ	AD9213-10G Max	Unit
RESOLUTION			12			12			Bits
ACCURACY									
No Missing Codes		Full	Guaranteed			Guaranteed			
Offset Error		Full							LSB
Gain Error		Full							%FSR
Differential Nonlinearity (DNL)		Full							LSB
Integral Nonlinearity (INL)		Full							LSB
ANALOG INPUTS									
Differential Input									
Voltage Range	Internal V_{REF} =	Full		1.4			1.4		V p-p
Resistance		70°C		50			50		Ω
Capacitance		70°C		1			1		pF
Internal Common-Mode Voltage (V_{CM})		Full		0.5			0.5		V
Analog Full-Power									
Bandwidth	Internal termination	70°C		6.5			6.5		GHz
Input Referred Noise		70°C							LSB_{RMS}
POWER SUPPLIES									
BVDD2		70°C		2.0			2.0		V
BVNN1		70°C		−1.0			−1.0		V
AVNN1		70°C		−1.0			−1.0		V
BVNN2	Internally generated	70°C		−2.0			−2.0		V
BVDD3	Internally generated	70°C		3.0			3.0		V
AVDD		70°C		1.0			1.0		V
CLKVDD_LF		70°C		1.0			1.0		V
CLKVDD_HF		70°C		1.0			1.0		V
PLLVDD2		70°C		2.0			2.0		V
AVDDFS8		70°C		1.0			1.0		V
FVDD		70°C		1.0			1.0		V
VDD_NVG		70°C		1.0			1.0		V
RVDD2		70°C		2.0			2.0		V
SVDD2		70°C		2.0			2.0		V
JVDD2		70°C		2.0			2.0		V
DVDD		70°C		1.0			1.0		V
JVTT		70°C		1.0			1.0		V
JVDD		70°C		1.0			1.0		V
TMU_AVDD2		70°C		2.0			2.0		V
TMU_DVDD1		70°C		1.0			1.0		V
I_{BVDD2}		70°C		111			136		mA
$I_{BVNN1} + I_{AVNN1}$[2]		70°C		122			122		mA
I_{BVNN2}[3]		70°C							mA
I_{BVDD3}[3]		70°C							mA
I_{AVDD}		70°C		1750			2250		mA
I_{CLKVDD_LF}		70°C		30			33		mA
I_{CLKVDD_HF}		70°C		40			66		mA
$I_{PLLVDD2}$		70°C		71			71		mA
I_{FVDD}		70°C		25			30		mA

Parameter	Test Conditions/ Comments	Temperature[1]	AD9213-6G Min	AD9213-6G Typ	AD9213-6G Max	AD9213-10G Min	AD9213-10G Typ	AD9213-10G Max	Unit
I_{VDD_NVG}		70°C		363			420		mA
I_{RVDD2}		70°C		35			37		mA
$I_{SVDD2} + I_{JVDD2}$		70°C		29			29		mA
I_{DVDD}[4]+$I_{AVDDFS8}$		70°C		676			1170		mA
$I_{JVDD} + I_{JVTT}$		70°C		490			800		mA
I_{TMU_AVDD2}		70°C		2			2		mA
I_{TMU_DVDD1}		70°C		3			3		mA
Power Dissipation[5]		70°C		3.7			5.1		W
Power-Down Dissipation									mW

[1] Full temperature range is −10°C to +115°C junction temperature (T_j). All temperatures are junction temperature.
[2] Sink current if supplied by an external source. This current is normally provided by VNEG_OUT when VNEG_OUT is connected to BVNN1 and AVNN1 on the board.
[3] Internally supplied.
[4] Digital downconverter (DDC) off.
[5] Power with optional PLL off, DDC off. Power and supply currents are estimates.

AC SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, AIN = −1.0 dBFS.

Table 2.

Parameter	Test Conditions/ Comments	Temperature[1]	AD9213-6G Min	AD9213-6G Typ	AD9213-6G Max	AD9213-10G Min	AD9213-10G Typ	AD9213-10G Max	Unit
ANALOG INPUT	Full scale	Full		1.4			1.4		V p-p
NOISE DENSITY		70°C							dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)									
f_{IN} = 150 MHz		70°C		57.5			57.2		dBFS
f_{IN} = 1000 MHz		70°C		56.8			56.2		dBFS
f_{IN} = 2600 MHz		70°C		54.9			52		dBFS
f_{IN} = 4000 MHz		70°C		53.0			49.5		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)									
f_{IN} = 150 MHz		70°C		56.5			55		dBc
f_{IN} = 1000 MHz		70°C		55.8			54.0		dBc
f_{IN} = 2600 MHz		70°C		53.9			49.8		dBc
f_{IN} = 4000 MHz		70°C		52.0			47.3		dBc
EFFECTIVE NUMBER OF BITS (ENOB)									
f_{IN} = 150 MHz		70°C		9.1			8.8		Bits
f_{IN} = 1000 MHz		70°C		9.0			8.7		Bits
f_{IN} = 2600 MHz		70°C		8.7			8.0		Bits
f_{IN} = 4000 MHz		70°C		8.3			7.6		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR)	Including second or third harmonic								
f_{IN} = 150 MHz		70°C		78			61		dBc
f_{IN} = 1000 MHz		70°C		67			68		dBc
f_{IN} = 2600 MHz		70°C		66			63		dBc
f_{IN} = 4000 MHz		70°C		53			56		dBc
SECOND HARMONIC (H2)									
f_{IN} = 150 MHz		70°C		−78			−61		dBc
f_{IN} = 1000 MHz		70°C		−67			−68		dBc
f_{IN} = 2600 MHz		70°C		−67			−63		dBc
f_{IN} = 4000 MHz		70°C		−53			−56		dBc

Parameter	Test Conditions/ Comments	Temperature[1]	AD9213-6G Min	AD9213-6G Typ	AD9213-6G Max	AD9213-10G Min	AD9213-10G Typ	AD9213-10G Max	Unit
THIRD HARMONIC (H3)									
f_{IN} = 150 MHz		70°C		−78			−73		dBc
f_{IN} = 1000 MHz		70°C		−70			−70		dBc
f_{IN} = 2600 MHz		70°C		−66			−66		dBc
f_{IN} = 4000 MHz		70°C		−68			−72		dBc
WORST OTHER SPUR	Excluding second or third harmonic								
f_{IN} = 150 MHz		70°C		−90			−90		dBc
f_{IN} = 1000 MHz		70°C		−90			−90		dBc
f_{IN} = 2600 MHz		70°C		−85			−85		dBc
f_{IN} = 4000 MHz		70°C		−85			−85		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD3, $2f_{IN1}$-f_{IN2})	At −8 dBFS per tone								
f_{IN1} = 750 MHz, f_{IN2} = 760 MHz		70°C		−88					dBc
f_{IN1} = 1800 MHz, f_{IN2} = 1810 MHz		70°C		−83					dBc

[1] Full temperature range is −10°C to +115°C junction temperature (T_j). All temperatures are junction temperature.

DIGITAL SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, AIN = −1.0 dBFS.

Table 3.

Parameter	Temperature[1]	Min	Typ	Max	Unit
CLOCK INPUTS (CLK_P, CLK_N)					
Differential Input Voltage	Full		800		mV p-p
Common-Mode Input Voltage	Full				V
Input Resistance (Differential)	Full				kΩ
Input Capacitance	Full				pF
SYSREF INPUTS (SYSREF_P, SYSREF_N)					
Logic Compliance			LVDS		
Differential Input Voltage	Full		700		mV p-p
Common-Mode Input Voltage	Full		1.2		V
Input Resistance (Differential)	Full				kΩ
Input Capacitance	Full				pF
LOGIC INPUTS (SDIO, SCLK, CSB)					
Logic Compliance			CMOS		
Voltage					
Logic 1	Full				V
Logic 0	Full				V
Input Resistance (differential)	Full		100		Ω
Input Capacitance	Full				pF
SYNCINB_P/SYNCINB_N INPUT					
Logic Compliance	Full		LVDS		
Input Voltage					
Differential	Full				mV p-p
Common Mode	Full				V
Input Resistance (Differential)	Full				Ω
Input Capacitance	Full				pF
LOGIC OUTPUT (SDIO)					
Logic Compliance			CMOS		
Voltage					
Logic 1 (I_{OH} = 800 µA)	Full				V
Logic 0 (I_{OL} = 50 µA)	Full				V

Parameter	Temperature[1]	Min	Typ	Max	Unit
DIGITAL OUTPUTS (SERDOUT_P[x], SERDOUT_N[x])					
Compliance	Full		CML		
Output Voltage					
Differential	Full				mV p-p
Offset	Full				mV p-p
Differential Return Loss (RL_{DIFF})[2]	70°C				dB
Common-Mode Return Loss (RL_{CM})	70°C				dB
Differential Termination Impedance	70°C			100	Ω
RESET (RSTB)					
Voltage					
Logic 1	Full				V
Logic 0	Full				V
Input Resistance (Differential)	Full				kΩ
Input Capacitance	Full				pF
PWDN					
Logic Compliance			CMOS		
Voltage					
Logic 1	Full				V
Logic 0	Full				V
Input Resistance (Differential)	Full				kΩ
Input Capacitance	Full				pF

[1] Full temperature range is −10°C to +115°C junction temperature (T_J). All temperatures are junction temperature.
[2] Differential and common-mode return loss measured from 100 MHz to 0.75 × baud rate.

SWITCHING SPECIFICATIONS

Nominal supply voltages, specified maximum sampling rate, internal reference, AIN = −1.0 dBFS.

Table 4.

Parameter	Test Conditions/Comments	Temperature[1]	Min	Typ	Max	Unit
CLOCK (CLK)						
Maximum Clock Rate		Full			10.25	GSPS
Minimum Clock Rate		Full				MSPS
Clock Pulse Width High		Full				% duty cycle
Clock Pulse Width Low		Full				% duty cycle
SYSREF (SYSREF±)[2]						
Setup Time (t_{SU_SR})		70°C				ps
Hold Time (t_{H_SR})		70°C				ps
FAST DETECT OUTPUT (FD)						
Latency		Full				Clock cycles
OUTPUT PARAMETERS (SERDOUT[x]±)						
Rise Time		70°C				ps
Fall Time		70°C				ps
Pipeline Latency		70°C				Clock cycles
SYNCB± Falling Edge to First K.28 Characters		70°C				Multiframes
CGS Phase K.28 Characters Duration		70°C				Multiframes
Differential Termination Resistance		70°C				Ω
APERTURE						
Delay		Full				ps
Uncertainty (Jitter)		Full		50		f_S rms
Out-of-Range Recovery Time		Full				Clock cycles

[1] Full temperature range is −10°C to +115°C junction temperature (T_J). All temperatures are junction temperature.
[2] SYSREF± setup and hold times are defined with respect to the rising SYSREF± edge and rising clock edge. Positive setup time leads the clock edge. Negative hold time also leads the clock edge.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK				ns
t_{DH}	Hold time between the data and the rising edge of SCLK				ns
t_{CLK}	Period of the SCLK				ns
t_S	Setup time between CSB and SCLK				ns
t_H	Hold time between CSB and SCLK				ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state				ns
t_{LOW}	Minimum period that SCLK should be in a logic low state				ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge				ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge				ns

Timing Diagrams

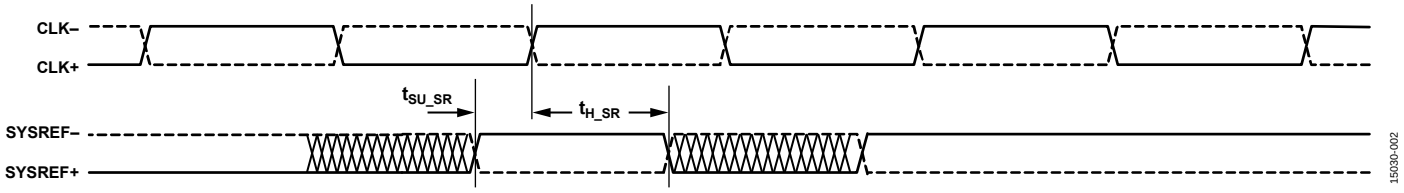

Figure 2. SYSREF± Setup and Hold Timing

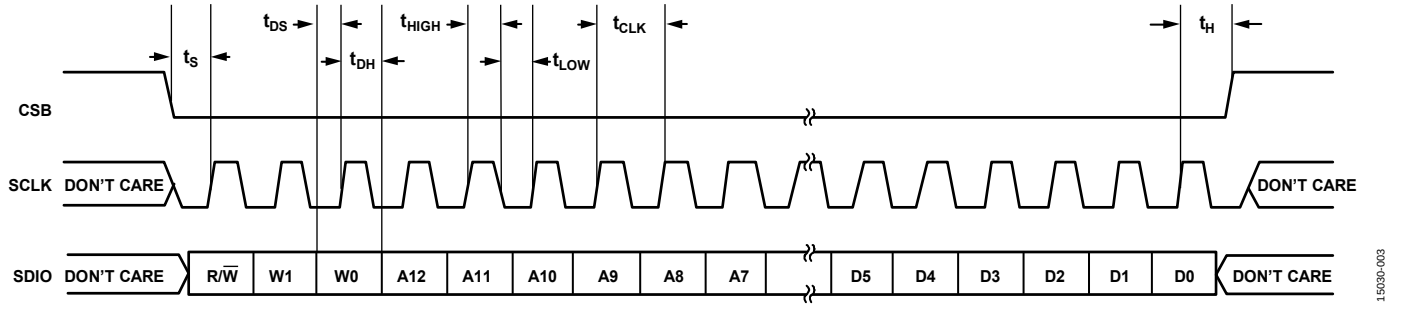

Figure 3. Serial Port Interface Timing Diagram (MSB First)

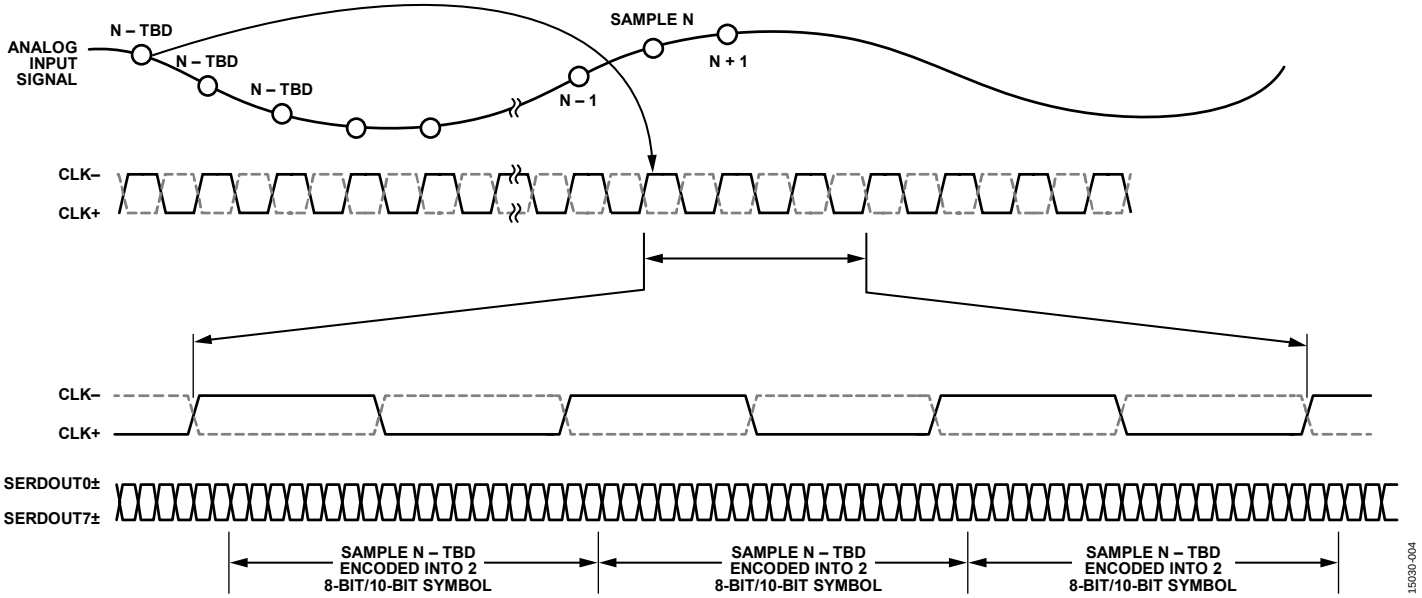

Figure 4. Data Output Timing for Eight Lane Mode

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	TBD
Environmental	
Storage Temperature Range	TBD
Operating Junction Temperature Range	−10°C to +115°C
Maximum Junction Temperature	TBD

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
BP-192-1			
4-Layer	TBD	TBD	°C/W
10-Layer	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

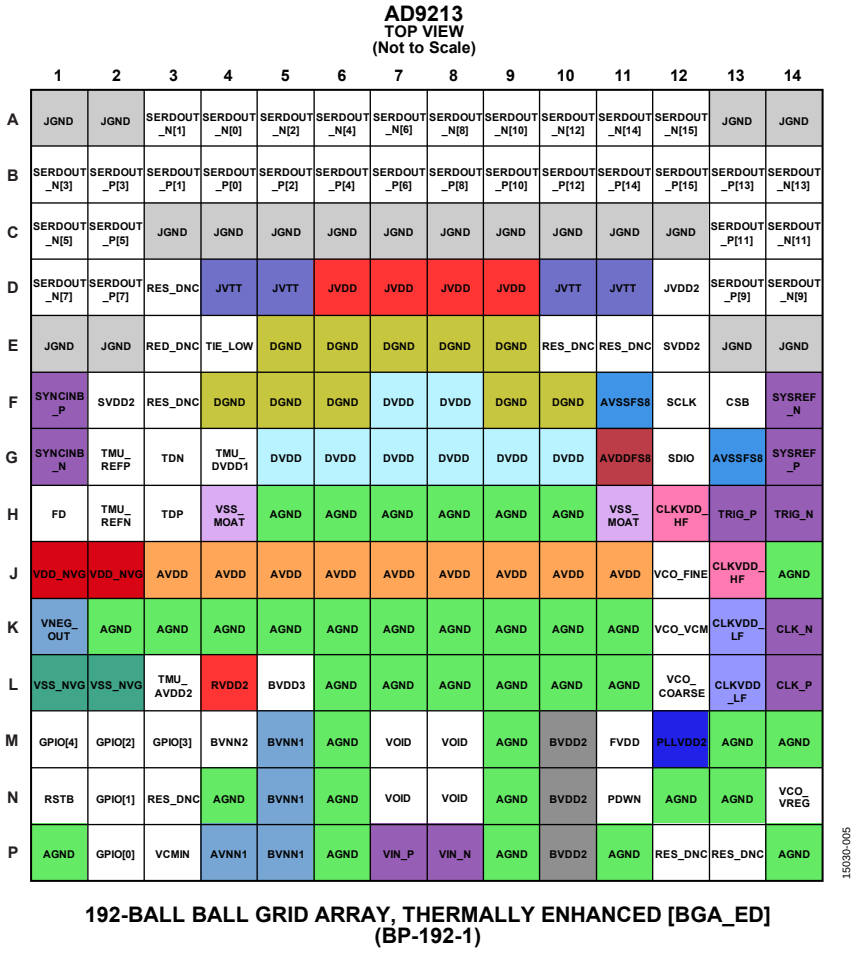

Figure 5. Pin Configuration, Top View, Not To Scale

Table 8. Pin Function Descriptions

Pin No.	Ball Name	Input/Output	Signal Type	Description
P3	VCMIN	Output	Static	Export VCM
P7, P8	VIN_P, VIN_N	Input	RF	ADC inputs, high frequency
N3	RES_DNC			Reserved, Do Not Connect
H3, G3	TDP, TDN		Static	Temperature Diode anode/cathode (can float if unused)
L14, K14	CLK_P, CLK_N	Input	RF	Clock inputs, high frequency
G14, F14	SYSREF_P, SYSREF_N	Input/Output	LVDS/CML	Differential Synchronization Signal. Critical timing relative to CLK. Placed near CLK inputs. Used to establish deterministic latency. (Internally tied to ground through 50 Ω in default configuration. Can leave floating if set to Subclass0 mode by Register 0x525)
H13, H14	TRIG_P, TRIG_N	Input	LVDS	Trigger input for freq. hopping. Similar to SYSREF inputs. (Internally tied to ground through 50 Ω in default configuration. Can leave floating if left disabled by default with Register 0x602)

Pin No.	Ball Name	Input/Output	Signal Type	Description
K12	VCO_VCM	Input/Output	Static	PLL: Common-mode pin tapping from center of VCO, used in filter
J12	VCO_FINE	Input/Output	Static	PLL loop filter fine connection
L12	VCO_COARSE	Input/Output	Static	PLL loop filter coarse connection
N14	VCO_VREG	Input/Output	Static	PLL LDO Regulator output; can be overdriven
P12, P13	RES_DNC			Reserved, Do Not Connect
H2	TMU_REFN	Input	Static	Connect to clean ground on board.
G2	TMU_REFP	Input	Static	Connect to clean 1.8 V reference supply on the board. Should be less or equal to TMU_AVDD2.
G12	SDIO	Input/Output		Main SPI input/output
F12	SCLK	Input		Main SPI clock
F13	CSB	Input		Chip Select for SPI
F1, G1	SYNCINB_P/SYNCINB_N	Input		When low, JESD handshakes with rcvr; goes high when handshake is complete
B4, A4	SERDOUT_P[0]/SERDOUT_N[0]	Output	JESD204B	Lane0 differential pair
B3, A3	SERDOUT_P[1]/SERDOUT_N[1]	Output	JESD204B	Lane1 differential pair
B5, A5	SERDOUT_P[2]/SERDOUT_N[2]	Output	JESD204B	Lane2 differential pair
B2, B1	SERDOUT_P[3]/SERDOUT_N[3]	Output	JESD204B	Lane3 differential pair
B6, A6	SERDOUT_P[4]/SERDOUT_N[4]	Output	JESD204B	Lane4 differential pair
C2, C1	SERDOUT_P[5]/SERDOUT_N[5]	Output	JESD204B	Lane5 differential pair
B7, A7	SERDOUT_P[6]/SERDOUT_N[6]	Output	JESD204B	Lane6 differential pair
D2, D1	SERDOUT_P[7]/SERDOUT_N[7]	Output	JESD204B	Lane7 differential pair
B8, A8	SERDOUT_P[8]/SERDOUT_N[8]	Output	JESD204B	Lane8 differential pair
D13, D14	SERDOUT_P[9]/SERDOUT_N[9]	Output	JESD204B	Lane9 differential pair
B9, A9	SERDOUT_P[10]/SERDOUT_N[10]	Output	JESD204B	Lane10 differential pair
C13, C14	SERDOUT_P[11]/SERDOUT_N[11]	Output	JESD204B	Lane11 differential pair
B10, A10	SERDOUT_P[12]/SERDOUT_N[12]	Output	JESD204B	Lane12 differential pair
B13, B14	SERDOUT_P[13]/SERDOUT_N[13]	Output	JESD204B	Lane13 differential pair
B11, A11	SERDOUT_P[14]/SERDOUT_N[14]	Output	JESD204B	Lane14 differential pair
B12, A12	SERDOUT_P[15]/SERDOUT_N[15]	Output	JESD204B	Lane15 differential pair
M1, M3, M2, N2, P2	GPIO[4], GPIO[3], GPIO[2], GPIO[1], GPIO[0]	Input / Output		General Purpose I/O (Can be left floating in default configuration)
E4	TIE_LOW	Input	CMOS	Connect to ground
H1	FD	Output	CMOS	Fast Detect
E11, E10, D3, E3, F3	RES_DNC			Reserved – Do Not Connect
N11	PDWN	Input	CMOS	Powerdown/Standby Mode Control
N1	RSTB	Input		
M10, N10, P10	BVDD2	Supply		2V supply for input buffer
M5, N5, P5	BVNN1	Supply		–1V supply for input buffer
M4	BVNN2	Supply		Internally generated -2V supply for input buffer - used for decoupling cap
L5	BVDD3	Supply		Internally generated 3V supply for input buffer - used for decoupling cap
K13, L13	CLKVDD_LF	Supply		1V supply for clock
M12	PLLVDD2	Supply		2.0V LDO Supply
J13, H12	CLKVDD_HF	Supply		1V Supply
G11	AVDDFS8	Supply		1V supply for clocks w/ fs/8 energy
F11, G13	AVSSFS8	Ground		
M11	FVDD	Supply		1V supply for refADC

Pin No.	Ball Name	Input/Output	Signal Type	Description
J1, J2	VDD_NVG	Supply		1V Supply for NVG
L1, L2	VSS_NVG	Ground		VSS for NVG
K1	VNEG_OUT	Output		Internally generated −1V output
L4	RVDD2	Supply		2V supply for top_ref
P4	AVNN1	Supply		−1V supply for top_ref
J3, J4, J5, J6, J7, J8, J9, J10, J11	AVDD	Supply		1V supply for ADC
H5, H6, H7, H8, H9, H10, J14, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11, M6, M9, M13, M14, N4, N6, N9, N12, N13, P1, P6, P9, P11, P14	AGND	Ground		Ground for ADC
H4, H11	VSS_MOAT	Ground		
E12, F2	SVDD2	Supply		2V supply for digital I/O and SPI
F7, F8, G5, G6, G7, G8, G9, G10	DVDD	Supply		1V supply for digital
E5, E6, E7, E8, E9, F4, F5, F6, F9, F10	DGND	Ground		
A1, A2, A13, A14, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, E1, E2, E13, E14	JGND	Ground		
D4, D5, D10, D11	JVTT	Supply		1V supply for JESD204B
D6, D7, D8, D9	JVDD	Supply		1V supply for JESD204B
D12	JVDD2	Supply		2V supply for JESD204B
L3	TMU_AVDD2	Supply		2V analog supply for TMU.
G4	TMU_DVDD1	Supply		TMU digital domain supply.
M7, M8, N7, N8	Void			No balls at these locations

TYPICAL PERFORMANCE CHARACTERISTICS

AD9213-6G

Nominal supply voltages, 1.4 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, T_A = 25°C, 64k FFT

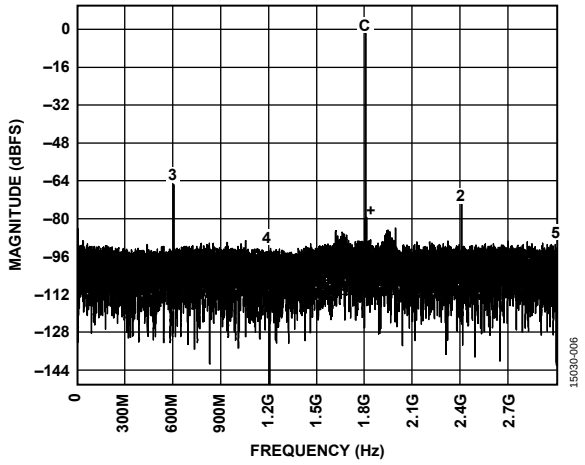

Figure 6. Single Tone FFT with Fin = 1.8 GHz, CLK = 6 GSPS

AD9213-10G

Nominal supply voltages, 1.4 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, T_A = 25°C, 64k FFT

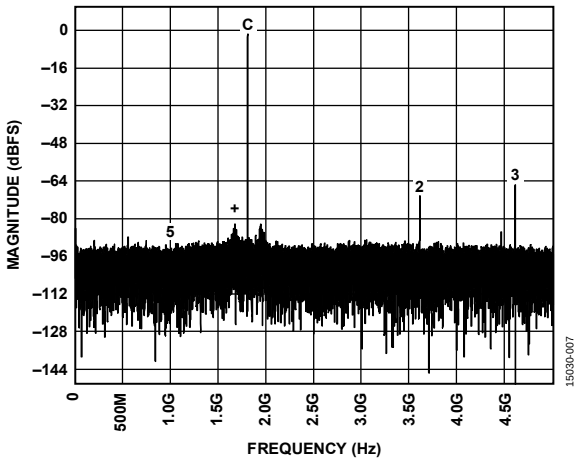

Figure 7. Tone FFT with Fin = 1.8 GHz, CLK = 10 GSPS

EQUIVALENT CIRCUITS

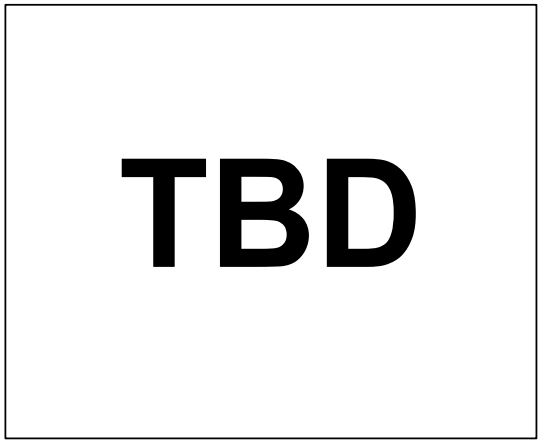

Figure 8. Analog Inputs

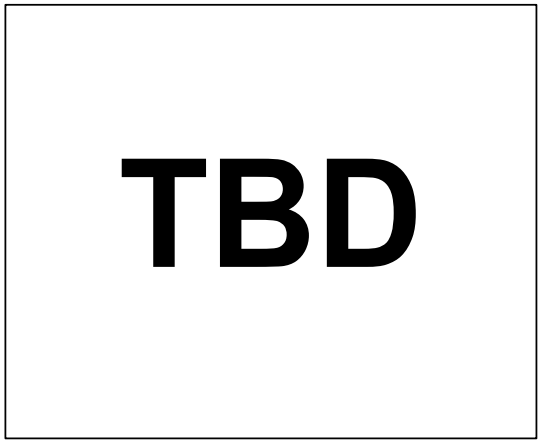

Figure 11.

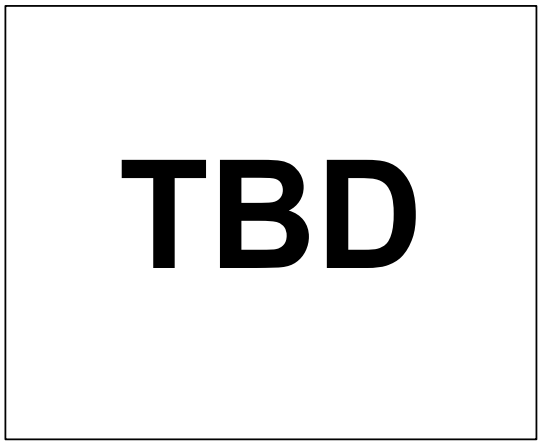

Figure 9.

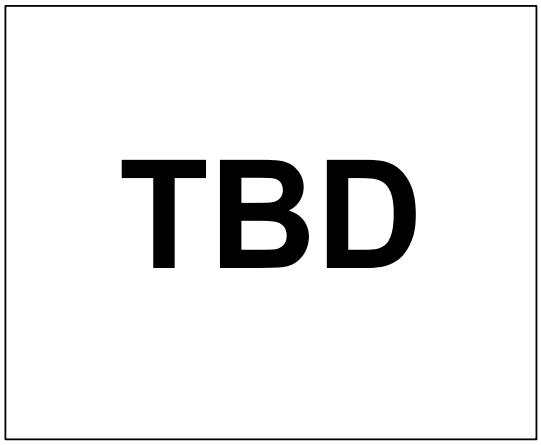

Figure 12. SYSREF± Inputs

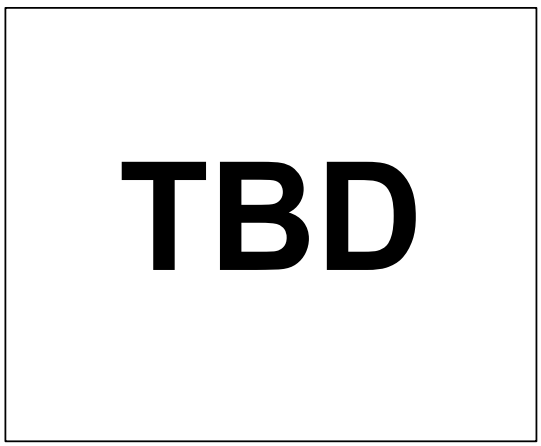

Figure 10. Clock Inputs

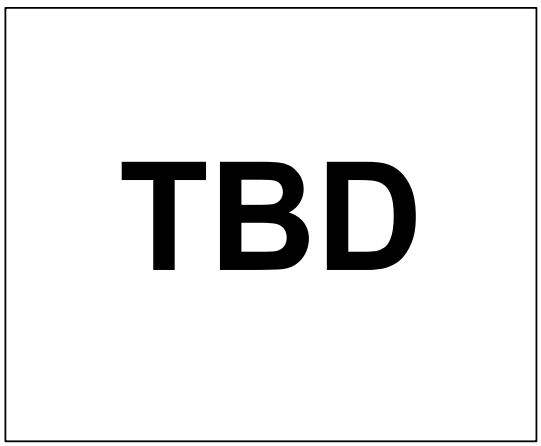

Figure 13.

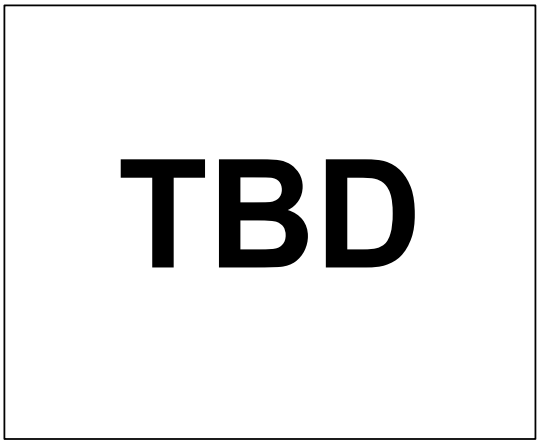

Figure 14. FD Output

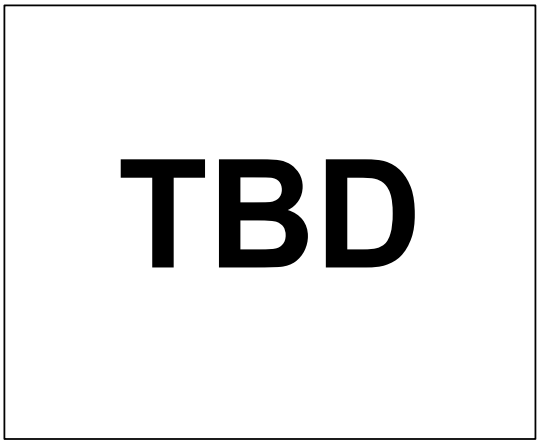

Figure 17.

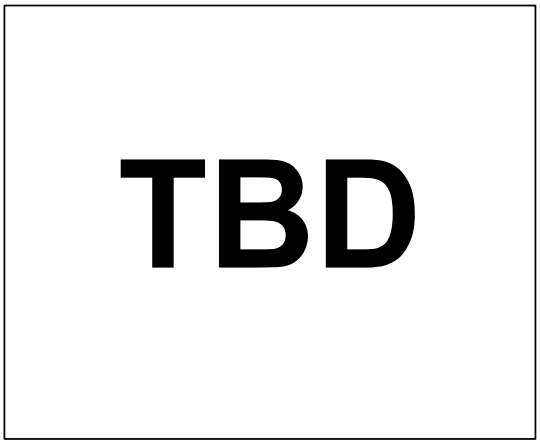

Figure 15.

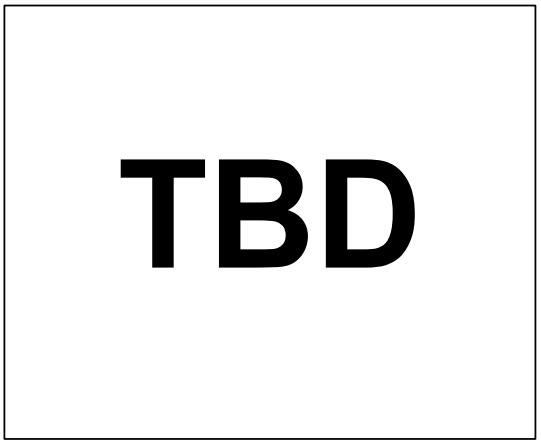

Figure 18.

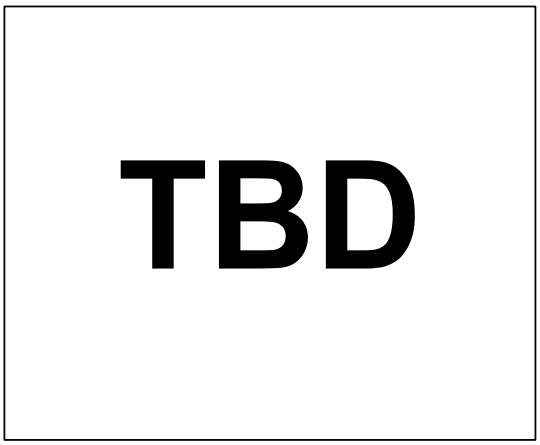

Figure 16. PDWN Input

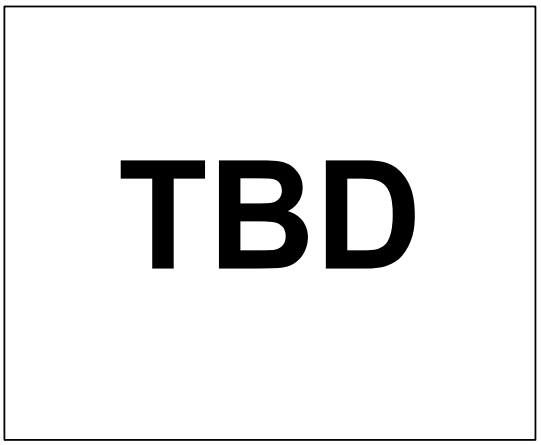

Figure 19.

THEORY OF OPERATION

The AD9213 is a single ADC with sixteen JESD204B output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 6.5 GHz. The AD9213 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The AD9213 analog input features wide input bandwidth supporting a variety of input ranges. An integrated voltage reference eases design considerations.

A programmable threshold detector allows monitoring of the signal power in the digital backend of the ADC. If the signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data lanes can be configured to multiple configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

ADC ARCHITECTURE

The architecture of the AD9213 consists of an input buffered pipelined ADC. The input buffer is designed to provide a termination impedance to the analog input signal of 50 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure xx. The input buffer is optimized for high linearity, low noise, and low power.

The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9213 is a differential buffer. The internal common-mode voltage of the buffer is AVDD/2 (nominally 0.5 V). The clock signal alternately switches the input circuit between sample mode and hold mode.

At radio frequencies, care must be taken when designing the network between the signal source and the AD9213 inputs.

Additional loading will affect bandwidth and possibly signal integrity. For more information, refer to the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the specific configuration and component values depend on the application.

For best dynamic performance, the source impedances driving VIN + x and VIN − x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Differential Input Configurations

There are several ways to drive the AD9213, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9213.

For low to midrange frequencies, a double balun or double transformer network is recommended for optimum performance of the AD9213. For higher frequencies it is better to remove some of the front-end passive components to ensure wideband operation.

Input Common Mode

The analog inputs of the AD9213 are internally biased to the common mode. In dc-coupled applications, the common-mode voltage of the signal source must be 0.5 V, ±TBD mV to ensure proper ADC operation. For these types of applications the input buffer has the option of disabling the internal biasing.

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD9213 is xx V p-p differential. Signals above this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9213. This internal 0.5 V reference is used to set the full-scale input range of the ADC.

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9213 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional external biasing.

Clock Synthesis

The AD9213 has a low jitter clock receiver with optional clock synthesis capability. The same clock receiver can be used for applying the sample clock as well as the reference clock for the internal PLL.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock signal. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = 20 \times \log 10 \left(2 \times \pi \times f_A \times t_J\right)$$

In this equation, the rms aperture jitter represents the root sum square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications.

Higher frequencies are increasingly sensitive to jitter (see Figure 20).

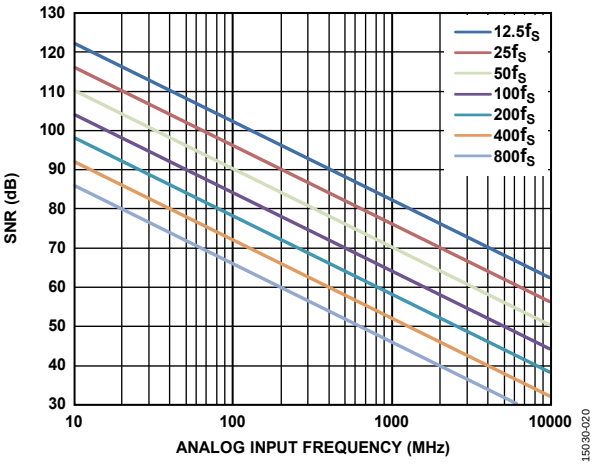

Figure 20. Ideal SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9213. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

Power-Down/Standby Mode

The AD9213 has a PDWN pin that can be used to configure the device in power-down or standby mode.

Temperature Diode and Sensor

The AD9213 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

A Temperature Measurement Unit is also designed into the AD9213.

ADC FAST DETECT

Highly pipelined converters can have significant latency. The AD9213 contains fast detect circuitry to monitor the converted signal amplitude crossing a threshold and assert the Fast Detect (FD) signal.

FAST THRESHOLD DETECTION (FD)

The FD bit is immediately set whenever the absolute value of the converted signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

DIGITAL DOWNCONVERTER (DDC)

The AD9213 includes a digital data path that can be configured for direct real data, down converted real data, or down converted complex IQ data. For the DDC data path, the NCO provides 48-bit overall Frequency Tuning Word (FTW) resolution. The decimation filter can be configured for 2^N complex decimation where N = 1 to 7 as well as 3×2^M complex decimation where M = 1 to 5.

The registers needed to configure the AD9213 DDC are Register 0x606, Register 0x607 Register 0x631. Descriptions of these registers are in the Memory Map section. The following table shows the AD9213 decimation modes and associated register settings.

Table 9 No Decimation, Full Bandwidth (Default)

Chip Configurations	Number of Virtual Converters Required	Chip Application Layer Mode (0x606 Bit0)	Real/Complex (0x606 Bit5)	Chip Decimation Ratio (DCM) (0x607)	DDC Decimation Ratio (0x631)	Register Settings
1 ADC	1	Full Bandwidth Mode	Don't Care	1	N/A	Register 0x606 = 0x00 Register 0x607 = 0x00 Register 0x631 = 0x00

Table 10. Real (I only)

Chip Configurations	Number of Virtual Converters Required	Chip Application Layer Mode (0x606 Bit0)	Real/Complex (0x606 Bit5)	Chip Decimation Ratio (DCM) (0x607)	DDC Decimation Ratio (0x631)	Register Settings
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	1	2	Register 0x606 = 0x21 Register 0x607 = 0x00 Register 0x630 = 0x10 Register 0x631 = 0x00
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	2	4	Register 0x606 = 0x21 Register 0x607 = 0x01 Register 0x630 = 0x10 Register 0x631 = 0x01
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	4	8	Register 0x606 = 0x21 Register 0x607 = 0x02 Register 0x630 = 0x10 Register 0x631 = 0x02
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	8	16	Register 0x606 = 0x21 Register 0x607 = 0x03 Register 0x630 = 0x10 Register 0x631 = 0x03
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	16	32	Register 0x606 = 0x21 Register 0x607 = 0x04 Register 0x630 = 0x10 Register 0x631 = 0x04
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	32	64	Register 0x606 = 0x21 Register 0x607 = 0x05 Register 0x630 = 0x10 Register 0x631 = 0x05
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	64	128	Register 0x606 = 0x21 Register 0x607 = 0x06 Register 0x630 = 0x10 Register 0x631 = 0x06
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	3	6	Register 0x606 = 0x21 Register 0x607 = 0x09 Register 0x630 = 0x10 Register 0x631 = 0x08
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	6	12	Register 0x606 = 0x21 Register 0x607 = 0x0A Register 0x630 = 0x10 Register 0x631 = 0x09

Chip Configurations	Number of Virtual Converters Required	Chip Application Layer Mode (0x606 Bit0)	Real/Complex (0x606 Bit5)	Chip Decimation Ratio (DCM) (0x607)	DDC Decimation Ratio (0x631)	Register Settings
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	12	24	Register 0x606 = 0x21 Register 0x607 = 0x0B Register 0x630 = 0x10 Register 0x631 = 0x0A
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	24	48	Register 0x606 = 0x21 Register 0x607 = 0x0C Register 0x630 = 0x10 Register 0x631 = 0x0B
1 ADC + 1 DDC (I Only)	1	DDC Mode	Real (I Only)	48	96	Register 0x606 = 0x21 Register 0x607 = 0x0D Register 0x630 = 0x10 Register 0x631 = 0x0C

Table 11. Complex (I/Q)

Chip Configurations	Number of Virtual Converters Required	Chip Application Layer Mode (0x606 Bit0)	Real/Complex (0x606 Bit5)	Chip Decimation Ratio (DCM) (0x607)	DDC Decimation Ratio (0x631)	Register Settings
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	2	2	Register 0x606 = 0x01 Register 0x607 = 0x01 Register 0x631 = 0x00
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	4	4	Register 0x606 = 0x01 Register 0x607 = 0x02 Register 0x631 = 0x01
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	8	8	Register 0x606 = 0x01 Register 0x607 = 0x03 Register 0x631 = 0x02
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	16	16	Register 0x606 = 0x01 Register 0x607 = 0x04 Register 0x631 = 0x03
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	32	32	Register 0x606 = 0x01 Register 0x607 = 0x05 Register 0x631 = 0x04
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	64	64	Register 0x606 = 0x01 Register 0x607 = 0x06 Register 0x631 = 0x05
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	128	128	Register 0x606 = 0x01 Register 0x607 = 0x07 Register 0x631 = 0x06
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	6	6	Register 0x606 = 0x01 Register 0x607 = 0x0A Register 0x631 = 0x08
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	12	12	Register 0x606 = 0x01 Register 0x607 = 0x0B Register 0x631 = 0x09
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	24	24	Register 0x606 = 0x01 Register 0x607 = 0x0C Register 0x631 = 0x0A
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	48	48	Register 0x606 = 0x01 Register 0x607 = 0x0D Register 0x631 = 0x0B
1 ADC + 1 DDC (I/Q)	2	DDC Mode	Complex (I/Q)	96	96	Register 0x606 = 0x01 Register 0x607 = 0x0E Register 0x631 = 0x0C

NUMERICALLY CONTROLLED OSCILLATOR (NCO)

The NCO frequency is set to a 48bit level of accuracy by setting the contents of Registers 0x634, 0x635, 0x636, 0x637, 0x638 and 0x639. These registers are six 8-bit registers that make up a 48-bit Frequency Tuning Word (FTW). Register 0x639 contains the most-significant-word; Register 0x634 contains the least-significant-word.

The value of the FTW is calculated using this formula:

$$FTW = \text{round}\left(2^{48}\frac{\text{mod}(f_C, f_S)}{f_S}\right)$$

where:

FTW is the 48-bit twos complement number representing the NCO FTW.
f_S is the ADC sampling frequency.
f_C is the desired NCO carrier frequency.
mod(*x*,*y*) is the remainder function which returns the remainder after division of x by y. For example mod(110,100) = 10.
round(*x*) is the rounding function which rounds x to the nearest integer. For example round(3.6) = 4.

For example, if for the desired f_S and f_C, FTW = 0xFEDCBA987654, the FTW is set by the following register writes:

- Write Register 0x634 = 0x54
- Write Register 0x635 = 0x76
- Write Register 0x636 = 0x98
- Write Register 0x637 = 0xBA
- Write Register 0x638 = 0xDC
- Write Register 0x639 = 0xFE

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9213 digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9213 to a digital processing device over a serial interface with lane rates of up to 16 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD9213 JESD204B data transmit block maps one physical ADC or, one or two virtual converters (when DDC is enabled) over a link. A link can be configured to use up to 16 JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9213 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes/converter device (lanes/link) (AD9213 value = 1, 2, 4, 8, 16, 3, 6, 12)
- M is the number of converters/converter device (virtual converters/link) (AD9213 value = 1, 2)
- F is the octets/frame (AD9213 value = 1, 2, 4)
- N′ is the number of bits per sample (JESD204B word size) (AD9213 value = 8, 12 or 16)
- N is the converter resolution (AD9213 value = 7 to 16)
- CS is the number of control bits/sample (AD9213 value = 0, 1, 2, or 3)
- K is the number of frames per multiframe, K = 32 is supported for all S
- K = 16, 32 is supported for configurations except when S = 1 and TBD, in which case, only K = 32 is supported
- S is the samples transmitted/single converter/frame cycle (AD9213 value = set automatically based on L, M, F, and N′)
- HD is the high density mode (AD9213 = set automatically based on L, M, F, and N′)
- CF is the number of control words/frame clock cycle/converter device (AD9213 value = 0)

Figure 21 shows a simplified block diagram of the AD9213 JESD204B link. By default, the AD9213 is configured as one converter feeding all 16 lanes. The AD9213 allows other configurations that are set up via a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD9213, the 12-bit converter word is broken into two octets (eight bits of data). Bit x (MSB) through Bit x are in the first octet. The second octet contains Bit x through Bit x (LSB) and x tail bits. The tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8-bit/10-bit encoder. The 8-bit/10-bit encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 22 shows how the 12-bit data is taken from the ADC, how the tail bits are added, how the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 22 illustrates the default data format.

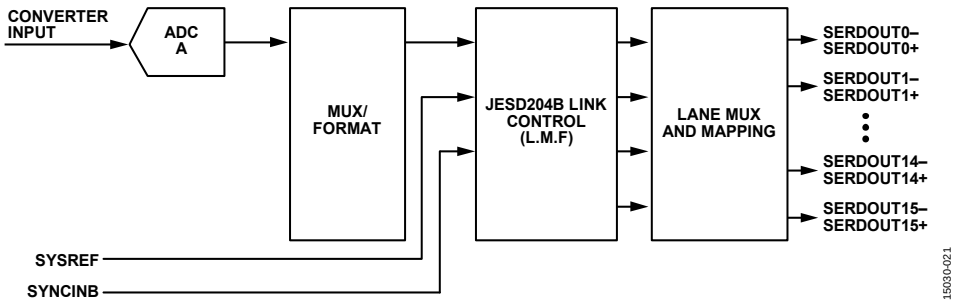

Figure 21. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x606 = 0x00)

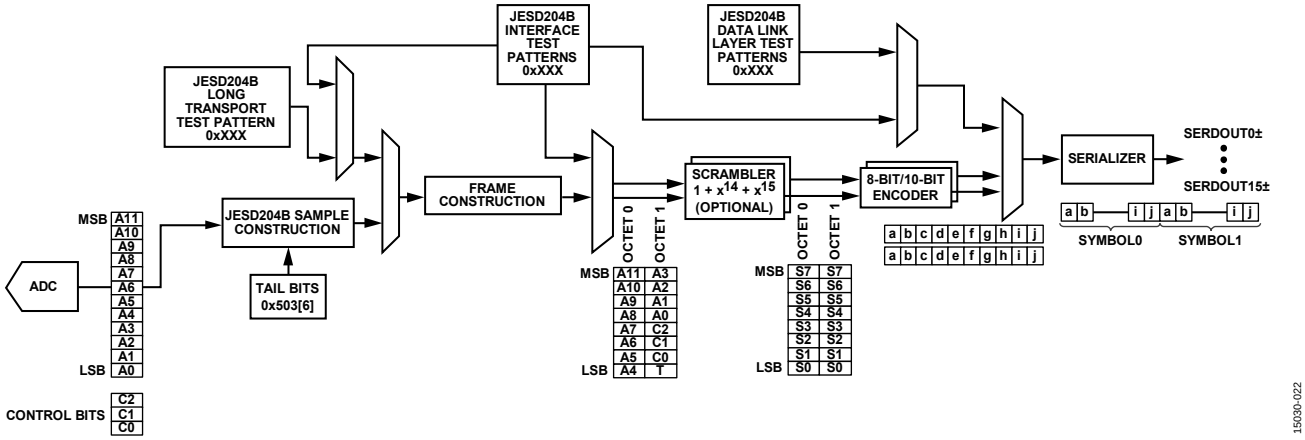

Figure 22. ADC Output Data Path Showing Data Framing (Conceptual Diagram)

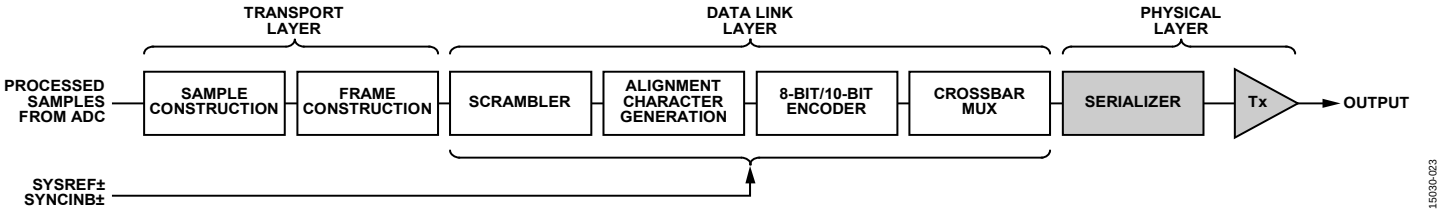

Figure 23. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 23 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. The following equation can be used to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters for multichip synchronization/lane alignment/monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one through sixteen lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD9213 JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in the JEDEC Standard 204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB±, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS) and SYNCINB±

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD9213 low. The JESD204B Tx then begins sending /K/ characters. Once the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The AD9213 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential dc-coupled LVDS mode signal by default, but it can also be driven single-ended.

For more information on configuring the SYNCINB± pin operation, refer to Register 0x508.

The SYNCINB± pins can also be configured to run in CMOS (single-ended) mode, by setting Bit[5] in Register 0x508. When running SYNCINB± in CMOS mode, connect the CMOS SYNCINB signal to Pin F1 (SYNCINB_P) and leave Pin G1 (SYNCINB_N) floating.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data will follow. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 24. The four multiframes include the following:

- Multiframe 1. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2. Begins with an /R/ character followed by a /Q/ character (/K28.4/), followed by link configuration parameters over 14 configuration octets (see Table 12) and ends with an /A/ character. Many of the parameter values are of the value – 1 notation.
- Multiframe 3. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

User Data and Error Detection

After the initial lane alignment sequence is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames are equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x503.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 12. The 8-bit/10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit/10-bit interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are troubleshooting tools for the verification of the digital front end (DFE). See the Memory Map section, Register 0x504[2:1] for information on configuring the 8-bit/10-bit encoder.

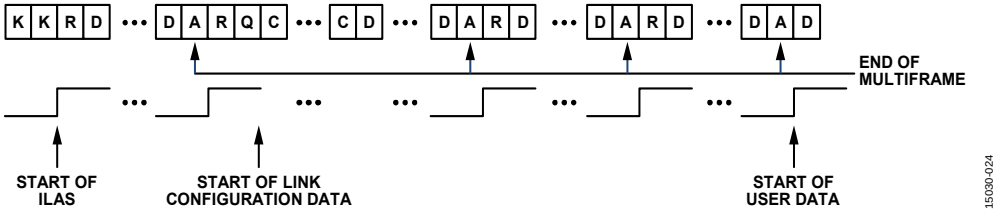

Figure 24. Initial Lane Alignment Sequence

Table 12. AD9213 Control Characters used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = –1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9213 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV p-p swing at the receiver (see Figure 25). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage is JVDD/2.

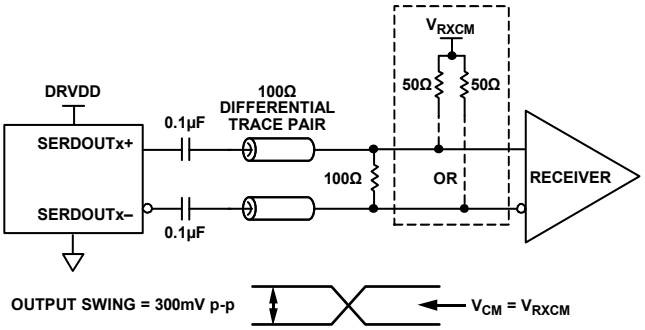

Figure 25. AC-Coupled Digital Output Termination Example

The AD9213 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible.

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors can result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and of equal lengths.

Figure 26 to Figure 31 show examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve for one AD9213 lane running at x Gbps and x Gbps, respectively. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x622).

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link can cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it can increase electromagnetic interference (EMI). See the Memory Map section (Register 0x551 to Register 0x556 in Table 19) for more details.

Phase-Locked Loop

The phase-locked loop (PLL) is used to generate the serializer clock, which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL locked status bit (Register 0x4BF, Bit 7). This read only bit lets the user know if the PLL has achieved a lock for the specific setup. The JESD204B lane rate control, Bit x of Register 0xxxx, must be set to correspond with the lane rate.

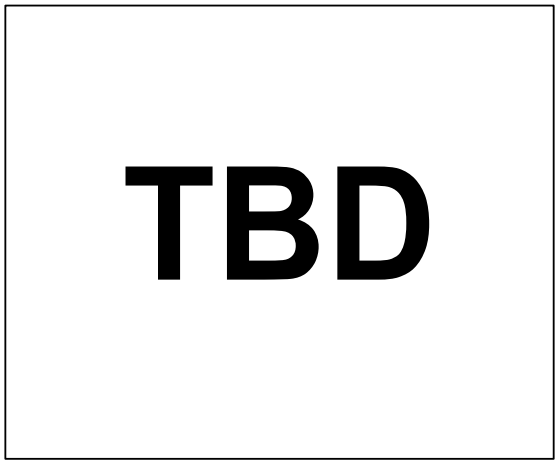

Figure 26. Digital Outputs Data Eye, External 100 Ω Terminations at 16 Gbps

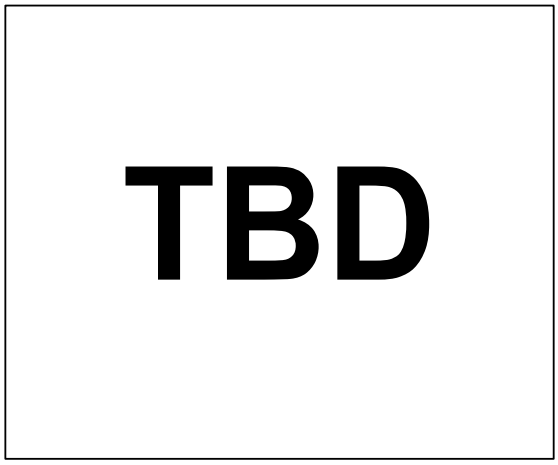

Figure 29. Digital Outputs Data Eye, External 100 Ω Terminations at 12.5 Gbps

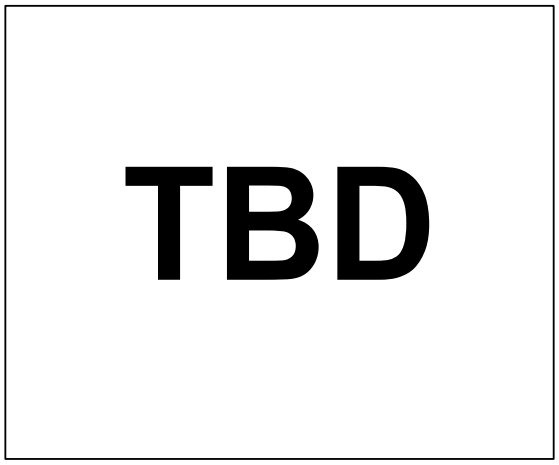

Figure 27. Digital Outputs Histogram, External 100 Ω Terminations at 16 Gbps

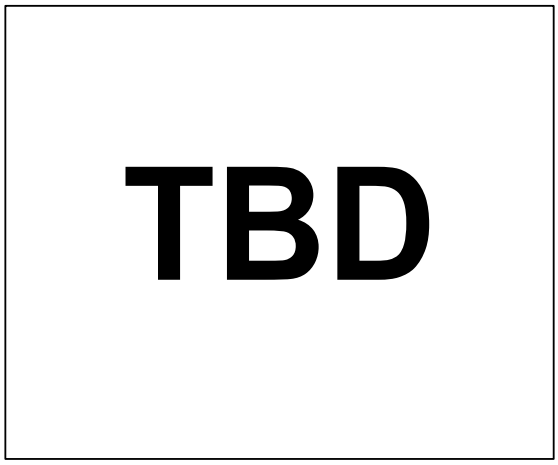

Figure 30. Digital Outputs Histogram, External 100 Ω Terminations at 12.5 Gbps

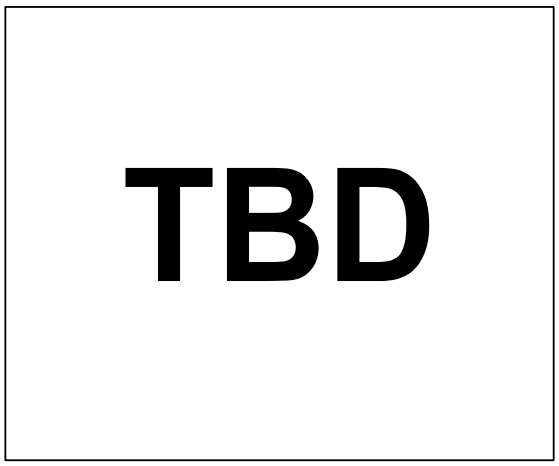

Figure 28. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 16 Gbps

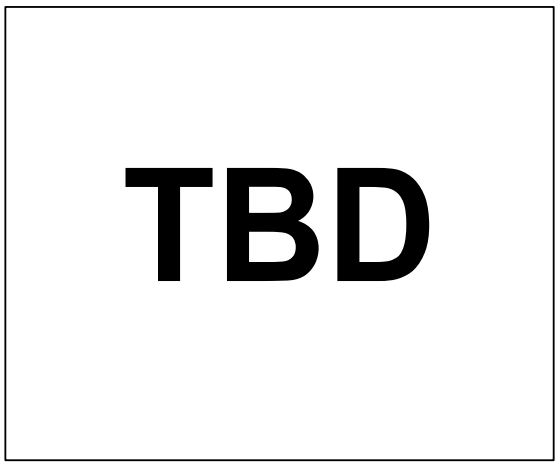

Figure 31. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 12.5 Gbps

SETTING UP THE AD9213 DIGITAL INTERFACE

In order to ensure proper operation of the AD9213 at startup, some SPI writes are needed to initialize the link. Additionally, these registers need to be written every time the ADC is reset . Any one of the following resets warrant the initialization routine for the digital interface:

- Hard reset as in power up
- Power up using PDWN pin
- Power up using SPI (0x02[1:0])
- SPI Soft Reset (0xXXXX = 0xXX)
- Data path soft reset (0x1507 = 0x07)
- JESD204B link power cycle (0xXXXX = 0xXX, then 0xXX)

The initialization SPI writes are as shown in Table 13:

Table 13. AD9213 JESD204B Initialization

Register	Value	Comment
0xXXXX	0xXX	
0xXXXX	0xXX	
0xXXXX	0xXX	
0xXXXX	0xXX	
0xXXXX	0xXX	
0xXXXX	0xXX	
0xXXXX	0xXX	

The AD9213 has one JESD204B link. The device offers an easy way to set up the JESD204B link through the JESD204B quick configuration register (Register 0x502). The serial outputs (SERDOUT0± to SERDOUT15±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are:

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDC is used for on-chip digital processing, M represents the number of virtual converters. The virtual converter mapping setup is shown in TBD Section.

The maximum lane rate allowed by the AD9213 is 16 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$Lane\ Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where:

$$f_{OUT} = \frac{f_{ADC\_CLOCK}}{Decimation\ Ratio}$$

The decimation ratio (DCM) is the parameter programmed in Register 0x631.

The following steps can be used to configure the output:

1. Power down the link.
2. Select JESD204B link configuration options.
3. Configure detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.
7. Initialize the JESD204B link by issuing the commands in Table 13.

If the lane line rate calculated is less than X Gbps, select the low line rate option by programming a value of 0xXX to Register 0x500.

Table 14, Table 15, and Table 16 show the JESD204B output configurations supported for N′ = 16, N′ = 12 and N′ = 8 for a given number of virtual converters. Take care to ensure that the serial line rate for a given configuration is within the supported range of X Gbps to 16 Gbps.

JESD204B Transport Layer Settings

In Table 14, Table 15, and Table 16, the JESD204B transport layer descriptions are as follows:

- L = Number of lanes/converter device (Lanes per link)
- M = Number of Virtual Converters/converter device (Virtual Converters per link).
- F = Octets per lane in a frame
- S = Samples transmitted/Virtual Converter/frame cycle
- HD = High Density Mode
- N = Virtual Converter Resolution (in bits)
- N'= Total number of bits per sample (JESD word size)
- CS = Number of control bits/conversion sample
- K = Number of frames per multi-frame

Serial Line Rates

In Table 14, Table 15, and Table 16, the serial line rates are as follows:

- Fin = ADC Sample Rate
- CDR = Chip Decimation Ratio
- Fout = Output Sample Rate = Fin / CDR.
- SLR = JESD204B Serial Line Rate
- The following equations must be met due to internal clock divider requirements:
- SLR ≥ 390 Mbps and SLR ≤ 16000 Mbps.
- SLR/40 ≤ Fin
- 20 × CDR × f_{OUT} / SLR ≤ 512
- When the SLR is ≤ 16000 Mbps and > 12500 Mbps, the Low Line Rate mode must set to VCO post divide by 1 with no bit repeat (set bits [7:4] to 0x3). When the SLR is ≤ 12500 Mbps and ≥ 6250 Mbps, the Low Line Rate mode must set to VCO post divide by 2 with no bit repeat (set bits [7:4] to 0x0). When the SLR is < 6250 Mbps and ≥ 3125 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with no bit repeat (set bits [7:4] to 0x1).

When the SLR is < 3125 Mbps and ≥ 1562.5 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with bit repeat by 2(set bits [7:4] to 0x5 in). When the SLR < 1562.5 Mbps and ≥ 781.25 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with bit repeat by 4(set bits [7:4] to 0x9). When the SLR is < 781.25 Mbps and ≥ 390.0625 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with bit repeat by 4(set bits [7:4] to 0xD).

K Settings

In Table 14, Table 15, and Table 16, the number of samples per converter per frame cycle, S is calculated as follows:

- $S = 8 \times F \times L/(N' \times M)$
- K = 32 is supported for all S
- K = 16, 32 is supported for configurations except when S = 1 and C2R = 1 in which case, only K = 32 is supported.

Table 14. JESD204B Output Configurations (N' = 16)

No. of Virtual Converters Supported (Same Value as M)	JESD Serial Line Rate[1]	DCM Supported[2]	JESD204B Transport Layer Settings[3]								
			L	M	F	S	HD	N	N'	CS	K
1	20 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	1	2	1	0	8-16	16	0-3	See the K Settings section
	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	1	1	1	8-16	16	0-3	See the K Settings section
	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	2	2	0	8-16	16	0-3	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	1	1	2	1	8-16	16	0-3	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	1	2	4	0	8-16	16	0-3	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	1	1	4	1	8-16	16	0-3	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	1	2	8	0	8-16	16	0-3	See the K Settings section
	1.25 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	16	1	1	8	1	8-16	16	0-3	See the K Settings section
	1.25 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	16	1	2	16	0	8-16	16	0-3	See the K Settings section
2	40 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	2	4	1	0	8-16	16	0-3	See the K Settings section
	20 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	2	2	1	0	8-16	16	0-3	See the K Settings section
	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	1	1	1	8-16	16	0-3	See the K Settings section
	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	2	2	0	8-16	16	0-3	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	8	2	1	2	1	8-16	16	0-3	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	8	2	2	4	0	8-16	16	0-3	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	16	2	1	4	1	8-16	16	0-3	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	16	2	2	8	0	8-16	16	0-3	See the K Settings section

[1] See the Serial Line Rates section for full definitions and conditions.
[2] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.
[3] See the JESD204B Transport Layer Settings section for full definitions.

Table 15. JESD204B Output Configurations (N'=12)

No. of Virtual Converters Supported (Same Value as M)	JESD Serial Line Rate[1]	DCM Supported[2]	JESD204B Transport Layer Settings[3]								
			L	M	F	S	HD	N	N'	CS	K
1	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	3	1	1	2	1	8-12	12	0-3	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	6	1	1	4	1	8-12	12	0-3	See the K Settings section
	1.25 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	12	1	1	8	1	8-12	12	0-3	See the K Settings section
2	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	3	2	1	1	1	8-12	12	0-3	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	6	2	1	2	1	8-12	12	0-3	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	12	2	1	4	1	8-12	12	0-3	See the K Settings section

[1] See the Serial Line Rates section for full definitions and conditions.
[2] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.
[3] See the JESD204B Transport Layer Settings section for full definitions.

Table 16. JESD204B Output Configurations (N'=8)

No. of Virtual Converters Supported (Same Value as M)	Serial Line Rate[1]	DCM Supported[2]	JESD204B Transport Layer Settings[3]								
			L	M	F	S	HD	N	N'	CS	K
1	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	1	1	1	0	7-8	8	0-1	See the K Settings section
	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	1	2	2	0	7-8	8	0-1	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	1	2	0	7-8	8	0-1	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	2	4	0	7-8	8	0-1	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	1	4	8	0	7-8	8	0-1	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	4	1	1	4	0	7-8	8	0-1	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	4	1	2	8	0	7-8	8	0-1	See the K Settings section
	1.25 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	8	1	1	8	0	7-8	8	0-1	See the K Settings section
	1.25 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32	8	1	2	16	0	7-8	8	0-1	See the K Settings section
2	20 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	1	2	2	1	0	7-8	8	0-1	See the K Settings section
	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	2	1	1	0	7-8	8	0-1	See the K Settings section
	10 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	2	2	2	2	0	7-8	8	0-1	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	1	2	0	7-8	8	0-1	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	2	4	0	7-8	8	0-1	See the K Settings section
	5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96, 128	4	2	4	8	0	7-8	8	0-1	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	2	1	4	0	7-8	8	0-1	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	2	2	8	0	7-8	8	0-1	See the K Settings section
	2.5 × F_{OUT}	1, 2, 4, 6, 8, 12, 16, 24, 32, 48, 64	8	2	4	16	0	7-8	8	0-1	See the K Settings section

[1] See the Serial Line Rates section for full definitions and conditions.
[2] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.
[3] See the JESD204B Transport Layer Settings section for full definitions.

FSx MODE

The basic intention of FSX mode is to have the lane rate be 1x of the sample rate. FSX1 mode has L=16.

With 10 GSPS sampling, lane rate can be 10 GHz with all lanes of JESD in use (L=16).

In FSX modes, data from the DFORMAT (internal) block output is available as 4 samples of 12-bit data in every cycle of a div4x_clk (which is at 625 MHz for a 10 GSPS sampling example). This data needs to be re-packed as 4 samples of 16-bit data (including 4 control bits) in every cycle of a div5x_clk(500 MHz for a 10 GSPS example).

The four control bits would indicate if a sysref timestamp was present along with any of the input samples. The input is also expected to contain one bit of sysref_timestamp along with each 12b sample in div4x_domain.

The general data repacking scheme in FSX mode is as shown in Figure 32.

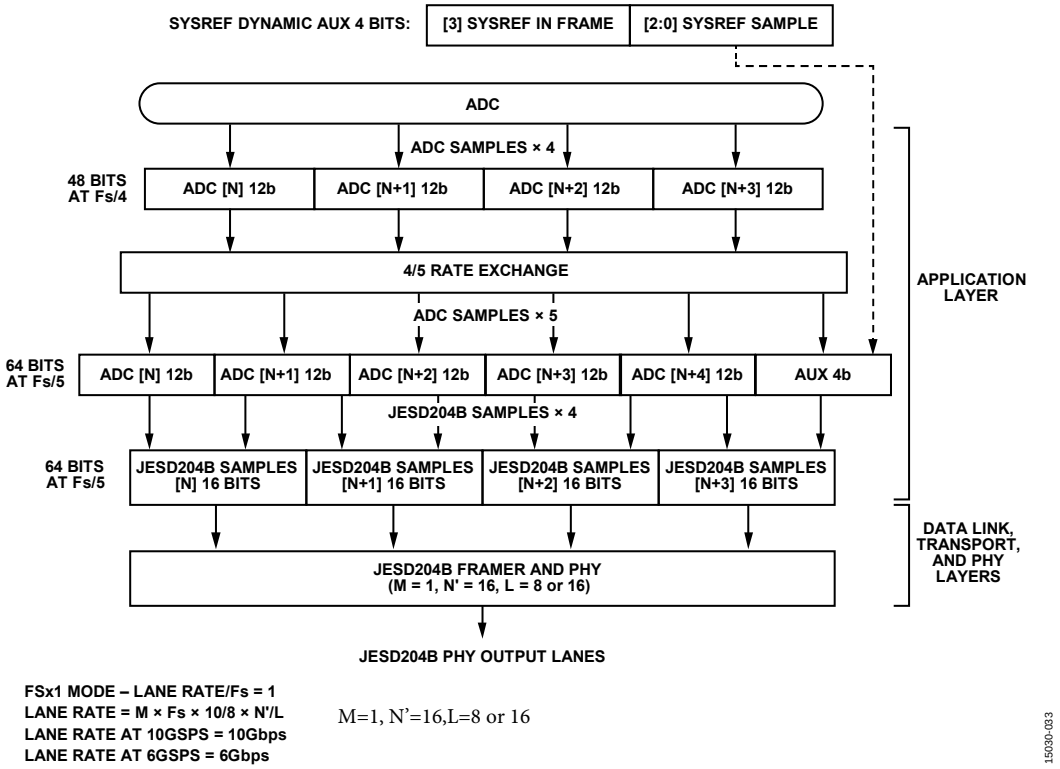

Figure 32 Data Flow in FSx Modes (Example of FSx1 Shown)

Four auxiliary bits are added to five 12-bit samples to make up 64 bits, which are then handed over as four 16-bit samples to JESD. These four control bits are present as the MSB 4 bits of each 64-bit group. Information on the four control bits is as follows:

Table 17. AUXCTRL

Bit 3	Bits[2:0]
1 = > One sysref timestamp was present in any of the five 12b samples in the group. 0 => No sysref timestamp was present in any of the five 12b samples in the group.	The sample number (1, 2, 3 4 or 5) in which the 3'b001 => Nth sample had sysref 3'b010 => N+1th sample had sysref 3'b011 => N+2th sample had sysref 3'b101 => N+3th sample had sysref 3'b101 => N+4th sample had sysref

The 64-bit data group can be indicated as follows:

MSB					LSB
AUXCTRL	N+4	N+3	N+2	N+1	N

FSx1 MODE:

PLL clock division ratios are as follows:

- pll_pre_div = 3'd1 - A pre division of 2
- pll_pre_div3_en = 1'b1
- pll_fb_div = 7'h6 – A feedback div factor of 48

PROGRAMMING IN FSx MODE

FSx mode can be enabled via the FSX_CTRL register (Register 0x680) as shown in Figure 33. Setting FSX_MODE bit to 1 enables FSx mode. In FSx mode, JTX should be programmed with N'=16. The DFORMAT output resolution would be restricted to 12-bits. Only Full-Bandwidth mode is supported with FSX enabled. DDC modes are not supported. Hence, JTX_M parameter would be 1 (only 1 virtual converter). JTX_L parameter could be programmed for 6 lanes for FSX1 mode.

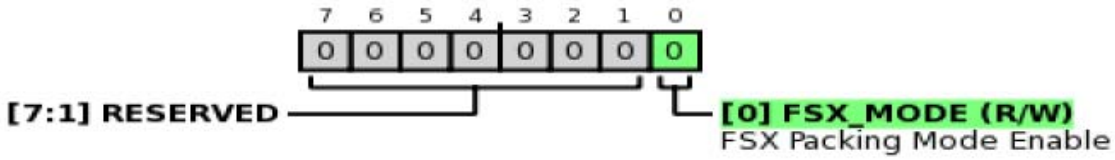

Figure 33. Enable FSx Mode via the FSX_CTRL Register (Register 0x680)

JTX CONFIGURATION FOR FSx MODE

JESD204B Transport Layer Settings

In Table 18, the JESD204B transport layer descriptions are as follows:

- L = Number of lanes/converter device (Lanes per link)
- M = Number of Virtual Converters/converter device (Virtual Converters per link).
- F = Octets per lane in a frame
- S = Samples transmitted/Virtual Converter/frame cycle
- HD = High Density Mode
- N = Virtual Converter Resolution (in bits)
- N'= Total number of bits per sample (JESD word size)
- CS = Number of control bits/conversion sample
- K = Number of frames per multiframe

Serial Line Rates

In Table 18, the serial line rates are as follows:

- Fin = ADC Sample Rate
- CDR = Chip Decimation Ratio = 1 for FSx modes
- F_{OUT} = Output Sample Rate = Fin / CDR = Fin
- SLR = JESD204B Serial Line Rate
- The following equations must be met due to internal clock divider requirements:
- SLR ≥ 390 Mbps and SLR ≤ 16000 Mbps.
- Other restrictions may come from allowed ADC sampling rates
- When the SLR is ≤ 16000 Mbps and > 12500 Mbps, the Low Line Rate mode must set to VCO post divide by 1 with no bit repeat (set bits [7:4] to 0x3). When the SLR is ≤ 12500 Mbps and ≥ 6250 Mbps, the Low Line Rate mode must set to VCO post divide by 2 with no bit repeat (set bits [7:4] to 0x0). When the SLR is < 6250 Mbps and ≥ 3125 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with no bit repeat (set bits [7:4] to 0x1). When the SLR is < 3125 Mbps and ≥ 1562.5 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with bit repeat by 2(set bits [7:4] to 0x5 in). When the SLR < 1562.5 Mbps and ≥ 781.25 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with bit repeat by 4(set bits [7:4] to 0x9). When the SLR is < 781.25 Mbps and ≥ 390.0625 Mbps, the Low Line Rate mode must be set to VCO post divide by 4 with bit repeat by 4(set bits [7:4] to 0xD).

K Settings

Number of samples per converter per frame cycle, S is calculated as follows:

- S = 8 × F × L / (N' × M)
- K = 32 will be supported for all S
- K = 16, 32 will be supported for configurations except when S = 1 and C2R = 1 in which case, only K = 32 will be supported.

Table 18.

Number of Virtual Converters Supported (Same Value as M)	FSx Mode	JESD Serial Line Rate[1]	DCM Supported	JESD204B Transport Layer Settings[2]								
				L	M	F	S	HD	N	N'	CS	K
1	FSx1	Fin	1	16	1	1	8	1	16	16	0	See the K Settings section
	FSx1	Fin	1	16	1	2	16	0	16	16	0	See the K Settings section

[1] See the Serial Line Rates section for full definitions and conditions.
[2] See the JESD204B Transport Layer Settings section for full definitions.

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to non-repeatable latencies across the link from one power cycle or link reset to the next. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9213 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x525[5] sets the subclass mode for the AD9213 and its default is set for subclass 1 operating mode (0x525[5] = 1). If deterministic latency is not a system requirement, subclass 0 operation is recommended and the SYSREF signal may not be required. Even in subclass 0 mode, the SYSREF signal may be required in an application where multiple AD9213 devices need to be synchronized with each other. This topic is addressed in the "Using SYREF as a Time Stamp" section (not yet included).

SUBCLASS 0 OPERATION

If there is no requirement for multi-chip synchronization while operating in subclass 0 mode (0x525[5] = 0), the SYSREF input can be left disconnected. In this mode, the relationship of the 204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the receiver's ability to capture and align the lanes within the link.

SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames and multiframes as described in the "Transport Layer" section of this document. The local multiframe clock (LMFC) is synchronous with the beginnings of these multiframes. In subclass 1 operation, the SYSREF is used to synchronize the LMFCs for each device in a link or across multiple links (within the AD9213, SYSREF also synchronizes the internal sample dividers). This is illustrated in Figure *34*. The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and also to achieve a fixed latency between power cycles and link reset conditions.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links and devices must be ≤ 1 LMFC periods (see Figure *34*). This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Setting Deterministic Latency Registers

The JESD204B receive buffer in the logic device will buffer data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, it is possible that from one power cycle to the next, the data arrival time at the receive buffer may straddle an LMFC boundary. In order to ensure deterministic latency in this case, a phase adjustment of the LMFC at either the transmitter or receiver will need to be performed. Typically, adjustments to accommodate the receive buffer are made to the receiver's LMFC. In the AD9213, this adjustment can be made using the LMFC Offset register (0x50A[4:0]). This register will delay the LMFC in frame clock increments, depending on the "F" parameter (# of octets per lane per frame). For F = 1, every 4th setting (0, 4, 8, …) will result in a 1-frame clock shift. For F = 2, every other setting (0, 2, 4, …) will result in a 1-frame clock shift. For all other values of F, each setting results in a 1-frame clock shift. Figure *35* shows that, in the case where the link latency is near an LMFC boundary, the AD9213's local LMFC can be delayed in order to delay the data arrival time at the receiver. Figure *36* shows how the receiver's LMFC is delayed to accommodate the receive buffer timing. Consult the applicable JESD204B receiver user guide for details on making this adjustment. If the total latency in the system is not near an integer multiple of the LMFC period or if the appropriate adjustments have been made to the LMFC phase at the clock source, it is still possible to have variable latency from one power cycle to the next. In this case, users should check for the possibility that the setup and hold time requirements for the SYSREF are not being met. This can be checked by reading the SYSREF Setup/Hold Monitor register (0x1509). This function is fully described in the "SYSREF± Setup/Hold Window Monitor" section (not included yet).

If reading register 0x1509 indicates you may have a timing problem, there are a couple of adjustments that can made in the AD9213. Changing the SYSREF level that is used for alignment is possible using the SYSREF transition select bit (0x1508[1]). Also, changing which edge of CLK is used to capture SYSREF can be done using the CLK edge select bit (0x1508[0]). Both of these options are described in the SYSREF control features section (not included yet). If neither of these measures help achieve an acceptable setup and hold time, adjusting the phase of SYSREF and/or the device clock (CLK+/-) may be required.

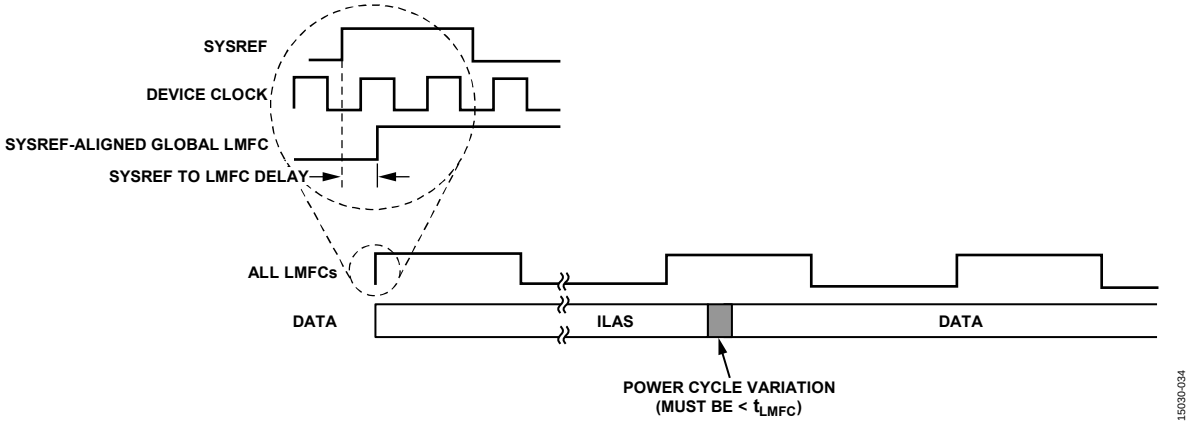

Figure 34. SYSREF and LMFC

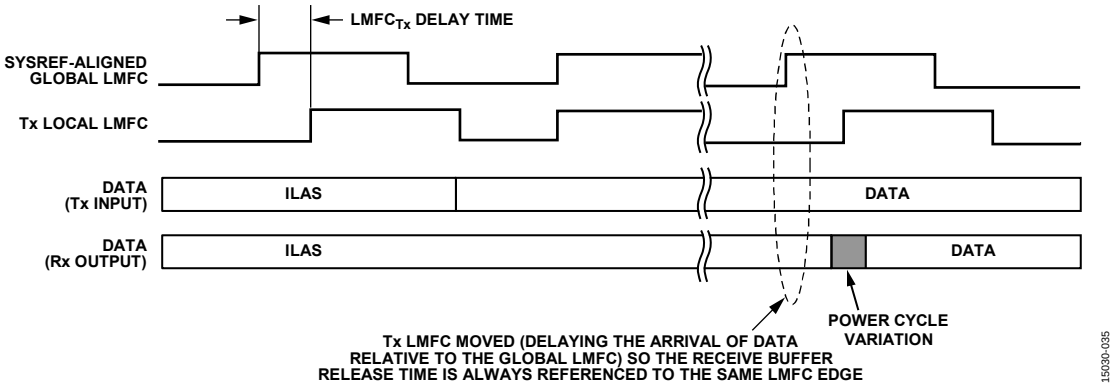

Figure 35. Adjusting the 204B Tx LMFC in the AD9213

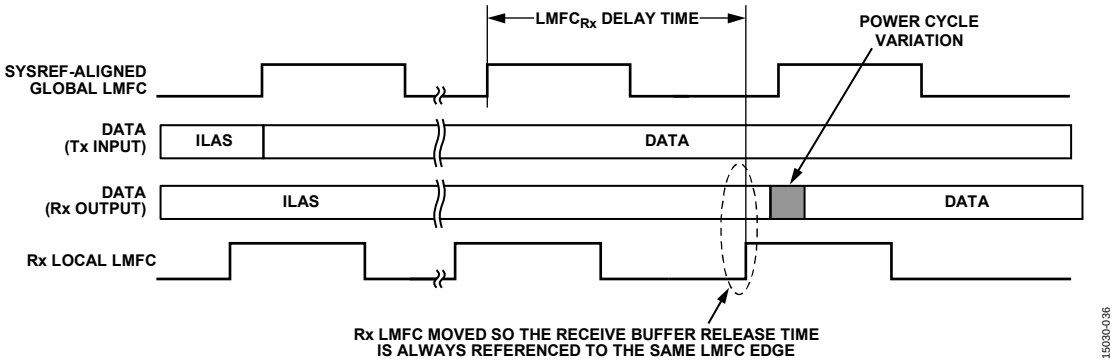

Figure 36. Adjusting the 204B Rx LMFC in the Logic Device

MULTICHIP SYNCHRONIZATION

The AD9213 has a JESD204B subclass1 compatible SYSREF± input that provides flexible options for synchronizing the internal blocks of the AD9213. The SYSREF± input is a source synchronous system reference signal used to align the boundaries of local clocks in the device that enables multichip synchronization between multiple AD9213s. The input clock divider, DDC, signal monitor block, and JESD204B link can be synchronized using the SYSREF± input.

The AD9213 incorporates two SYSREF operating modes: SAMPLED SYSREF MODE and AVERAGED SYSREF MODE. The SPI is used to select between these modes.

SAMPLED SYSREF MODE

In Sampled Mode, SYSREF± operates as a standard JESD204B Subclass1 signal. Some characteristics of Sampled SYSREF synchronization:

- Synchronous sampling of SYSREF
- Must meet Setup/Hold time requirements for reliable synchronization. This is increasingly difficult to achieve as the sample rate increases.
- SYSREF jitter must be much less than one sample clock period. SYSREF coming from ASICs or FPGAs can have significant jitter.

Because Setup and Hold time requirements with respect to the sample clock must be met for Sampled Mode to properly synchronize multiple devices, Sampled Mode will not operate properly at the full sample rate of the AD9213.

For multi-chip synchronization at full sample rate, Averaged Mode must be used.

AVERAGED SYSREF MODE

In Averaged SYSREF Mode, the averaging function determines the phase of SYSREF. This information is used to regenerate an internal version. This averaged version is tolerant to random jitter on external SYSREF and is used to synchronize other downstream blocks within the ADC. Multiple AD9213s will each use their respective internally regenerated averaged local SYSREF signals. Some characteristics of Averaged SYSREF synchronization:

- Uses time-to-digital converters and filtering to recover phase of SYSREF and create a clean internal local version.
- Assumes SYSREF is continuous or in pulse trains
- No sampling issues due to Setup/Hold time violations
- Timing is recovered from the averaged waveform
- Extends JESD204B Subclass1 to the full sample rate of the AD9213.
- Jitter tolerant; jitter on SYSREF is cleaned-up by averaging of SYSREF timing.

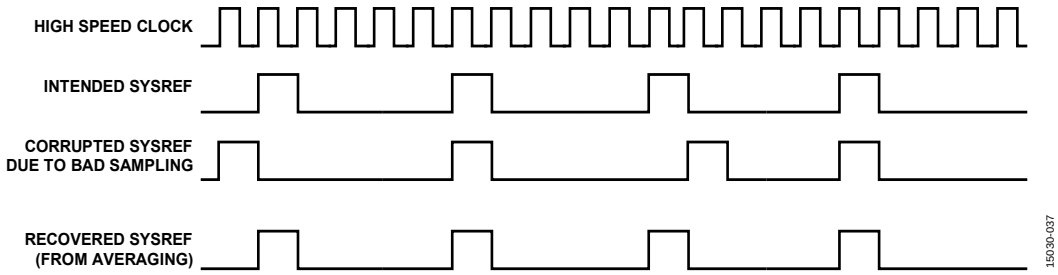

Figure 37. Conceptual Illustration of Recovered SYSREF

TEST MODES

ADC TEST MODES

The AD9213 has various test options that aid in the system level implementation. The AD9213 has ADC test modes that are available in Register 0xXXX. These test modes are described in Table XX. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not.

SERIAL PORT INTERFACE

The AD9213 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLES

Table 19 documents the default hexadecimal value for each hexadecimal address shown. All address locations that are not included in Table 19 are not currently supported for this device and should not be written.

Open and Reserved Locations

All address and bit locations that are not included in Table 19 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned. If the entire address location is open, do not write to this address location.

Default Values

After the AD9213 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 19.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- X denotes a don't care bit.

SPI Soft Reset

After issuing a soft reset by programming Register 0x000, the AD9213 requires x ms to recover. When programming the AD9213 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

REGISTER DETAILS: SYSTEM CONTROL SIGNALS (SPI_ONLY_REGMAP)

Table 19. Memory Map Register

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x20	SPI_BASE_ADDRn	[7:0]	spi_base_addr		32 bits SPI Base address bits [0, 7].	0x0	R/W
0x26	GEN_CTRL	[7:4]	RESERVED		Reserved.	0x1	R
		3	clk_switch		set to 1 for ADC to run off external clock	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R

REGISTER DETAILS: (USER_CTRL)

Table 20. Memory Map Register

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0333	scratch_shdw_reg0_cust	[7:2]	RESERVED		Reserved.	0x0	R
		1	wait_before_app_start		Value of '1' indicates to wait before start of app	0x0	R/W
		0	clock_sel		Value of '0' indicates that encode clock is to be used, '1' indicates the use of PLL	0x0	R/W
0x1600	GPIO_control	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	GPIO_profile		Define which GPIO profile to use	0x0	R/W
0x1601	cal_control	[7:1]	RESERVED		Reserved.	0x0	R
		0	cal_freeze		Freeze bit to halt BG cals	0x0	R/W
0x1620	mcs_tdc_mux_sel	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	mcs_tdc_b_mux_sel		Tdc B mux select, 0: sysref_out, 1: sysref_buf_in, 2: sysref_capture_out, 3:trig_buf_in	0x0	R/W
		[1:0]	mcs_tdc_a_mux_sel		Tdc A mux select, 0: sysref_buf_in, 1: sysref_out, 2:trig_buf_in, 3: sysref_capture_out	0x0	R/W
0x1621	mcs_mode	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	mcs_mode		0: sampled_sysref using custom ff, 1: sampled_sysref using other capture 2: averaging mode, 4: bidirectional sysref mode	0x0	R/W
0x1622	mcs_ctrl	[7:2]	RESERVED		Reserved.	0x0	R
		1	mcs_lock_en		Enable MCS to phase slip and lock within one sample clock period	0x0	R/W
		0	mcs_sync_en		Signal another SYNC event when not in one of the continuous modes	0x0	R/W
0x1633	mcs_bidir_ctrl	[7:1]	RESERVED		Reserved.	0x0	R
		0	mcs_bidir_count_done		Flag to indicate sysref bidirectional count is reached	0x0	R/W
0x1636	mcs_phase_slip_mode	[7:1]	RESERVED		Reserved.	0x0	R
		0	mcs_phase_slip_mode		if this bit is high, the phase slip will be applied for encode clk to ana_ctrl_dig, else configure the timestamp in the dp regmap	0x0	R/W

REGISTER DETAILS: (AD9213_CUST_SPI_REGMAP)

Table 21. Memory Map Register

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x100	fd_ctrl	[7:3]	RESERVED		Reserved.	0x0	R
		2	fd_fine_en		Enable fast detect on corrected ADC data	0x0	R/W
		1	fd_force_val		Force value for the fast detect	0x0	R/W
		0	fd_force		Force the fast detect output pin	0x0	R/W
0x101	fd_up_thresh_lsb	[7:0]	fd_up_thresh[7:0]		Fast Detect upper threshold unsigned	0x0	R/W
0x102	fd_up_thresh_msb	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	fd_up_thresh[10:8]		Fast Detect upper threshold unsigned	0x0	R/W
0x103	fd_low_thresh_lsb	[7:0]	fd_low_thresh[7:0]		Fast Detect lower threshold unsigned	0x0	R/W
0x104	fd_low_thresh_msb	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	fd_low_thresh[10:8]		Fast Detect lower threshold unsigned	0x0	R/W
0x105	fd_dwell_thresh_lsb	[7:0]	fd_dwell_thresh[7:0]		Fast Detect dwell time counter target	0x0	R/W
0x106	fd_dwell_thresh_msb	[7:0]	fd_dwell_thresh[15:8]		Fast Detect dwell time counter target	0x0	R/W
0x120	smon_statusn	[7:0]	smon_status		20 bits Signal Monitor Serial Data Output bits	0x0	R
0x123	smon_status_fcnt	[7:0]	smon_status_fcnt		Signal Monitor Frame counter. Increments whenever period counter expires	0x0	R
0x124	smon_period_0	[7:0]	smon_period[7:0]		24 bit value sets no. of clock cycles over which signal monitor performs operation	0x0	R/W
0x125	smon_period_1	[7:0]	smon_period[15:8]		24 bit value sets no. of clock cycles over which signal monitor performs operation	0x0	R/W
0x126	smon_period_2	[7:0]	smon_period[23:16]		24 bit value sets no. of clock cycles over which signal monitor performs operation	0x0	R/W
0x127	smon_status_ctrl	[7:5]	RESERVED		Reserved.	0x0	R
		4	smon_peak_en		Signal Monitor Peak Detector Enable	0x0	R/W
		[3:1]	smon_status_rdsel		Signal Monitor Status Read-back selection. 0x1 for Peak detector	0x0	R/W
		0	smon_status_update		A high transition on this signal will cause the status value to change in the regmap	0x0	R/W
0x128	smon_sframer	[7:2]	smon_sframer_insel		Signal Monitor Serial Framer Input Selection	0x0	R/W
		1	smon_sframer_mode		Signal Monitor Serial Framer Mode Selection	0x0	R/W
		0	smon_sframer_en		Signal Monitor Serial Framer Enable	0x0	R/W
0x129	smon_sync_ctrl	[7:2]	RESERVED		Reserved.	0x0	R
		1	smon_sync_next		SMON Next Synchronization Mode- 0: Continuous mode, 1: Next Synchronization Mode	0x0	R/W
		0	smon_sync_en		SMON Synchronization Enable	0x0	R/W
0x130	clk4_dis	[7:1]	RESERVED		Reserved.	0x0	R
		0	clk4_dis		Disables the div4 clock output from ana_ctrl_dig	0x0	R/W

REGISTER DETAILS: (MAIN_REGMAP)

Table 22. Memory Map Register

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0	SPI_CONFIG_A	7	soft_reset_1		SPI soft reset	0x0	R/W
		6	lsb_first_1		SPI Lsb first	0x0	R/W
		5	addr_ascension_1		SPI Address Increment	0x0	R/W
		4	sdo_active_1		SPI SDO Enable	0x0	R/W
		3	sdo_active_0		SPI SDO Enable	0x0	R/W
		2	addr_ascension_0		SPI address Increment	0x0	R/W
		1	lsb_first_0		SPI Lsb first	0x0	R/W
		0	soft_reset_0		SPI soft Reset	0x0	R/W
0x2	DEVICE_CONFIG	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	op_mode		Operating Mode	0x0	R/W
				00	Normal operation.		
				01	Normal operation with reduced power and corresponding performance.		
				10	Standby mode.		
				11	Sleep (powerdown) mode.		
0x3	CHIP_TYPE	[7:0]	chip_type		Chip Type: 0x03: High Speed ADCs	0x0	R
0x4	CHIP_ID_LSB	[7:0]	chip_id[7:0]		Chip ID	0x0	R
0x5	CHIP_ID_MSB	[7:0]	chip_id[15:8]		Chip ID	0x0	R
0x6	CHIP_GRADE	[7:4]	chip_speed_grade		Chip Speed Grade	0x0	R
		[3:0]	chip_die_rev		Chip Die Revision (undocumented to customer)	0x0	R
0x8	DEVICE_INDEX1	[7:0]	dev_index1		Offset pointer or lsb of the device index register. Offset pointer or device index	0x0	R/W
0x9	DEVICE_INDEX2	[7:0]	dev_index2		Offset pointer or lsb of the device index register. Offset pointer or device index	0x0	R/W
0xA	CHIP_SCRATCH	[7:0]	chip_scratch		Chip Scratch-Pad Register. Used to provide a consistent memory location for software debug.	0x0	R/W
0xB	SPI_REVISION	[7:0]	spi_revision		SPI Revision Register (undocumented to customer) 0x00: Draft 0.9e or earlier 0x01: Revision 1.0 0x02-0xFF: Undefined	0x1	R
0xC	VENDOR_ID_LSB	[7:0]	chip_vendor_id[7:0]		Vendor ID	0x56	R
0xD	VENDOR_ID_MSB	[7:0]	chip_vendor_id[15:8]		Vendor ID	0x4	R

REGISTER DETAILS

Table 23. Memory Map Register

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x500	PLL_CTRL	7	jtx_pll_bypass_lock		bypass pll lock input	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R
		[3:0]	jtx_low_line_rate		JESD Low Line Rate Selection	0x0	R/W
				0011	Normal Serializer Mode, VCO Post-Divide by 1 option.		
				0111	Bit Repeat by 2, VCO Post-Divide by 1 option.		
				1011	Bit Repeat by 4, VCO Post-Divide by 1 option.		
				1111	Bit Repeat by 8, VCO Post-Divide by 1 option.		
				0000	Normal Serializer Mode, VCO Post-Divide by 2 option.		
				0100	Bit Repeat by 2, VCO Post-Divide by 2 option.		
				1000	Bit Repeat by 4, VCO Post-Divide by 2 option.		
				1100	Bit Repeat by 8, VCO Post-Divide by 2 option.		
				0001	Normal Serializer Mode, VCO Post-Divide by 4 option.		
				0101	Bit Repeat by 2, VCO Post-Divide by 4 option.		
				1001	Bit Repeat by 4, VCO Post-Divide by 4 option.		
				1101	Bit Repeat by 8, VCO Post-Divide by 4 option.		
0x501	PLL_STATUS	7	jtx_pll_locked		PLL Locked Status Bit	0x0	R
		[6:0]	RESERVED		Reserved.	0x0	R
0x502	JTX_QUICK_CFG	[7:0]	jtx_quick_cfg		JTX Quick Configuration	0x81	R/W
0x503	JTX_LINK_CTRL1	7	jtx_link_stdby_mode		JESD204x Standby Mode	0x0	R/W
		6	jtx_tail_pn_en		JESD204x Serial Tail Bit PN Enable	0x0	R/W
		5	jtx_test_sample_en		JESD204x Serial Test Sample Enable	0x0	R/W
		4	jtx_lsync_en		JESD204x Serial Lane Synchronization Enable	0x1	R/W
		[3:2]	jtx_ilas_mode		JESD204x Serial Initial Lane Alignment Sequence Mode	0x1	R/W
		1	jtx_faci_disable		JESD204x Serial Frame Alignment Character Insertion (FACI) Disable	0x0	R/W
		0	jtx_link_pd		JESD204x Serial Transmit Link Power Down (active high)	0x0	R/W
0x504	JTX_LINK_CTRL2	[7:6]	jtx_sync_pin_mode		JESD204x Serial Sync Mode	0x0	R/W
		5	jtx_sync_pin_inv		JESD204x Serial Sync Pin Invert	0x0	R/W
		4	jtx_sync_pin_type		JESD204x Serial Sync Pin Logic Type	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		2	jtx_8b10b_bypass		JESD204x Serial 8b/10b Bypass (Test Mode Only)	0x0	R/W
		1	jtx_10b_inv		JESD204x 10b Serial Transmit Bit Invert	0x0	R/W
		0	jtx_10b_mirror		JESD204x 10b Serial Transmit Bit Mirror	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x505	JESD204B Link Control 3	[7:6]	Checksum mode			0x0	R/W
				00	Checksum is the sum of all 8-bit registers in the link configuration table.		
				01	Checksum is the sum of all individual link configuration fields (LSB aligned).		
				10	Checksum is disabled (set to zero). For test purposes only.		
				11	Unused.		
		[5:4]	Test injection point			0x0	R/W
				0	N' sample input.		
				1	10-bit data at 8-bit/10-bit output (for PHY testing).		
				10	8-bit data at scrambler input.		
		[3:0]	JESD204B test mode patterns			0x0	R/W
				0	Normal operation (test mode disabled).		
				1	Alternating checkerboard.		
				10	1/0 word toggle.		
				11	31-bit pseudorandom number (PN) sequence: $x^{31} + x^{28} + 1$.		
				100	23-bit PN sequence: $x^{23} + x^{18} + 1$.		
				101	15-bit PN sequence: $x^{15} + x^{14} + 1$.		
				110	9-bit PN sequence: $x^{9} + x^{5} + 1$.		
				111	7-bit PN sequence: $x^{7} + x^{6} + 1$.		
				1000	Ramp output.		
				1110	Continuous/repeat user test.		
				1111	Single user test.		
0x506	JESD204B Link Control 4	[7:4]	ILAS delay			0x0	R/W
				0	Transmit ILAS on first LMFC after SYNCINB± deasserted.		
				1	Transmit ILAS on second LMFC after SYNCINB± deasserted.		
				10	Transmit ILAS on third LMFC after SYNCINB± deasserted.		
				11	Transmit ILAS on fourth LMFC after SYNCINB± deasserted.		
				100	Transmit ILAS on fifth LMFC after SYNCINB± deasserted.		
				101	Transmit ILAS on sixth LMFC after SYNCINB± deasserted.		
				110	Transmit ILAS on seventh LMFC after SYNCINB± deasserted.		
				111	Transmit ILAS on eighth LMFC after SYNCINB± deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB± deasserted.		
				1001	Transmit ILAS on tenth LMFC after SYNCINB± deasserted.		
				1010	Transmit ILAS on eleventh LMFC after SYNCINB± deasserted.		
				1011	Transmit ILAS on twelfth LMFC after SYNCINB± deasserted.		
				1100	Transmit ILAS on thirteenth LMFC after SYNCINB± deasserted.		
				1101	Transmit ILAS on fourteenth LMFC after SYNCINB± deasserted.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1110	Transmit ILAS on fifteenth LMFC after SYNCINB± deasserted.		
				1111	Transmit ILAS on sixteenth LMFC after SYNCINB± deasserted.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode			0x0	R/W
				000	Normal operation (link layer test mode disabled).		
				001	Continuous sequence of /D21.5/ characters.		
				010	Reserved.		
				011	Reserved.		
				100	Modified RPAT test sequence.		
				101	JSPAT test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
0x507	JTX_LINK_CTRL5	[7:0]	jtx_ilas_cnt		Initial Lane Alignment Sequence Count	0x0	R/W
0x508	JTX_SYNC_CTRL	7	RESERVED		Reserved.	0x0	R
		6	spi_pd_syncb		power down sync	0x0	R/W
		5	spi_cmos_en_rc		sync pin cmos en	0x0	R/W
		[4:3]	spi_syncb_ibias_rc		sync pin ibias control	0x0	R/W
		[2:0]	spi_syncb_vcm_rc		sync pin vcm control	0x0	R/W
0x509	JTX_CS_BITS_CTRL	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	jtx_cs_bits_mode		jtx control bits mode	0x0	R/W
0x50A	JTX_LMFC_OFFSET	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lmfc_offset		Local Multi-Frame Clock (LMFC) Phase Offset Value.	0x0	R/W
0x50B	JTX_LINK_BIST	[7:5]	RESERVED		Reserved.	0x0	R
		4	jtx_bist_length		JESD204x Built-In Self Test Length	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		2	jtx_bist_init		JESD204x Built-In Self Test Initialization	0x0	R/W
		1	RESERVED		Reserved.	0x0	R
		0	jtx_bist_en		JESD204x Link Built-In Self Test Enable	0x0	R/W
0x50C	JTX_LINK_CRC_LSB	[7:0]	jtx_bist_crc_lsb		Least Significant Cyclic Redundancy Check (CRC) Bits	0x0	R
0x50D	JTX_LINK_CRC_MSB	[7:0]	jtx_bist_crc_msb		Least Significant Cyclic Redundancy Check (CRC) Bits	0x0	R
0x50E	JTX_DID_CFG	[7:0]	jtx_did_cfg		JESD204x Serial Device Identification (DID) number.	0x0	R/W
0x50F	JTX_BID_CFG	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	jtx_bid_cfg		JESD204x Serial Bank Identification (BID) number. (extension to DID)	0x0	R/W
0x510	JTX_LID0_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid0_cfg		JESD204x Serial Lane Identification (LID) number	0x0	R/W
0x511	JTX_LID1_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid1_cfg		JESD204x Serial Lane Identification (LID) number.	0x1	R/W
0x512	JTX_LID2_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid2_cfg		JESD204x Serial Lane Identification (LID) number.	0x2	R/W
0x513	JTX_LID3_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid3_cfg		JESD204x Serial Lane Identification (LID) number.	0x3	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x514	JTX_LID4_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid4_cfg		JESD204x Serial Lane Identification (LID) number.	0x4	R/W
0x515	JTX_LID5_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid5_cfg		JESD204x Serial Lane Identification (LID) number.	0x5	R/W
0x516	JTX_LID6_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid6_cfg		JESD204x Serial Lane Identification (LID) number.	0x6	R/W
0x517	JTX_LID7_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid7_cfg		JESD204x Serial Lane Identification (LID) number.	0x7	R/W
0x518	JTX_LID8_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid8_cfg		JESD204x Serial Lane Identification (LID) number	0x8	R/W
0x519	JTX_LID9_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid9_cfg		JESD204x Serial Lane Identification (LID) number.	0x9	R/W
0x51A	JTX_LID10_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid10_cfg		JESD204x Serial Lane Identification (LID) number.	0xA	R/W
0x51B	JTX_LID11_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid11_cfg		JESD204x Serial Lane Identification (LID) number.	0xB	R/W
0x51C	JTX_LID12_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid12_cfg		JESD204x Serial Lane Identification (LID) number.	0xC	R/W
0x51D	JTX_LID13_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid13_cfg		JESD204x Serial Lane Identification (LID) number.	0xD	R/W
0x51E	JTX_LID14_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid14_cfg		JESD204x Serial Lane Identification (LID) number.	0xE	R/W
0x51F	JTX_LID15_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_lid15_cfg		JESD204x Serial Lane Identification (LID) number.	0xF	R/W
0x520	JTX_SCR_L_CFG	7	jtx_scr_cfg		JESD204x Serial Scrambler Mode (SCR=jtx_scr_cfg)	0x1	R/W
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_l_cfg		JESD204x Serial Lane Control (L=jtx_l_cfg+1)	0xF	R/W
0x521	JTX_F_CFG	[7:0]	jtx_f_cfg		JESD204x Number of Octets per frame (F = jtx_f_cfg + 1)	0x1	R/W
0x522	JTX_K_CFG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_k_cfg		JESD204x Number of frames per multiframe (K = jtx_k_cfg + 1). Only values where F*K which are divisible by 4 can be used.	0x1F	R/W
0x523	JTX_M_CFG	[7:0]	jtx_m_cfg		JESD204x Number of converters per link/device (M = jtx_m_cfg + 1)	0x0	R/W
0x524	JTX_CS_N_CFG	[7:6]	jtx_cs_cfg		JESD204x Number of control bits per sample.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_n_cfg		JESD204x Converter Resolution (N=jtx_n_cfg+1)	0xF	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x525	JTX_SCV_NP_CFG	[7:5]	jtx_subclassv_cfg		JESD204x Device Subclass Version	0x1	R/W
		[4:0]	jtx_np_cfg		JESD204x Total number of bits per sample (N'=jtx_np_cfg+1)	0xF	R/W
0x526	JTX_JV_S_CFG	[7:5]	jtx_jesdv_cfg		JESD204x Version(Only JESD204B support)	0x0	R
		[4:0]	jtx_s_cfg		JESD204x Samples Per Converter Frame Cycle (S=jtx_s_cfg+1)	0xF	R
0x527	JTX_HD_CF_CFG	7	jtx_hd_cfg		JESD204x High Density Format (HD)	0x0	R
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	jtx_cf_cfg		JESD204x Number of control words per frame clock cycle per link (CF=jtx_cf_cfg)	0x0	R
0x528	JTX_RES1_CFG	[7:0]	jtx_res1_cfg		JESD204x Serial Reserved Field #1 (RES1)	0x0	R/W
0x529	JTX_RES2_CFG	[7:0]	jtx_res2_cfg		JESD204x Serial Reserved Field #2 (RES2)	0x0	R/W
0x52A	JTX_ADJ_CFG	[7:6]	RESERVED		Reserved.	0x0	R
		5	jtx_phadj_cfg		Phase ADJ CFG	0x0	R/W
		4	jtx_adjdir_cfg		ADJ DIR CFG	0x0	R/W
		[3:0]	jtx_adjcnt_cfg		ADJ CNT CFG	0x0	R/W
0x52B	JTX_CHKSUM0_CFG	[7:0]	jtx_chksum0_cfg		JESD204x Serial Checksum Value of Lane 0	0xC3	R
0x52C	JTX_CHKSUM1_CFG	[7:0]	jtx_chksum1_cfg		JESD204x Serial Checksum Value of Lane 1	0xC4	R
0x52D	JTX_CHKSUM2_CFG	[7:0]	jtx_chksum2_cfg		JESD204x Serial Checksum Value of Lane 2	0xC5	R
0x52E	JTX_CHKSUM3_CFG	[7:0]	jtx_chksum3_cfg		JESD204x Serial Checksum Value of Lane 3	0xC6	R
0x52F	JTX_CHKSUM4_CFG	[7:0]	jtx_chksum4_cfg		JESD204x Serial Checksum Value of Lane 4	0xC7	R
0x530	JTX_CHKSUM5_CFG	[7:0]	jtx_chksum5_cfg		JESD204x Serial Checksum Value of Lane 5	0xC8	R
0x531	JTX_CHKSUM6_CFG	[7:0]	jtx_chksum6_cfg		JESD204x Serial Checksum Value of Lane 6	0xC9	R
0x532	JTX_CHKSUM7_CFG	[7:0]	jtx_chksum7_cfg		JESD204x Serial Checksum Value of Lane 7	0xCA	R
0x533	JTX_CHKSUM8_CFG	[7:0]	jtx_chksum8_cfg		JESD204x Serial Checksum Value of Lane 8	0x0	R
0x534	JTX_CHKSUM9_CFG	[7:0]	jtx_chksum9_cfg		JESD204x Serial Checksum Value of Lane 9	0x0	R
0x535	JTX_CHKSUM10_CFG	[7:0]	jtx_chksum10_cfg		JESD204x Serial Checksum Value of Lane 10	0x0	R
0x536	JTX_CHKSUM11_CFG	[7:0]	jtx_chksum11_cfg		JESD204x Serial Checksum Value of Lane 11	0x0	R
0x537	JTX_CHKSUM12_CFG	[7:0]	jtx_chksum12_cfg		JESD204x Serial Checksum Value of Lane 12	0x0	R
0x538	JTX_CHKSUM13_CFG	[7:0]	jtx_chksum13_cfg		JESD204x Serial Checksum Value of Lane 13	0x0	R
0x539	JTX_CHKSUM14_CFG	[7:0]	jtx_chksum14_cfg		JESD204x Serial Checksum Value of Lane 14	0x0	R
0x53A	JTX_CHKSUM15_CFG	[7:0]	jtx_chksum15_cfg		JESD204x Serial Checksum Value of Lane 15	0x0	R
0x53B	JTX_LANE_PDWN	[7:0]	jtx_force_lane_pd[7:0]		Physical Lane Force Power Down	0x0	R/W
0x53C	JTX_LANE_PDWN2	[7:0]	jtx_force_lane_pd[15:8]		Physical Lane Force Power Down	0x0	R/W
0x53D	JTX_LANE_ASSIGN1	[7:4]	jtx_lane_assign_1		Physical Lane Assignment	0x1	R/W
		[3:0]	jtx_lane_assign_0		Physical Lane Assignment	0x0	R/W
0x53E	JTX_LANE_ASSIGN2	[7:4]	jtx_lane_assign_3		Physical Lane Assignment	0x3	R/W
		[3:0]	jtx_lane_assign_2		Physical Lane Assignment	0x2	R/W
0x53F	JTX_LANE_ASSIGN3	[7:4]	jtx_lane_assign_5		Physical Lane Assignment	0x5	R/W
		[3:0]	jtx_lane_assign_4		Physical Lane Assignment	0x4	R/W
0x540	JTX_LANE_ASSIGN4	[7:4]	jtx_lane_assign_7		Physical Lane Assignment	0x7	R/W
		[3:0]	jtx_lane_assign_6		Physical Lane Assignment	0x6	R/W
0x541	JTX_LANE_ASSIGN5	[7:4]	jtx_lane_assign_9		Physical Lane Assignment	0x9	R/W
		[3:0]	jtx_lane_assign_8		Physical Lane Assignment	0x8	R/W
0x542	JTX_LANE_ASSIGN6	[7:4]	jtx_lane_assign_11		Physical Lane Assignment	0xB	R/W
		[3:0]	jtx_lane_assign_10		Physical Lane Assignment	0xA	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x543	JTX_LANE_ASSIGN7	[7:4]	jtx_lane_assign_13		Physical Lane Assignment	0xD	R/W
		[3:0]	jtx_lane_assign_12		Physical Lane Assignment	0xC	R/W
0x544	JTX_LANE_ASSIGN8	[7:4]	jtx_lane_assign_15		Physical Lane Assignment	0xF	R/W
		[3:0]	jtx_lane_assign_14		Physical Lane Assignment	0xE	R/W
0x545	JTX_ENG_LANE_PDWN	[7:0]	jtx_eng_force_lane_pd[7:0]		Engineering lane power down	0x0	R/W
0x546	JTX_ENG_LANE_PDWN2	[7:0]	jtx_eng_force_lane_pd[15:8]		Engineering lane power down	0x0	R/W
0x547	JTX_QBF_STATUS	[7:0]	jtx_qbf_status		QBF Status	0x0	R
0x550	SER_DRV_ADJUST	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	ser_iswing_bit		Sets swing control of output driver	0xF	R/W
0x551	SER_PREEMPH_SEL	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	ser_preemph_sel		Preemphas control setting for all channels	0x0	R/W
0x552	SER_PREEMPH_EN	[7:0]	ser_preemph_en		Preemphas control setting for all channels	0x0	R/W
0x553	SER_PREEMPH_CTRL1	[7:4]	ser_preemph_extra_ctrl_ch0_1		Extra Tap Weight factor added to ser_preemph_ctrl for nonlinear control in MOAD	0x0	R/W
		[3:0]	ser_preemph_ctrl_ch0_1		Tap Weight factor of pre-emphasis in XOR	0x0	R/W
0x554	SER_PREEMPH_CTRL2	[7:4]	ser_preemph_extra_ctrl_ch2_3		Extra Tap Weight factor added to ser_preemph_ctrl for nonlinear control in MOAD	0x0	R/W
		[3:0]	ser_preemph_ctrl_ch2_3		Tap Weight factor of pre-emphasis in XOR	0x0	R/W
0x555	SER_PREEMPH_CTRL3	[7:4]	ser_preemph_extra_ctrl_ch4_5		Extra Tap Weight factor added to ser_preemph_ctrl for nonlinear control in MOAD	0x0	R/W
		[3:0]	ser_preemph_ctrl_ch4_5		Tap Weight factor of pre-emphasis in XOR	0x0	R/W
0x556	SER_PREEMPH_CTRL4	[7:4]	ser_preemph_extra_ctrl_ch6_7		Extra Tap Weight factor added to ser_preemph_ctrl for nonlinear control in MOAD	0x0	R/W
		[3:0]	ser_preemph_ctrl_ch6_7		Tap Weight factor of pre-emphasis in XOR	0x0	R/W
0x557	JTX_TEST_GEN_INV	[7:1]	RESERVED		Reserved.	0x0	R
		0	jtx_test_gen_inv		JESD Test Generator Invert	0x0	R/W
0x558	CHIP_USR_PAT_1_7_0	[7:0]	chip_usr_pat_1_7_0		chip_usr_pat_1	0x0	R/W
0x559	CHIP_USR_PAT_1_15_8	[7:0]	chip_usr_pat_1_15_8		chip_usr_pat_1	0x0	R/W
0x55A	CHIP_USR_PAT_2_7_0	[7:0]	chip_usr_pat_2_7_0		chip_usr_pat_2	0x0	R/W
0x55B	CHIP_USR_PAT_2_15_8	[7:0]	chip_usr_pat_2_15_8		chip_usr_pat_2	0x0	R/W
0x55C	CHIP_USR_PAT_3_7_0	[7:0]	chip_usr_pat_3_7_0		chip_usr_pat_3	0x0	R/W
0x55D	CHIP_USR_PAT_3_15_8	[7:0]	chip_usr_pat_3_15_8		chip_usr_pat_3	0x0	R/W
0x55E	CHIP_USR_PAT_4_7_0	[7:0]	chip_usr_pat_4_7_0		chip_usr_pat_4	0x0	R/W
0x55F	CHIP_USR_PAT_4_15_8	[7:0]	chip_usr_pat_4_15_8		chip_usr_pat_4	0x0	R/W
0x560	SER_PARITY_RESET_EN1	[7:0]	ser_parity_reset_en[7:0]		Parity reset enable	0x0	R/W
0x561	SER_PARITY_RESET_EN2	[7:0]	ser_parity_reset_en[15:8]		Parity reset enable	0x0	R/W
0x564	SER_PARITY_ERR1	[7:0]	ser_parity_err[7:0]		Parity error	0x0	R
0x565	SER_PARITY_ERR2	[7:0]	ser_parity_err[15:8]		Parity error	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x566	LMFC_CTL	[7:5]	RESERVED		Reserved.	0x0	R
		4	lmfc_div_edge		Which edge of LMFC is used for division before sending out of GPIO. 0 for posedge	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		[2:0]	lmfc_out_div		Divider value before passing LMFC out of GPIO	0x0	R/W
0x567	FORCE_LINK_RESET_REG	[7:1]	RESERVED		Reserved.	0x0	R
		0	force_link_reset		Force link reset from Regmap	0x0	R/W
0x570	PLL_ENABLE_CTRL	0	pwrup_lcpll		Power up JTX PLL	0x0	R/W

REGISTER DETAILS

Table 24. Memory Map Register

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x600	DDC_SYNC_CTRL	7	DDC_TRIG_NCO_RESET_EN		DDC Trig NCO Reset Enable. DDC Trig NCO reset enable	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R
		4	DDC_SOFT_RESET		Digital Down Converter Soft Reset. Digital Down Converter Soft Reset 0: Normal Operation 1: DDC Held in Reset. Note: this bit can be used to synchronize all the NCO's inside the DDC blocks.	0x0	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		1	DDC_SYNC_NEXT		DDC Next Synchronization Mode. DDC Next Synchronization Mode 0: Continuous mode 1: Next Synchronization mode - only the next valid edge of SYSREF pin will be used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF pin will be ignored. Note: The SYSREF pin must an integer multiple of the NCO frequency in order for this function to operate correctly in continuous mode.	0x1	R/W
		0	DDC_SYNC_EN		DDC Synchronization Enable. DDC Synchronization Enable 0: Synchronization Disabled 1: Synchronization Enabled. If ddc_sync_next == 1, only the next valid edge of the SYSREF pin will be used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF pin will be ignored. Once the next SYSREF has been received, this bit has to be cleared for any subsequent use of next sysref. Note: the SYSREF input pin must be enabled in order to synchronize the DDC.	0x0	R/W
0x601	DDC_SYNC_STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	DDC_SYNC_EN_CLEAR		DDC Sync Enable Clear Status. DDC Sync Enable Clear Status	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x602	DDC_TRIG_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	DDC_TRIG_HOP_EN		DDC Trig Hop Enable. DDC Trig Hop Enable 0: Frequency hopping is independent of trig signal. 1: Trig signal us used for frequency hopping. When disabled, frequency hopping is done based on channel selection decoded from regmap or GPIO. For single channel the phase_inc, phase_offset written into active channel shadow register.	0x0	R/W
0x606	CHIP_DP_MODE	[7:6]	RESERVED		Reserved.	0x0	R
		5	CHIP_I_ONLY		Chip I Only. Chip Real (I) Only Selection 0: Both Real (I) and Complex (Q) Selected 1: Only Real (I) Selected. Complex (Q) is ignored.	0x0	R/W
		4	RESERVED		Reserved.	0x0	R
		[3:0]	CHIP_DP_APP_MODE		Chip Application Layer Operation Mode. Chip Application Layer Operating Mode 0x0 = Full Bandwidth Mode (High Performance Mode) 0x1 = One Digital Down Converter (DDC) Mode (DDC 0 Only) 0x2-0xF = Unused	0x0	R/W
0x607	CHIP_DEC_RATIO	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CHIP_DEC_RATIO		Chip Decimation Ratio. Chip Decimation Ratio 0x0 = Full Sample Rate (Decimate by 1) 0x1 = Decimate by 2 Ratio 0x2 = Decimate by 4 Ratio 0x3 = Decimate by 8 Ratio 0x4 = Decimate by 16 Ratio 0x5 = Decimate by 32 Ratio 0x6 = Decimate by 64 Ratio 0x7 = Decimate by 128 Ratio 0x8 = Reserved 0x9 = Decimate by 3 Ratio 0xA = Decimate by 6 Ratio 0xB = Decimate by 12 Ratio 0xC = Decimate by 24 Ratio 0xD = Decimate by 48 Ratio 0xE = Decimate by 96 Ratio 0xF = Reserved	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x608	CHIP_RES_0	[7:4]	CHIP_CONV_RES_0		Chip Conv Res 0. Chip Converter Resolution for Application Layer Mode 0 (High Performance Mode) 0x0: 16-bit resolution 0x1: 15-bit resolution 0x9: 7-bit resolution 0xA-F: Reserved	0x0	R/W
		[3:0]	CHIP_OUT_RES_0		Chip Out Res 0. Chip Output Resolution for Application Layer Mode 0 (High Performance Mode): 0x0: 16-bit resolution 0x1: 15-bit resolution 0x9: 7-bit resolution 0xA-F: Reserved	0x0	R/W
0x609	CHIP_RES_1	[7:4]	CHIP_CONV_RES_1		Chip Conv Res 1. Chip Converter Resolution for Application Layer Mode 1 0x0: 16-bit resolution 0x1: 15-bit resolution 0x9: 7-bit resolution 0xA-F: Reserved	0x0	R/W
		[3:0]	CHIP_OUT_RES_1		Chip Out Res 1. Chip Output Resolution for Application Layer Mode 1 0x0: 16-bit resolution 0x1: 15-bit resolution 0x9: 7-bit resolution 0xA-F: Reserved	0x0	R/W
0x620	CTRL_0_1_SEL	[7:4]	DFORMAT_CTRL_BIT_1_SEL		Control Bit 1 Mux Selection. Converter Control Bit 1 Selection 0x0: Tie low (1'b0) 0x1: Overrange Bit 0x2: Signal Monitor (SMON) Bit 0x3: Fast Detect (FD) Bit 0x4: DPD High/Low Resolution Bit 0x5: SYSREF 0x6-0x7: Reserved 0x8: NCO Channel Selection Bit 0 0x9: NCO Channel Selection Bit 1 0xA: Reserved(NCO Channel Selection Bit 2) 0xB: Reserved(NCO Channel Selection Bit 3)	0x0	R/W
		[3:0]	DFORMAT_CTRL_BIT_0_SEL		Control Bit 0 Mux Selection. Converter Control Bit 1 Selection 0x0: Tie low (1'b0) 0x1: Overrange Bit 0x2: Signal Monitor (SMON) Bit 0x3: Fast Detect (FD) Bit 0x4: DPD High/Low Resolution Bit 0x5: SYSREF 0x6-0x7: Reserved 0x8: NCO Channel Selection Bit 0 0x9: NCO Channel Selection Bit 1 0xA: Reserved(NCO Channel Selection Bit 2) 0xB: Reserved(NCO Channel Selection Bit 3)	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x621	CTRL_2_SEL	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DFORMAT_CTRL_BIT_2_SEL		Control Bit 2 Mux Selection. Converter Control Bit 1 Selection 0x0: Tie low (1'b0) 0x1: Overrange Bit 0x2: Signal Monitor (SMON) Bit 0x3: Fast Detect (FD) Bit 0x4: DPD High/Low Resolution Bit 0x5: SYSREF 0x6-0x7: Reserved 0x8: NCO Channel Selection Bit 0 0x9: NCO Channel Selection Bit 1 0xA: Reserved(NCO Channel Selection Bit 2) 0xB: Reserved(NCO Channel Selection Bit 3)	0x0	R/W
0x622	OUT_FORMAT_SEL	[7:3]	RESERVED		Reserved.	0x0	R
		2	DFORMAT_INV		Output Data Inversion Enable. Digital ADC Sample Invert (undocumented to customers) 0: ADC sample data is NOT inverted 1: ADC sample data is inverted	0x0	R/W
		[1:0]	DFORMAT_SEL		Output Data Format Selection. Digital ADC Data Format Select (DFS) (undocumented to customers) 00: 2's complement (default) 01: Offset Binary 10: Gray Code 11: Reserved	0x0	R/W
0x623	OVR_STATUS	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DFORMAT_OVR_STATUS		Output Overrange Status Indicator. Converter Over-range Indication Sticky Bits (active high). One bit for each virtual converter 0: No Over-Range has occurred 1: Over-Range has occurred This bit is set to "1" if converter is driven beyond the specified input range. It is "sticky," i.e., it remains set until explicitly cleared by writing a "1" to the corresponding dformat_ovr_clear[1:0] bit . The corresponding dformat_ovr_clear[1:0] bit would need to be cleared for further overflows to be reported [0] = Over-range Sticky bit for converter 0 [1] = Over-range Sticky bit for converter 1	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x624	OVR_CLR	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DFORMAT_OVR_CLR		Overrange Status Clear. Converter Over-range Clear bit(active high) Once an Over-range sticky bit has been set, it remains set until explicitly cleared by writing a "1" to the corresponding dformat_ovr_clear[1:0] bit. The dformat_ovr_clear[1:0] bit must be cleared for further overrange to be reported . [0] = Over-range Sticky bit clear for converter 0 [1] = Over-range Sticky bit clear for converter 1	0x0	R/W
0x625	OUT_CHAN_SEL	[7:2]	RESERVED		Reserved.	0x0	R
		1	DFORMAT_CHAN_ REPLICATE		Output Channel Replication Control. Converter Channel Replicate Control (undocumented to customers) 0: Unused converter outputs are zero. 1: Unused converter outputs are replicas of valid converter outputs. For example, while in High Performance Mode (chip_app_mode = 0x0), Converter 1 is unused, when this bit is set, converters 0 will be replicated on converter 1	0x0	R/W
		0	DFORMAT_CHAN_SWAP		Output Converter Channel Swap Control. Converter Channel Swap Control (undocumented to customers) 0: Normal Channel Ordering 1: Channel Swap Enabled. Converter 0 and 1 swapped	0x0	R/W
0x626	OUT_RES	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DFORMAT_RES		Data Output Resolution. Chip Output Resolution 0x0: 16-bit resolution 0x1: 15-bit resolution 0x9: 7-bit resolution 0xA-F: Reserved	0x0	R/W
0x628	DDC_DITHER	[7:2]	RESERVED		Reserved.	0x0	R
		1	DDC0_PHASE_DITHER_ EN		Phase Dither Enable. Phase Dither Enable 0: Enabled 1: Disabled	0x0	R/W
		0	DDC0_AMP_DITHER_EN		Amplitude Dither Enable. Amplitude Dither Enable 0: Enabled 1: Disabled	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x630	DDC_CTRL	[7:5]	RESERVED		Reserved.	0x0	R
		4	DDC0_C2R_EN		Complex to Real Enable. Complex to Real Enable 0: Complex (I and Q) Outputs Contain Valid Data 1: Real (I) Output Only. Complex to Real Enabled. Uses extra Fs/4 mixing to convert to Real.	0x0	R/W
		[3:2]	DDC0_IF_MODE		DDC Intermediate Frequency (IF) Mode. DDC Intermediate Frequency (IF) Mode 00: Variable IF Mode Mixers and NCO enabled.ddc_phase_inc[11:0] can be used to digitally tune the IF frequency. 01: 0 Hz IF Mode Mixers bypassed and NCO disabled. Should infer clock gating cells inside Mixer and NCO. Also, should gate combinatorial logic in Mixer multiplier to save dynamic logic. 10: Fs/4 Hz IF Mode Mixers and NCO enabled in special down-mixing by Fs/4 mode. This power saving mode is described in more detail in section 1.1.6.1.6. Fs/4 IF mode gain is different in this mode than variable IF mode Fs/4. 11: Test Mode Input samples are forced to +0.999… (+FS). NCO is enabled. This test mode allows the NCO's to directly drive the decimation filters and is useful when evaluating the performance of the NCOs and decimation filters.	0x0	R/W
		1	DDC0_GAIN		Gain Selection. Gain Selection 0: 0 dB Gain 1: 6 dB Gain (multiply by 2) Note: Gain can be used to compensate for the 6dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R
0x631	DDC_DEC_CTRL	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DDC0_DEC_SEL		DECIMATION RATIO SELECTION. DDC decimation selection bus. Encoded as: 0 -> DCM by 2 , //8 -> DCM by 6 1 -> DCM by 4 , //9 -> DCM by 12 2 -> DCM by 8 , //10-> DCM by 24 3 -> DCM by 16 , //11-> DCM by 48 4 -> DCM by 32 , //12-> DCM by 96 5 -> DCM by 64 , //13-> Reserved 6 -> DCM by 128, //14-> Reserved 7 -> Reserved, //15-> Reserved	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x632	DDC_NCO_CTRL	[7:4]	DDC0_NCO_CHAN_SEL_MODE		NCO Channel Selection Mode. NCO Channel Selection Mode NCO Channel Selection Mode. Mode decoding is TBD. 0000: Register Map control (Use ddc_nco_regmap_chan_sel) 0001: GPIO[0] Is used. Pin level control {3'b0, GPIO[0]} 0010: GPIO[1:0] are used . Pin level control {2'b0, GPIO[1:0]} 0011: GPIO[2 :0] are used. Pin level control {1'b0, GPIO[2:0]} 0100: GPIO[3 :0] are used. Pin level control { GPIO[3:0]} 0101-0111 : Reserved 1000: GPIO[0] Pin edge control- increment internal counter when rising edge of GPIO[0] Pin. 1001: GPIO[1] Pin edge control- increment internal counter when rising edge of GPIO[1] Pin. 1010: GPIO[2] Pin edge control- increment internal counter when rising edge of GPIO[2] Pin. 1011: GPIO[3] Pin edge control- increment internal counter when rising edge of GPIO[3] Pin. 1100: FHT expire based control - increment internal counter when FHT is expired. 1101 - 1111: Reserved Note: For edge control/fht based control, the internal counter wraps once ddc_nco_regmap_chan_sel value is reached.	0x0	R/W
		[3:0]	DDC0_NCO_REGMAP_CHAN_SEL		NCO Channel Select Register. NCO Channel Select Register map control 0000: Select NCO Channel 0 0001: Select NCO Channel 1 0010: Select NCO Channel 2 0011: Select NCO Channel 3 0100 : Select NCO Channel 4 1111 : Select NCO Channel 15	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x633	DDC_PROFILE_CTRL	7	DDC0_PROFILE_UPDATE_MODE		DDC Profile Update Mode. DDC Phase Update Mode 0 : Instantaneous/Continuous Update. Phase increment and phase offset values are updated immediately. 1: Phase increment and phase offset values are updated synchronously either with the chip transfer bit is set low to high.	0x0	R/W
		[6:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DDC0_PROFILE_UPDATE_INDEX		Profile Update Index. Indexes the NCO channel whose phase and offset gets updated. The update method is based on the 'ddc_phase_update_mode', which could be continuous or require 'chip_transfer'. 0000: Update NCO Channel 0 0001: Update NCO Channel 1 0010: Update NCO Channel 2 0011: Update NCO Channel 3 0100 : Update NCO Channel 4 1111 : Update NCO Channel 15	0x0	R/W
0x634	DDC_PHASE_INC0	[7:0]	DDC0_PHASE_INC0		Bits [7:0] of PHASE INCRMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x635	DDC_PHASE_INC1	[7:0]	DDC0_PHASE_INC1		Bits [15:8] of PHASE INCRMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x636	DDC_PHASE_INC2	[7:0]	DDC0_PHASE_INC2		Bits [23:16] of PHASE INCRMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x637	DDC_PHASE_INC3	[7:0]	DDC0_PHASE_INC3		Bits [31:24] of PHASE INCRMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x638	DDC_PHASE_INC4	[7:0]	DDC0_PHASE_INC4		Bits [39:32] of PHASE INCRMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x639	DDC_PHASE_INC5	[7:0]	DDC0_PHASE_INC5		Bits [47:40] of PHASE INCRMENT. NCO Phase Increment Value. Two's Complement Phase Increment Value for the NCO. Complex mixing frequency = (ddc_phase_inc * Fs) / 2^48.	0x0	R/W
0x63A	DDC_PHASE_OFFSET0	[7:0]	DDC0_PHASE_OFFSET0		Bits [7:0] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x63B	DDC_PHASE_OFFSET1	[7:0]	DDC0_PHASE_OFFSET1		Bits [15:8] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x63C	DDC_PHASE_OFFSET2	[7:0]	DDC0_PHASE_OFFSET2		Bits [23:16] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x63D	DDC_PHASE_OFFSET3	[7:0]	DDC0_PHASE_OFFSET3		Bits [31:24] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x63E	DDC_PHASE_OFFSET4	[7:0]	DDC0_PHASE_OFFSET4		Bits [39:32] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x63F	DDC_PHASE_OFFSET5	[7:0]	DDC0_PHASE_OFFSET5		Bits [47:40] of PHASE OFFSET. Two's Complement Phase Offset Value for the NCO.	0x0	R/W
0x640	DDC_PHASE_INC_ FRAC_A0	[7:0]	DDC0_PHASE_INC_ FRAC_A0		Bits [7:0] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator	0x0	R/W
0x641	DDC_PHASE_INC_ FRAC_A1	[7:0]	DDC0_PHASE_INC_ FRAC_A1		Bits [15:8] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator	0x0	R/W
0x642	DDC_PHASE_INC_ FRAC_A2	[7:0]	DDC0_PHASE_INC_ FRAC_A2		Bits [23:16] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator	0x0	R/W
0x643	DDC_PHASE_INC_ FRAC_A3	[7:0]	DDC0_PHASE_INC_ FRAC_A3		Bits [31:24] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator	0x0	R/W
0x644	DDC_PHASE_INC_ FRAC_A4	[7:0]	DDC0_PHASE_INC_ FRAC_A4		Bits [39:32] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator	0x0	R/W
0x645	DDC_PHASE_INC_ FRAC_A5	[7:0]	DDC0_PHASE_INC_ FRAC_A5		Bits [47:40] of PHASE INCREMENT NUMERATOR. Two's Complement Numerator correction term for modulus phase accumulator	0x0	R/W
0x646	DDC_PHASE_INC_ FRAC_B0	[7:0]	DDC0_PHASE_INC_ FRAC_B0		Bits [7:0] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator	0x0	R/W
0x647	DDC_PHASE_INC_ FRAC_B1	[7:0]	DDC0_PHASE_INC_ FRAC_B1		Bits [15:8] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator	0x0	R/W
0x648	DDC_PHASE_INC_ FRAC_B2	[7:0]	DDC0_PHASE_INC_ FRAC_B2		Bits [23:16] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator	0x0	R/W
0x649	DDC_PHASE_INC_ FRAC_B3	[7:0]	DDC0_PHASE_INC_ FRAC_B3		Bits [31:24] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator	0x0	R/W
0x64A	DDC_PHASE_INC_ FRAC_B4	[7:0]	DDC0_PHASE_INC_ FRAC_B4		Bits [39:32] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x64B	DDC_PHASE_INC_ FRAC_B5	[7:0]	DDC0_PHASE_INC_ FRAC_B5		Bits [47:40] of PHASE INCREMENT DENOMINATOR. Two's Complement denominator correction term for modulus phase accumulator	0x0	R/W
0x64C	DDC_TRANSFER_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	DDC0_CHIP_TRANSFER		DDC Chip Transfer. DDC chip Transfer 1: Used to synchronize the transfer of data from master to slave registers. 0: Do nothing. Note: This bit is used to update the DDC Phase Increment and Phase Offset registers when ddc_phase_update_mode = 1 and ddc_gpio_chip_transfer_mode = 0.	0x0	R/W
0x64D	DDC_TRANSFER_ STATUS	[7:1]	RESERVED		Reserved.	0x0	R
		0	DDC0_CHIP_TRANSFER_ STATUS		DDC Chip Transfer Status. DDC chip Transfer Status Bit 1: Transfer of data from master to slave registers is complete. 0: Indicates the data transfer is not requested or not completed.	0x0	R
0x650	MOD_NCO_PHASE_ ERROR_LOAD_REG0	[7:0]	MOD_NCO_PHASE_ ERROR_LOAD_VALUE[7:0]		MOD NCO Phase Error Value. MOD NCO Phase Error Value	0x0	R/W
0x651	MOD_NCO_PHASE_ ERROR_LOAD_REG1	[7:0]	MOD_NCO_PHASE_ ERROR_LOAD_VALUE[15:8]		MOD NCO Phase Error Value. MOD NCO Phase Error Value	0x0	R/W
0x652	MOD_NCO_PHASE_ ERROR_LOAD_REG2	[7:0]	MOD_NCO_PHASE_ ERROR_LOAD_ VALUE[23:16]		MOD NCO Phase Error Value. MOD NCO Phase Error Value	0x0	R/W
0x653	MOD_NCO_PHASE_ ERROR_LOAD_REG3	[7:0]	MOD_NCO_PHASE_ ERROR_LOAD_ VALUE[31:24]		MOD NCO Phase Error Value. MOD NCO Phase Error Value	0x0	R/W
0x654	MOD_NCO_PHASE_ ERROR_LOAD_REG4	[7:0]	MOD_NCO_PHASE_ ERROR_LOAD_ VALUE[39:32]		MOD NCO Phase Error Value. MOD NCO Phase Error Value	0x0	R/W
0x655	MOD_NCO_PHASE_ ERROR_LOAD_REG5	[7:0]	MOD_NCO_PHASE_ ERROR_LOAD_ VALUE[47:40]		MOD NCO Phase Error Value. MOD NCO Phase Error Value	0x0	R/W
0x656	MOD_NCO_PHASE_ ERROR_LOAD_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	MOD_NCO_PHASE_ ERROR_LOAD_ENABLE		MOD NCO Phase Error Load Enable. MOD NCO Phase Error Load Enable	0x0	R/W
0x657	MOD_NCO_PHASE_ ERROR_LOAD_STATUS	[7:3]	RESERVED		Reserved.	0x0	R
		2	MOD_NCO_PHASE_ ERROR_LOAD_STATUS		MOD NCO Phase Error Load Status. Profile Select Timer Load Status	0x0	R
		[1:0]	RESERVED		Reserved.	0x0	R
0x65F	DDC_PSW_0	[7:0]	DDC0_PSW0		DDC Profile Select Word. DDC Profile Select Word (PSW): Bits 0-7 The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x660	DDC_PSW_1	[7:0]	DDC0_PSW1		DDC Profile Select Word. DDC Profile Select Word (PSW) : Bits 8-15 The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x661	DDC_PSW_2	[7:0]	DDC0_PSW2		DDC Profile Select Word. DDC Profile Select Word (PSW) : Bits 16-23 The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x662	DDC_PSW_3	[7:0]	DDC0_PSW3		DDC Profile Select Word. DDC Profile Select Word (PSW) : Bits 24-31 The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x663	DDC_PSW_4	[7:0]	DDC0_PSW4		DDC Profile Select Word. DDC Profile Select Word (PSW) : Bits 32-39 The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x664	DDC_PSW_5	[7:0]	DDC0_PSW5		DDC Profile Select Word. DDC Profile Select Word (PSW) : Bits 40-47 The PSW specifies the rollover point (in encode samples) for the Profile Select Timer (PST). Whenever the Profile Select Timer rolls over to zero, channel selection counter increments when channel selection is through Profile Select Timer.	0x0	R/W
0x665	DDC_ACTIVE_PHASE_INC0	[7:0]	DDC0_ACTIVE_PHASE_INC0		Bits [7:0] of ACTIVE PHASE INCRMENT. NCO Active Phase Increment Value.	0x0	R
0x666	DDC_ACTIVE_PHASE_INC1	[7:0]	DDC0_ACTIVE_PHASE_INC1		Bits [15:8] of ACTIVE PHASE INCRMENT. NCO Active Phase Increment Value.	0x0	R
0x667	DDC_ACTIVE_PHASE_INC2	[7:0]	DDC0_ACTIVE_PHASE_INC2		Bits [23:16] of ACTIVE PHASE INCRMENT. NCO Active Phase Increment Value.	0x0	R
0x668	DDC_ACTIVE_PHASE_INC3	[7:0]	DDC0_ACTIVE_PHASE_INC3		Bits [31:24] of ACTIVE PHASE INCRMENT. NCO Active Phase Increment Value.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x669	DDC_ACTIVE_PHASE_INC4	[7:0]	DDC0_ACTIVE_PHASE_INC4		Bits [39:32] of ACTIVE PHASE INCRMENT. NCO Active Phase Increment Value.	0x0	R
0x66A	DDC_ACTIVE_PHASE_INC5	[7:0]	DDC0_ACTIVE_PHASE_INC5		Bits [47:40] of ACTIVE PHASE INCRMENT. NCO Active Phase Increment Value.	0x0	R
0x66B	DDC_ACTIVE_PHASE_OFFSET0	[7:0]	DDC0_ACTIVE_PHASE_OFFSET0		Bits [7:0] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x66C	DDC_ACTIVE_PHASE_OFFSET1	[7:0]	DDC0_ACTIVE_PHASE_OFFSET1		Bits [15:8] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x66D	DDC_ACTIVE_PHASE_OFFSET2	[7:0]	DDC0_ACTIVE_PHASE_OFFSET2		Bits [23:16] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x66E	DDC_ACTIVE_PHASE_OFFSET3	[7:0]	DDC0_ACTIVE_PHASE_OFFSET3		Bits [31:24] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x66F	DDC_ACTIVE_PHASE_OFFSET4	[7:0]	DDC0_ACTIVE_PHASE_OFFSET4		Bits [39:32] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x670	DDC_ACTIVE_PHASE_OFFSET5	[7:0]	DDC0_ACTIVE_PHASE_OFFSET5		Bits [47:40] of ACTIVE PHASE OFFSET. NCO Active Phase Increment Value.	0x0	R
0x671	TIMESTAMP_READ_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	TIMESTAMP_READ_ENABLE		Timestamp Read Enable. Time Stamp Read enable. Rise edge on Time stamp read enable is detected and then timestamp counter data is latched. This stored time stamp data is used for timestamp status read.	0x0	R/W
0x672	TIMESTAMP_COUNTER_REG0	[7:0]	TIMESTAMP[7:0]		TimeStamp Data. Time Stamp counter value	0x0	R
0x673	TIMESTAMP_COUNTER_REG1	[7:0]	TIMESTAMP[15:8]		TimeStamp Data. Time Stamp counter value	0x0	R
0x674	TIMESTAMP_COUNTER_REG2	[7:0]	TIMESTAMP[23:16]		TimeStamp Data. Time Stamp counter value	0x0	R
0x675	TIMESTAMP_COUNTER_REG3	[7:0]	TIMESTAMP[31:24]		TimeStamp Data. Time Stamp counter value	0x0	R
0x676	TIMESTAMP_COUNTER_REG4	[7:0]	TIMESTAMP[39:32]		TimeStamp Data. Time Stamp counter value	0x0	R
0x677	TIMESTAMP_COUNTER_REG5	[7:0]	TIMESTAMP[47:40]		TimeStamp Data. Time Stamp counter value	0x0	R
0x678	TIMESTAMP_COUNTER_REG6	[7:0]	TIMESTAMP[55:48]		TimeStamp Data. Time Stamp counter value	0x0	R
0x679	TIMESTAMP_COUNTER_REG7	[7:0]	TIMESTAMP[63:56]		TimeStamp Data. Time Stamp counter value	0x0	R
0x680	FSX_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	FSX_MODE		FSX Packing Mode Enable. FSX Packing Mode Enable 0 - FSX mode is disabled 1 - FSX1 mode is enabled	0x0	R/W
0x690	SYSREF_DELAY	[7:0]	SYSREF_PROGDELAY		Programmable Delay on Sysref Path to DDC NCO. 8 bit delay in terms of sampling clock	0x0	R/W
0x691	TRIG_DELAY	[7:0]	TRIG_PROGDELAY		Programmable Delay on TRIG Path to DDC NCO. 8 bit delay in terms of sampling clock	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x692	TIMESTAMP_DELAY	[7:0]	TIMESTAMP_PROGDELAY		Programmable Delay on Timestamp Path in DFORMAT. 8 bit delay in terms of sampling clock	0x0	R/W
0x693	SYSREF_RESYNC	[7:1]	RESERVED		Reserved.	0x0	R
		0	SYSREF_RESYNC		SYSREF Resynchronization Mode Enable. Sysref Resynchronization Mode Enable 0 - Sysref timestamp mode enabled 1 - Sysref re-synchronization mode enabled	0x0	R/W

REGISTER DETAILS: (AD9213_CUST_REG)

Table 25. Memory Map Register

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1501	pll_pwdn	[7:3]	RESERVED		Reserved.	0x0	R
		2	impala_pll_pd		power down all blocks inside impala pll	0x1	R/W
		[1:0]	RESERVED		Reserved.	0x2	R/W
0x1502	pll_reset	[7:3]	RESERVED		Reserved.	0x0	R
		2	d_impala_porb_1p8		Goes high when 1V supply is above 0.8V. c	0x0	R
		1	d_impala_porb_1p0		Goes high when 1.8V supply is above 1.6V and 1V supply is above 0.8V. c	0x0	R
		0	d_cal_reset		Resets vco calibration. (1 = reset) c	0x1	R/W
0x1503	pll_divider	[7:2]	d_divide_control		Programmable divide by N value from 2 to 50. c	0x8	R/W
		[1:0]	d_refin_div		Programmable predivider value. c	0x0	R/W
				0	/1.		
				1	/2.		
				10	/3.		
				11	/4.		
0x1504	pll_divider2	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	d_vco_div_control		Vco output divider: 00: /1; 01: /2; 10: /3; 11: /4. c	0x0	R/W
0x1506	pll_lock	[7:3]	RESERVED		Reserved.	0x0	R
		2	impala_pll_lock		Impala PLL lock detect	0x0	R
		[1:0]	d_pll_lock_control		Select PLL lock mode. c	0x3	R/W
				0	No locks enabled.		
				1	Fast lock enabled.		
				10	Slow lock enabled.		
				11	Lock signal is AND (fast lock, slow lock).		
0x1507	reset_ctrl	[7:5]	RESERVED		Reserved.	0x0	R
		4	reset_jtx		Reset JTX block	0x0	R/W
		3	RESERVED		Reserved.	0x0	R/W
		2	reset_dpath		Reset data path.	0x0	R/W
		1	reset_dig_ana		Reset digital blocks in analog section. Reset digital blocks in analog section	0x1	R/W
		0	reset_ana		Reset analog section	0x1	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1508	sysref_ctrl	[7:2]	RESERVED		Reserved.	0x0	R
		1	sysref_transition_sel		SYSREF Transition Selection - 0: SYSREF is valid on LOW to HIGH transitions using selected CLK edge. 1: SYSREF is valid on HIGH to LOW transitions using selected CLK edge.	0x0	R/W
		0	sysref_edge_sel		SYSREF Capture Edge Selection - 0: Captured on Rising Edge of CLK input 1: Captured on Falling Edge of CLK input	0x0	R/W
0x1509	sysref_status	[7:4]	sysref_hold_status		Gives status of hold capture window	0x0	R
		[3:0]	sysref_setup_status		Gives status of setup capture window	0x0	R
0x150A	lvds_sel	[7:2]	RESERVED		Reserved.	0x0	R
		1	trig_rx_lvds_sel		Switch between LVDS and differential CMOS input modes for the trig - 0: Differential CMOS selected 1: LVDS selected	0x0	R/W
		0	sysref_rx_lvds_sel		Switch between LVDS and differential CMOS input modes for the sysref - 0: Differential CMOS selected 1: LVDS selected	0x0	R/W
0x150B	spi_pll_sel	[7:1]	RESERVED		Reserved.	0x0	R
		0	spi_pll_sel			0x0	R/W
0x150C	spi_en_dcs	[7:1]	RESERVED		Reserved.	0x0	R
		0	spi_en_dcs			0x0	R/W
0x150D	spi_en_fdly	[7:2]	RESERVED		Reserved.	0x0	R
		1	spi_en_sfdly			0x0	R/W
		0	spi_en_fdly			0x0	R/W
0x150E	spi_trm_fine_dly	[7:0]	spi_trm_fine_dly			0x0	R/W
0x150F	spi_trm_super_fine_dly	[7:0]	spi_trm_super_fine_dly			0x0	R/W
0x1510	spi_sfdc_bypass	[7:1]	RESERVED		Reserved.	0x0	R
		0	spi_sfdc_bypass			0x0	R/W
0x1511	bkend_top_gain_adj	[7:1]	RESERVED		Reserved.	0x0	R
		0	gain_2x		Setting this to 1 doubles the data at the output	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1512	supply_mon1	[7:6]	RESERVED		Reserved.	0x0	R
		5	supmon_vttphy_ser_0p9		+1V supply monitor for SERDES	0x0	R
		4	supmon_vddsynth_lcpll_0p9		+1V supply monitor for JESD synth	0x0	R
		3	supmon_vddd_lcpll_0p9		+1V digital supply monitor for JESD PLL	0x0	R
		2	supmon_vdda_refadc_1p0		+1V analog supply monitor for refADC	0x0	R
		1	supmon_vdda_clk_1p0		+1V analog supply monitor for clock	0x0	R
		0	supmon_vdda_1p0		+1V analog supply monitor	0x0	R
0x1513	supply_mon2	[7:5]	RESERVED		Reserved.	0x0	R
		4	supmon_vdda_tmu_1p8		+2V analog supply monitor for TMU	0x0	R
		3	supmon_vddldo_lcpll_1p8		+2V supply monitor for JESD LDO	0x0	R
		2	supmon_vddd_spi_1p8		+2V digital supply monitor for SPI pads	0x0	R
		1	supmon_vdda_ref_2p0		+2V analog supply monitor for reference	0x0	R
		0	supmon_vdda_buf_2p0		+2V analog supply monitor for buffer	0x0	R
0x1514	supply_mon3	[7:2]	RESERVED		Reserved.	0x0	R
		1	supmon_veea_neg1p0		−1V analog supply monitor	0x0	R
		0	supmon_veea_buf_neg1p0		−1V analog supply monitor for buffer	0x0	R
0x1515	pdown_ctrl	[7:3]	pdb_ref_nohclk		power down for reference	0x0	R/W
		2	spi_pdb_clkbuf		power down for clk buffer	0x0	R/W
		1	stdby_chip		standby chip	0x0	R/W
		0	pd_chip		power down chip	0x1	R/W
0x1516	spi_en_fdly_sys	[7:2]	RESERVED		Reserved.	0x0	R
		1	spi_en_sfdly_sys			0x0	R/W
		0	spi_en_fdly_sys			0x0	R/W
0x1517	spi_trm_fine_dly_sys	[7:0]	spi_trm_fine_dly_sys			0x0	R/W
0x1518	spi_trm_super_fine_dly_sys	[7:0]	spi_trm_super_fine_dly_sys			0x0	R/W
0x1519	spi_sfdc_bypass_sys	[7:1]	RESERVED		Reserved.	0x0	R
		0	spi_sfdc_bypass_sys			0x0	R/W
0x151A	en_vcm_mode	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	en_vcm_mode		VCMin Enable Mode Control	0x1	R/W
				00	Internal and External VCM control buffers disabled.		
				01	Startup: Internal VCM control buffer enabled.		
				10	External VCM control buffer enabled.		
				11	Internal and External VCM control buffers enabled - aux mode.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x151B	spi_nvg1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:1]	spi_en_sum_nvg_1p0			0x0	R/W
		0	spi_en_nvg_1p0			0x0	R/W
0x151C	spi_nvg2	[7:6]	RESERVED		Reserved.	0x0	R
		[5:0]	spi_nvg_1p0			0x0	R/W
0x151D	Clock_detect_ctrl	[7:1]	RESERVED		Reserved.	0x1	R
		0	clock_detect		Status of clock detect locked	0x0	R
0x151E	mcs_ctrl	[7:4]	RESERVED		Reserved.	0x0	R
		[3:2]	mcs_trig_freq_hop_mode	00 01 10 11	Trig used to frequency hop or Trig used as enable while sysref_out/div8 counter is used to frequency hop.	0x0	R/W
		1	mcs_dtll_lock_detect_cust		Read only status from MCS into customer regmap. Tells the customer that a lock has been achieved. Used in continuous SYSREF modes	0x0	R
		0	mcs_div8_sreset		Synchronous reset for sysref out divider: Active high	0x0	R/W
0x151F	mcs_div8_divide_ratio	[7:0]	mcs_div8_divide_ratio		Divide ratio for debug div8 divider in MCS. Can be used to generate a periodic frequency hop when trig is used as enable.	0x0	R/W
0x1520	mcs_div8_phase_offset	[7:0]	mcs_div8_phase_offset		Phase offset for debug div8 divider in MCS. Can be used to generate a periodic frequency hop when Trig is used as enable.	0x0	R/W
0x1521	mcs_sysref_ignore_count	[7:0]	mcs_sysref_ignore_count		Number of SYSREF pulses to ignore at startup	0x0	R/W

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

Several of the AD9213 supply domains can be combined and powered by the supply configuration shown in Figure 38 if desired. This is an example configuration for minimizing power supply components and power domains. This approach may slightly increase the risk of switching regulator artifacts being injected into the power supply domains of the ADC. Initial evaluations using this configuration suggest the noise impact is minimal and will typically be outweighed by its simplicity and use of fewer power supply components. Use of linear regulators and isolating specific supply pins could result in less noise. This configuration is for AD9213 operation with the clock multiplier PLL bypassed and powered down.

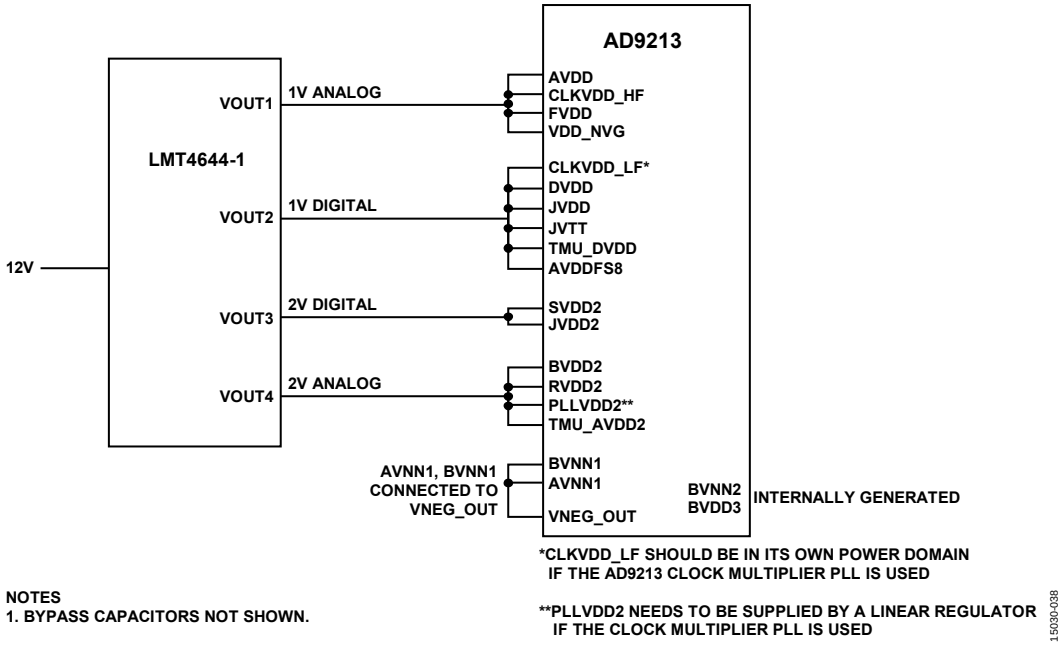

Figure 38.

OUTLINE DIMENSIONS

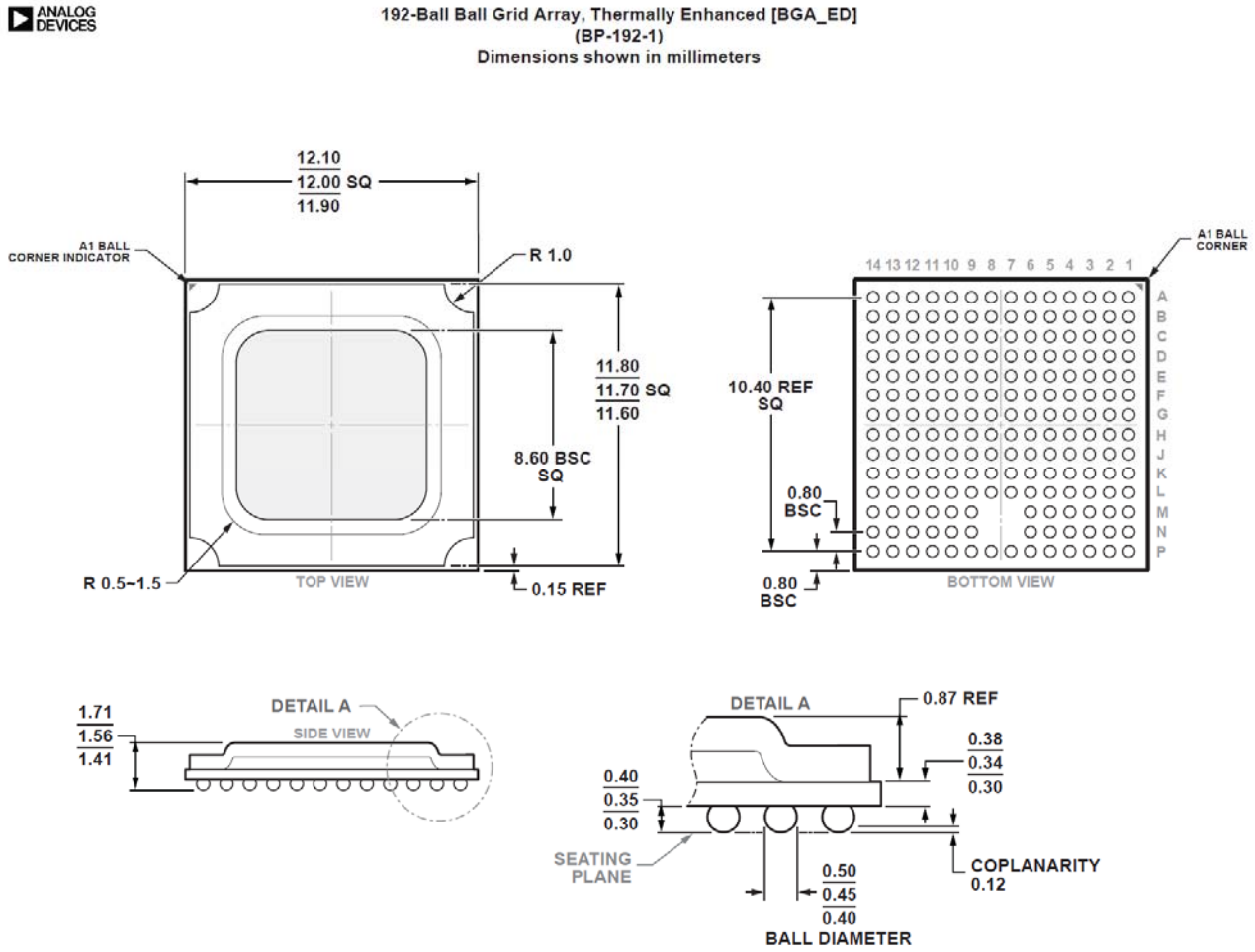

Figure 39. 192-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-192-1)
Dimensions shown in millimeters

PR15030-0-6/18(PrF)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD9213-6GEBZ AD9213-10GEBZ