

# TLE 8444SL

Quad Half-Bridge Driver IC

Automotive Power



Never stop thinking

## Table of Contents

<b>1</b>	<b>Overview</b> .....	<b>3</b>
<b>2</b>	<b>Block Diagram</b> .....	<b>4</b>
<b>3</b>	<b>Pin Configuration</b> .....	<b>6</b>
3.1	Pin Assignment .....	6
3.2	Pin Definitions and Functions .....	6
<b>4</b>	<b>General Product Characteristics</b> .....	<b>8</b>
4.1	Absolute Maximum Ratings .....	8
4.2	Functional Range .....	9
4.3	Thermal Resistance .....	9
4.4	Electrical Characteristics .....	10
<b>5</b>	<b>Block Description</b> .....	<b>12</b>
5.1	Power Supply .....	12
5.1.1	General .....	12
5.1.2	Sleep Mode .....	12
5.1.3	Reverse Polarity .....	13
5.2	Input / Output Stages .....	14
5.3	Monitoring Functions .....	16
5.3.1	Diagnostics .....	16
5.3.2	Power Supply Monitoring .....	17
5.3.3	Temperature Monitoring .....	18
5.4	Power-Outputs 1-4 (Half Bridge Outputs) .....	19
5.4.1	Protection and Diagnosis .....	19
5.4.1.1	Short Circuit of Output to Ground or Vs .....	19
5.4.1.2	Open Load .....	23
5.5	Output Switching Capability .....	24
5.5.1	Application Note for Bipolar Stepper Motor Control .....	28
<b>6</b>	<b>Package Outlines</b> .....	<b>30</b>
<b>7</b>	<b>Revision History</b> .....	<b>31</b>



## 1 Overview

### Features

- 4 Half-Bridge Power Outputs ( $1.3\Omega R_{DS(ON)MAX}$  @  $T_j=150^\circ\text{C}$ )
- Minimum Overcurrent Shutdown at 0.9A
- Simple parallel interface control of Half-Bridge Outputs
- Inverted and Non-inverted Inputs to minimize number of microcontroller connections
- Very low current consumption in sleep mode (max. 5 $\mu\text{A}$ )
- Error Flag Diagnosis
- Open Load Diagnosis in ON-state for all outputs
- Outputs protected against overcurrent
- Over temperature protection with hysteresis
- Over and Under voltage lockout
- 3.3V / 5V compatible inputs with hysteresis
- No crossover current
- Internal freewheeling diodes
- Thermally enhanced package (fused leads)
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-24

### Description

The TLE 8444SL is a protected **Quad-Half-Bridge-IC** targeted towards automotive and industrial motion control applications. It is a monolithic die based on Infineon's smart mixed technology SPT which combines bipolar and CMOS control circuitry with DMOS power devices.

DC-Motors can be driven in forward (cw), reverse (ccw), brake and high impedance modes where as Stepper-Motors can be driven in No-Current, negative / positive output current modes. These various modes can easily be achieved via standard parallel interface of the device to a microcontroller.

The PG-SSOP-24 package is advantageous as it saves PCB-board space and costs. The integrated short circuit and over-temperature protection as well as it's built-in diagnosis features such as over- and under voltage-lockout and open load detection improves system reliability and performance.

### Target Applications:

- Unipolar or Bipolar Loads
- Stepper Motors (e.g. Idle Speed Control)
- DC brush Motors

Type	Package	Marking
TLE 8444SL	PG-SSOP-24	TLE8444SL

## 2 Block Diagram

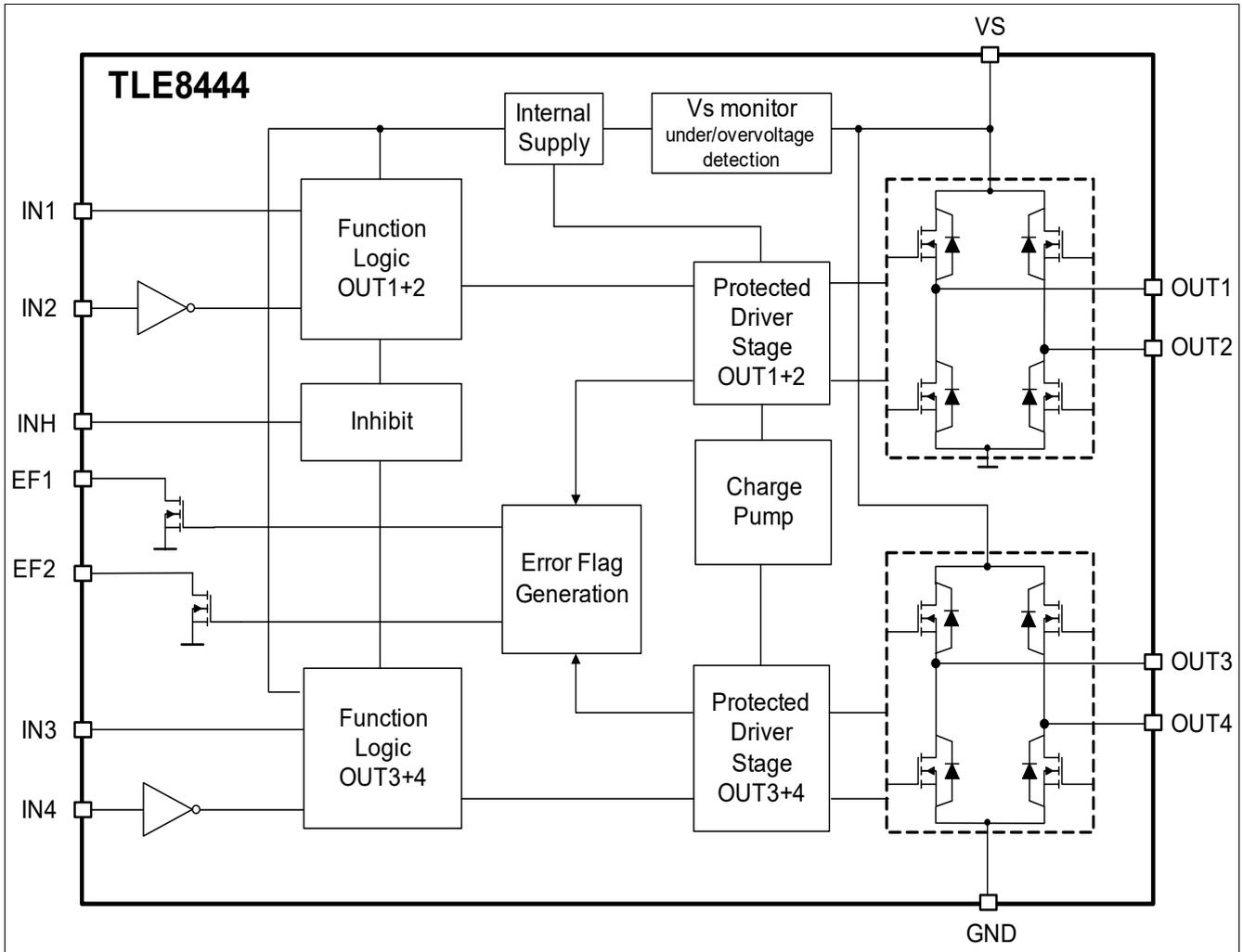


Figure 1 Block Diagram

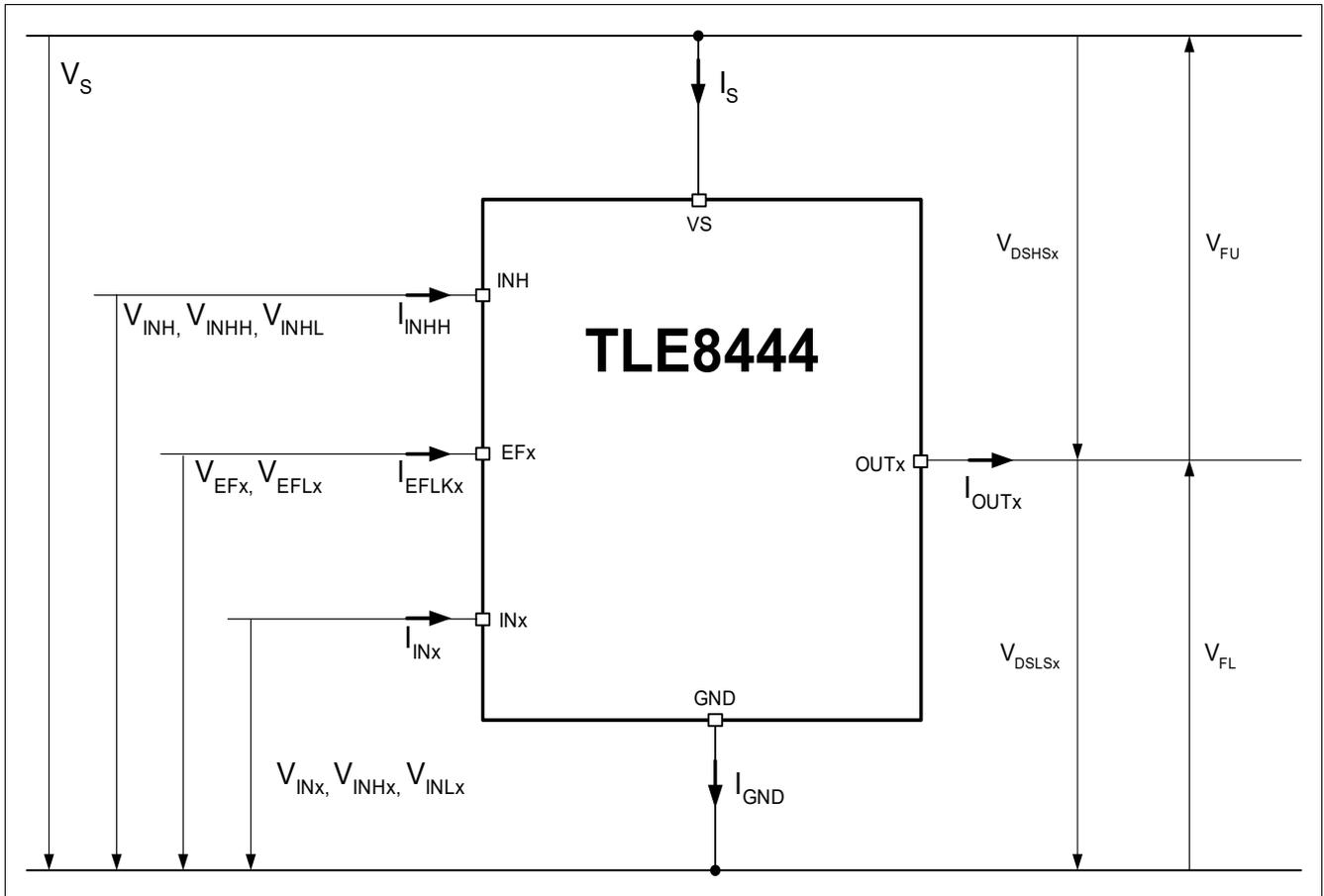


Figure 2 Terms

### 3 Pin Configuration

#### 3.1 Pin Assignment

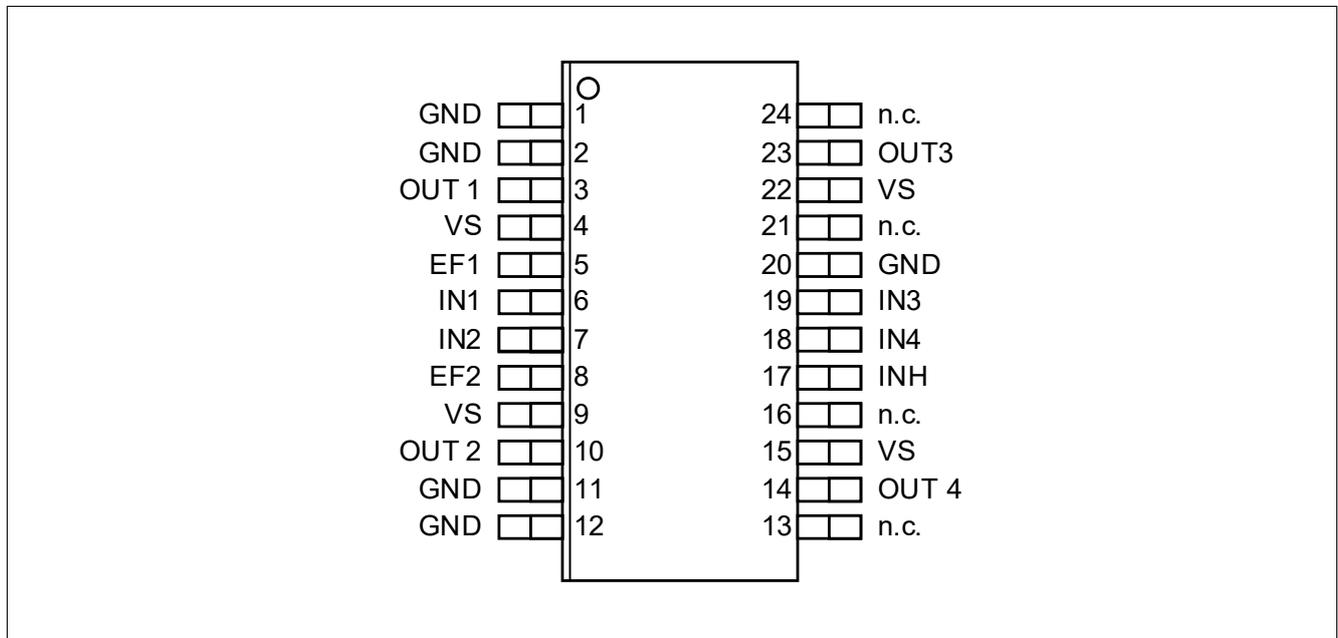


Figure 3 Pin Configuration

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1, 2, 11, 12, 20	GND	<b>Ground</b> ; Signal ground; All GND pins must be externally connected together to the common GND potential
3	OUT1	<b>Power Output of Half-bridge 1</b> Short circuit protected; with integrated free-wheeling diodes
4, 9, 15, 22	$V_S$	<b>Power Supply Voltage</b> ; All $V_S$ pins must be externally connected together to the Battery Voltage with Reverse protection Diode, buffer capacitance and Filter against EMC. See Application Diagram, <a href="#">Figure 18</a> and <a href="#">Figure 19</a> for more information
5	EF1	<b>Error Flag 1 (Diagnosis Output)</b> Open drain by default; Low = error
6	IN1	<b>Input Channel of Half-bridge 1</b> Controls OUT1, Non-inverting Input with internal Pull Down
7	IN2	<b>Input Channel of Half-bridge 2</b> Controls OUT2, Inverting Input with internal Pull Up
8	EF2	<b>Error Flag 2 (Diagnosis Output)</b> Open drain by default; Low = error
10	OUT2	<b>Power Output of Half-bridge 2</b> Short circuit protected; with integrated free-wheeling diodes
13, 16, 21, 24	N.C.	<b>Not Connected</b>

Pin Configuration

Pin	Symbol	Function
14	OUT4	<b>Power Output of Half-bridge 4</b> Short circuit protected; with integrated free-wheeling diodes
17	INH	<b>Inhibit Input</b> Low = Device in sleep mode
18	IN4	<b>Input Channel of Half-bridge 4</b> Controls OUT4, Inverting Input with internal Pull Up
19	IN3	<b>Input Channel of Half-bridge 3</b> Controls OUT3, Non-inverting Input with internal Pull Down
23	OUT3	<b>Power Output of Half-bridge 3</b> Short-circuit protected; with integrated free-wheeling diodes

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>Voltages</b>						
4.1.1	Supply voltage	$V_S$	-0.3	40	V	–
4.1.2	Logic input voltages (IN1; IN2; IN3; IN4; INH)	$V_{IN(1-4)}$ $V_{INH}$	-0.3	5.5	V	$0\text{ V} < V_S < 40\text{ V}$
4.1.3	Logic output voltage (EF <sub>1</sub> ; EF <sub>2</sub> )	$V_{EF(1+2)}$	-0.3	5.5	V	$0\text{ V} < V_S < 40\text{ V}$
<b>Currents</b>						
4.1.4	Output current (diode)	$I_{OUT(1-4)}$	-1	1	A	–
4.1.5	Output current (EF <sub>1</sub> ; EF <sub>2</sub> )	$I_{EF(1-2)}$	-2	5	mA	–
<b>Temperatures</b>						
4.1.6	Junction temperature	$T_j$	-40	150	°C	–
4.1.7	Storage temperature	$T_{stg}$	-50	150	°C	–
<b>ESD Susceptibility</b>						
4.1.8	ESD capability of OUT and $V_S$ pin vers. GND	$V_{ESD}$	-2	2	kV	<sup>2)</sup>
4.1.9	ESD capability of logic pins vers. GND	$V_{ESD}$	-2	2	kV	<sup>2)</sup>

1) Not subject to production test, specified by design.

2) Human Body Model according to ANSI EOS/ESD S5.1 standard (eqv. to MIL STD 883D and JEDEC JESD22-A114)

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Normal Operation	$V_{S(nor)}$	8	18	V	–
4.2.2	Extended Supply Voltage Range for Operation	$V_{S(ext)}$	$V_{UV OFF}$	$V_{OV OFF}$	V	Limit values, deviations possible; After $V_S$ rising above $V_{UV ON}$
4.2.3	Supply voltage increasing	$V_S$	-0.3	$V_{UV ON}$	V	Outputs are open
4.2.4	Supply voltage decreasing	$V_S$	-0.3	$V_{UV OFF}$	V	Outputs are open
4.2.5	Logic input voltages (IN1; IN2; IN3; IN4; INH)	$V_{IN(1-4)}$ $V_{INH}$	-0.3	5.5	V	–
4.2.6	Junction temperature	$T_j$	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering Point <sup>1)</sup>	$R_{thJSP}$	–	–	26	K/W	pin 1, 2, 11, 12 <sup>2)</sup>
4.3.2	Junction to Ambient <sup>1)</sup>	$R_{thJA}$	–	60	–	K/W	<sup>3)</sup>

1) Not subject to production test, specified by design

2) Specified RthJS value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). Ta=25°C, LS1+HS2+LS3+HS4 are dissipating 1W (0.25W each).

3) Specified RthJA value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Ta=25°C, LS1+HS2+LS3+HS4 are dissipating 1W (0.25W each).

## 4.4 Electrical Characteristics

### 4.4.3

#### Electrical Characteristics

$V_S = 8\text{ V to }18\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ , INH = HIGH;  $I_{OUT1-4} = 0\text{ A}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Current Consumption, INH = GND</b>							
4.4.1	Quiescent current	$I_S$	–	1	5	$\mu\text{A}$	$V_S = 13.5\text{ V}$ ; $T_j < 85\text{ °C}$
<b>Current Consumption, INH = HIGH</b>							
4.4.2	Supply current	$I_S$	–	5	10	$\text{mA}$	IN1+3=L, IN2+4=H
<b>Over- and Under Voltage Lockout</b>							
4.4.3	UV Switch ON voltage	$V_{UV\text{ ON}}$	4.2	–	5	$\text{V}$	$V_S$ increasing, see <a href="#">Figure 6</a>
4.4.4	UV Switch OFF voltage	$V_{UV\text{ OFF}}$	4	–	4.8	$\text{V}$	$V_S$ decreasing, see <a href="#">Figure 6</a>
4.4.5	UV ON/OFF hysteresis	$V_{UV\text{ HY}}$	0.05	0.26	0.7	$\text{V}$	$V_{UV\text{ ON}} - V_{UV\text{ OFF}}$ , see <a href="#">Figure 7</a>
4.4.6	OV Switch OFF voltage	$V_{OV\text{ OFF}}$	21	–	25	$\text{V}$	$V_S$ increasing, see <a href="#">Figure 6</a>
4.4.7	OV Switch ON voltage	$V_{OV\text{ ON}}$	20	–	24	$\text{V}$	$V_S$ decreasing, see <a href="#">Figure 6</a>
4.4.8	OV ON/OFF hysteresis	$V_{OV\text{ HY}}$	–	1	–	$\text{V}$	$V_{OV\text{ OFF}} - V_{OV\text{ ON}}$ , see <a href="#">Figure 7</a>
<b>Static Drain-source ON-Resistance</b>							
4.4.9	High- and low-side switch	$R_{\text{DS(ON)}}$	–	0.6	0.8	$\Omega$	$I_{\text{OUT}} = \pm 0.8\text{ A}$ ; $T_j = 25\text{ °C}$
			–	1.0	1.3	$\Omega$	$I_{\text{OUT}} = \pm 0.8\text{ A}$ ; $T_j = 150\text{ °C}$
<b>Output Protection and Diagnosis</b>							
4.4.10	Short Circuit Current <sup>1)</sup>	$I_{\text{SC(1-4)}}$	1.8	2.4	3.2	$\text{A}$	HS+LS each Channel, see <a href="#">Figure 13</a>
4.4.11	Overcurrent Shutdown Threshold	$I_{\text{SD(1-4)}}$	0.9	1.2	1.6	$\text{A}$	
4.4.12	Shutdown Delay Time	$t_{\text{dSD(1-4)}}$	10	25	50	$\mu\text{s}$	
4.4.13	Open Load Detection Current	$I_{\text{OLD(1-4)}}$	6	12	20	$\text{mA}$	each LS Channel, see <a href="#">Figure 15</a>
4.4.14	Open Load Delay Time	$t_{\text{dOLD(1-4)}}$	200	350	600	$\mu\text{s}$	
<b>Output Switching Times</b>							
4.4.15	high-side ON delay-time	$t_{\text{dONH}}$	7	10	14	$\mu\text{s}$	$V_S = 13.5\text{ V}$ , resistive Load = $100\Omega$ , see <a href="#">Figure 16</a> and <a href="#">Figure 17</a>
4.4.16	high-side switch ON time	$t_{\text{ONH}}$	2	6	9	$\mu\text{s}$	
4.4.17	high-side OFF delay-time	$t_{\text{dOFFH}}$	1	2	4	$\mu\text{s}$	
4.4.18	high-side switch OFF time	$t_{\text{OFFH}}$	0.2	1	2	$\mu\text{s}$	
4.4.19	low-side ON delay-time	$t_{\text{dONL}}$	2	5	8	$\mu\text{s}$	
4.4.20	low-side switch ON time	$t_{\text{ONL}}$	0.5	1	3	$\mu\text{s}$	
4.4.21	low-side OFF delay-time	$t_{\text{dOFFL}}$	1	2	5	$\mu\text{s}$	
4.4.22	low-side switch OFF time	$t_{\text{OFFL}}$	0.5	1	2	$\mu\text{s}$	
4.4.23	dead-time	$t_{\text{DB}}$	0.1	2	–	$\mu\text{s}$	
<b>Outputs OUT(1-4), Freewheeling Diodes</b>							
4.4.24	Forward voltage; upper	$V_{\text{FU}}$	–	1	1.5	$\text{V}$	$I_F = 0.4\text{ A}$ , INH = LOW

**General Product Characteristics**
**Electrical Characteristics (cont'd)**

$V_S = 8\text{ V to }18\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$ , INH = HIGH;  $I_{OUT1-4} = 0\text{ A}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.25	Forward voltage; lower	$V_{FL}$	–	0.9	1.4	V	$I_F = 0.4\text{ A}$ , INH = LOW

**Input Interface, Logic Inputs IN1, IN2, IN3, IN4**

4.4.26	High-input voltage IN1, IN3	$V_{INH(1+3)}$	2	–	–	V	–
4.4.27	Low-input voltage IN1, IN3	$V_{INL(1+3)}$	–	–	0.8	V	–
4.4.28	High-input voltage IN2, IN4	$V_{INH(2+4)}$	2	–	–	V	–
4.4.29	Low-input voltage IN2, IN4	$V_{INL(2+4)}$	–	–	0.8	V	–
4.4.30	Hysteresis of input voltage	$V_{INHY}$	0.1	0.3	–	V	–
4.4.31	Pull down current	$I_{IN(1+3)}$	10	25	50	$\mu\text{A}$	$V_{IN(1+3)} = 2\text{ V}$
4.4.32	Pull up current	$I_{IN(2+4)}$	10	25	50	$\mu\text{A}$	$V_{IN(2+4)} = 0.8\text{ V}$

**Input Interface, Logic Inputs INH**

4.4.33	High-input voltage	$V_{INHH}$	2	–	–	V	–
4.4.34	Low-input voltage	$V_{INHL}$	–	–	0.8	V	–
4.4.35	Hysteresis of input voltage	$V_{INHHY}$	–	0.25	–	V	–
4.4.36	Pull down current	$I_{INH}$	10	25	50	$\mu\text{A}$	$V_{INH} = 2\text{ V}$
4.4.37	Disable Delay Time	$t_{d\text{dis}}$	–	–	100	$\mu\text{s}$	$V_S = 13.5\text{ V}$ , resistive
4.4.38	Enable Delay Time	$t_{\text{den}}$	–	–	100	$\mu\text{s}$	Load = $100\ \Omega$ , see <a href="#">Figure 4</a>
4.4.39	Time delay to Sleep Mode	$t_{\text{SLEEP}}$	–	–	40	$\mu\text{s}$	INH = LOW until Sleep mode is reached

**Input Interface, Error-Flags EF(1+2)**

4.4.40	Low-output voltage level	$V_{EFL(1+2)}$	–	0.2	0.4	V	$I_{EF(1+2)} = 2\text{ mA}$
4.4.41	Leakage current	$I_{EFLK(1+2)}$	–	–	10	$\mu\text{A}$	$0\text{ V} < V_{EF(1+2)} < 5.5\text{ V}$
4.4.42	Error delay time	$t_{\text{dEF}}$	–	5	10	$\mu\text{s}$	–

**Thermal Shutdown**

4.4.43	Thermal shutdown junction temperature <sup>1)</sup>	$T_{\text{jSD}}$	150	175	200	$^{\circ}\text{C}$	–
4.4.44	Thermal switch-on junction temperature <sup>1)</sup>	$T_{\text{jSO}}$	125	–	175	$^{\circ}\text{C}$	–

1) Not subject to production test, specified by design

## 5 Block Description

### 5.1 Power Supply

#### 5.1.1 General

The TLE 8444SL has one power supply input  $V_S$  which is connected to the automotive 12V board-net. All power drivers are connected to this supply voltage  $V_S$ . The logic supply voltage for the integrated driver stages and logic block is generated by an internal bandgap reference circuit derived from the 12V board-net. To block the supply voltage of the device, a 47 $\mu$ F electrolytic capacitance is recommended. For EMC improvements a 100nF ceramic capacitance can be added and should be placed as close as possible to the  $V_S$ -Pin of the device. See Application Diagrams, [Figure 18](#) and [Figure 19](#) for more information.

#### 5.1.2 Sleep Mode

The TLE 8444SL can be placed in low current-consumption mode (or sleep mode) by setting the input, INH pin to LOW. The INH pin has an internal pull-down current source. In sleep-mode, all output transistors are switched off. An output disable and enable time is specified and this behavior is shown in [Figure 4](#) below.

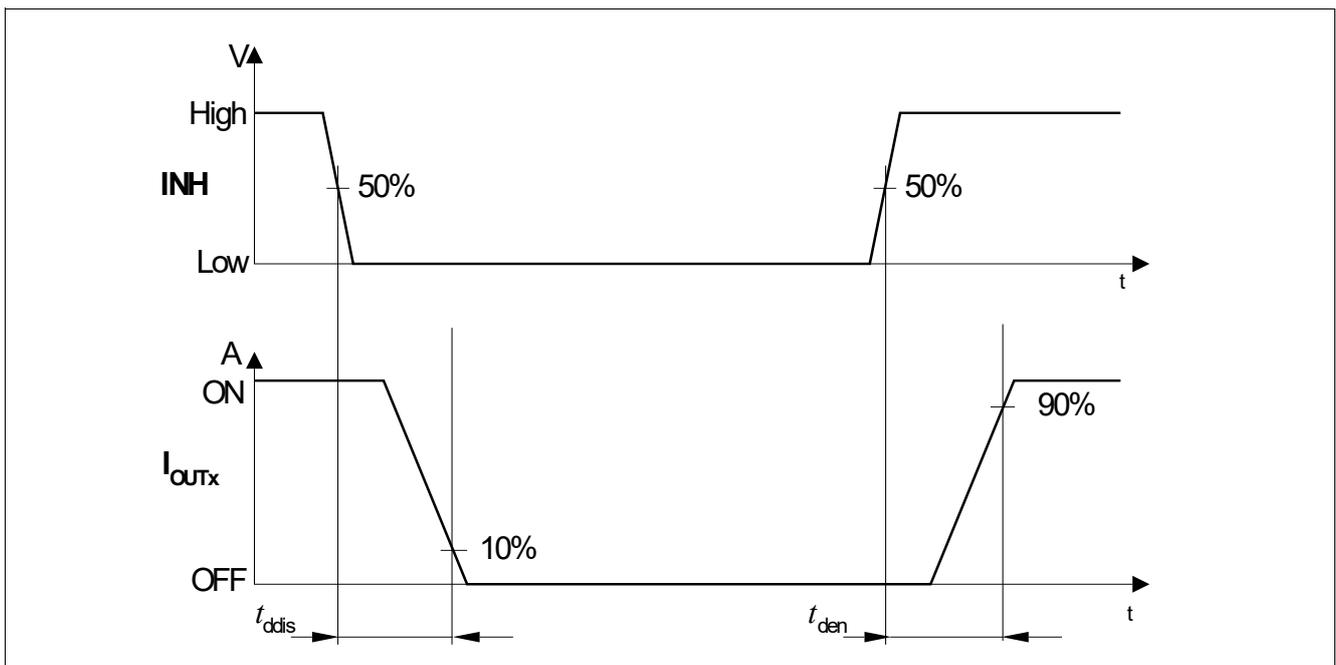


Figure 4 Enable and Disable Delay Time

### 5.1.3 Reverse Polarity

The TLE 8444SL requires an external reverse polarity protection. This protection is essential to avoid an undesired reverse current ( $I_{RB}$ ) to flow from ground potential to battery causing excessive power dissipation across the diodes in the event of reverse polarity. Hence a reverse polarity protection diode is recommended (Figure 5).

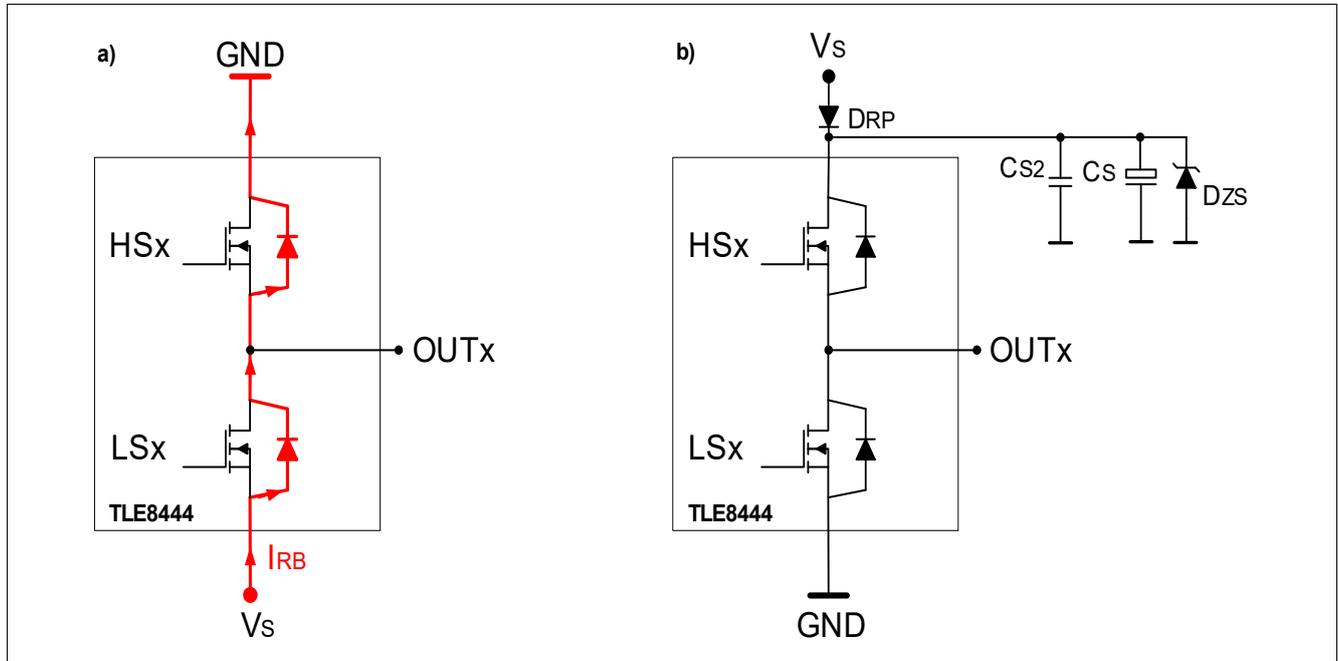


Figure 5 Reverse Polarity Protection

## 5.2 Input / Output Stages

### Input Circuit

The control inputs consist of TTL/CMOS-compatible schmitt-triggers with hysteresis. Inputs IN1 and IN3 have internal pull down circuits whereas IN2 and IN4 have internal pull up circuits. If no signal is applied to the inputs and INH=HIGH, then the drivers will by default be placed in Brake LL mode. In sleep mode, the outputs are switched OFF (tristate or High-Z). For optimized bipolar stepper motor control applications, the IN2 and IN4 inputs have internal inverting structures. This concept allows IN1+IN2 and IN3+IN4 to be tied together, which ultimately reduces  $\mu$ C output pins and provides a '2-phase' type of control to the device (refer to [Figure 19](#) and [Figure 21](#)).

### Output stages

The output stages consist of a total of 4 DMOS Half-bridges. Integrated circuits protect the outputs against overcurrent and overtemperature. Positive and negative voltage spikes, which occur during switching of inductive loads, are suppressed through integrated free-wheeling diodes.

The Truth Table below shows the output behavior of OUT1 and OUT2 for DC-motor applications. The same table is also applied to OUT 3 and OUT4.

**Table 1 Functional Truth Table of Half-bridge 1 and 2 for DC-Motor Application**

INH	IN1	IN2	OUT1	OUT2	Mode
0	X	X	Z	Z	Sleep Mode (Low current consumption mode)
1	open	open	L	L	Brake LL (both low side transistors turned-ON)
1	0	0	L	H	DC-Motor turns counterclockwise (CCW)
1	0	1	L	L	Brake LL (both low side transistors turned-ON)
1	1	0	H	H	Brake HH (both high side transistors turned-ON)
1	1	1	H	L	DC-Motor turns clockwise (CW)

*Note: Half-Bridges 1 and 2 form a full bridge*

The Truth Table below shows the output behavior of OUT1 and OUT2 for bipolar Stepper-motor applications. The same table is also applied to OUT 3 and OUT4.

**Table 2 Functional Truth Table of Half-bridge 1 and 2 for Bipolar Stepper Motor Application**

INH	IN1	IN2	OUT1	OUT2	Mode
0	X	X	Z	Z	Sleep Mode (Low current consumption mode)
1	open	open	L	L	no current (both low side transistors turned-ON)
1	0	0	L	H	negative phase current
1	0	1	L	L	no current (both low side transistors turned-ON)
1	1	0	H	H	no current (both high side transistors turned-ON)
1	1	1	H	L	positive phase current

*Note: Half-Bridges 1 and 2 form a full bridge*

**Block Description**

<b>IN1, IN3</b>	<b>OUT1, OUT3</b>
0 = Logic LOW	Low side transistor is turned-ON High side transistor is turned-OFF
1 = Logic HIGH	High side transistor is turned-ON Low side transistor is turned-OFF
<b>IN2, IN4</b>	<b>OUT2, OUT4</b>
0 = Logic LOW	High side transistor is turned-ON Low side transistor is turned-OFF
1 = Logic HIGH	Low side transistor is turned-ON High side transistor is turned-OFF
X = don't care	X = don't care
	Z  = High- and Lowside transistor are turned-OFF (Output in Tristate, High Z)

## 5.3 Monitoring Functions

### 5.3.1 Diagnostics

The EF1 and EF2 pins are open drain outputs and must be externally connected via pull-up resistors to 5V. In normal conditions, the EF1 and EF2 signals are by default high. In case of an error, EF1 and EF2 pins are pulled low. There are 3 different error conditions that could flag a fault condition:

#### 5.3.1.1 Overcurrent

Output shorted to Ground: If an output transistor is turned on and the current rises above the shutdown threshold  $I_{SD}$  for longer than the shutdown delay time  $t_{d\_SD}$ , the output transistor is turned off and the corresponding diagnosis bit is set. Within this delay time, the current is limited to  $I_{SC}$  as shown in [Figure 9](#). Changing the INHIBIT input resets the error flag. Also a power down event will reset the Error Flag.

- a) Output short to VS: same behavior as short to GND.
- b) Short across the load: same behavior as short to GND.

#### 5.3.1.2 Open load

If the current through the low side transistor is lower than the reference current  $I_{OLD}$  in ON-state for longer than the open-load detection delay time  $t_{d\_OLD}$ , the open-load error flag is set. The output will remain ON. Once the output current increases and  $I_{load} > I_{OLD}$ , the Error Flag will be reset automatically after the  $t_{d\_OLD}$  filter time ([Figure 15](#)).

#### 5.3.1.3 Over voltage / over temperature

- a) **Over voltage:** For voltages below the undervoltage switch OFF threshold ( $V_{UVOFF}$ ) and above the overvoltage switch OFF threshold ( $V_{OVOFF}$ ), the output stages will be switched OFF. The Error Flag however only signals the overvoltage switch OFF case ([Figure 6](#)). A switching hysteresis is implemented at both thresholds to allow an autorecovery mode if the supply voltage is back within the operational range.
- b) **Over Temperature:** At a junction temperature higher than the thermal shutdown temperature  $T_{jSD}$  (typ. 175°C) the device enters thermal shutdown which turns-Off all four output stages simultaneously and the corresponding Error Flags are set with a delay. After cooling down to the thermal switch-on junction temp  $T_{jSO}$  the device will auto restart. A thermal toggle behavior can be observed (the Error Flags and output stages will be modulated by the thermal time constants; [Figure 8](#)).

The Table below shows the behavior of the Error Flags:

**Table 3** Diagnosis

EF1	EF2	Interpretation of Error	Error Flag behavior	Output status	Priority
1	1	no error	-	normal operation	-
1	0	overcurrent	latch	latched switch OFF	2
0	1	open load	auto recovery	normal operation	3
0	0	over voltage / over temperature	auto recovery	auto recovery	1

### 5.3.2 Power Supply Monitoring

The power supply Voltage  $V_S$  is monitored for over- and under voltage (refer to block diagram: [Figure 1](#)). [Figure 6](#) shows the error flag signalling during an undervoltage and overvoltage situation where as [Figure 7](#) shows the hysteresis concept implemented during undervoltage and overvoltage.

#### Under Voltage

If the supply voltage  $V_S$  drops below the switch off voltage  $V_{UVOFF}$ , all output transistors are switched off but the Error Flags remain high (no error). If  $V_S$  rises again and reaches the switch on voltage  $V_{UVON}$ , the power stages are restarted.

#### Over Voltage

If the supply voltage  $V_S$  rises above the switch off voltage  $V_{OVOFF}$ , all output transistors are switched off and the Error Flags are set. The error is not latched, i.e. if  $V_S$  falls again and reaches the switch on voltage  $V_{OVON}$ , the power stages are restarted and the Error Flags are reset.

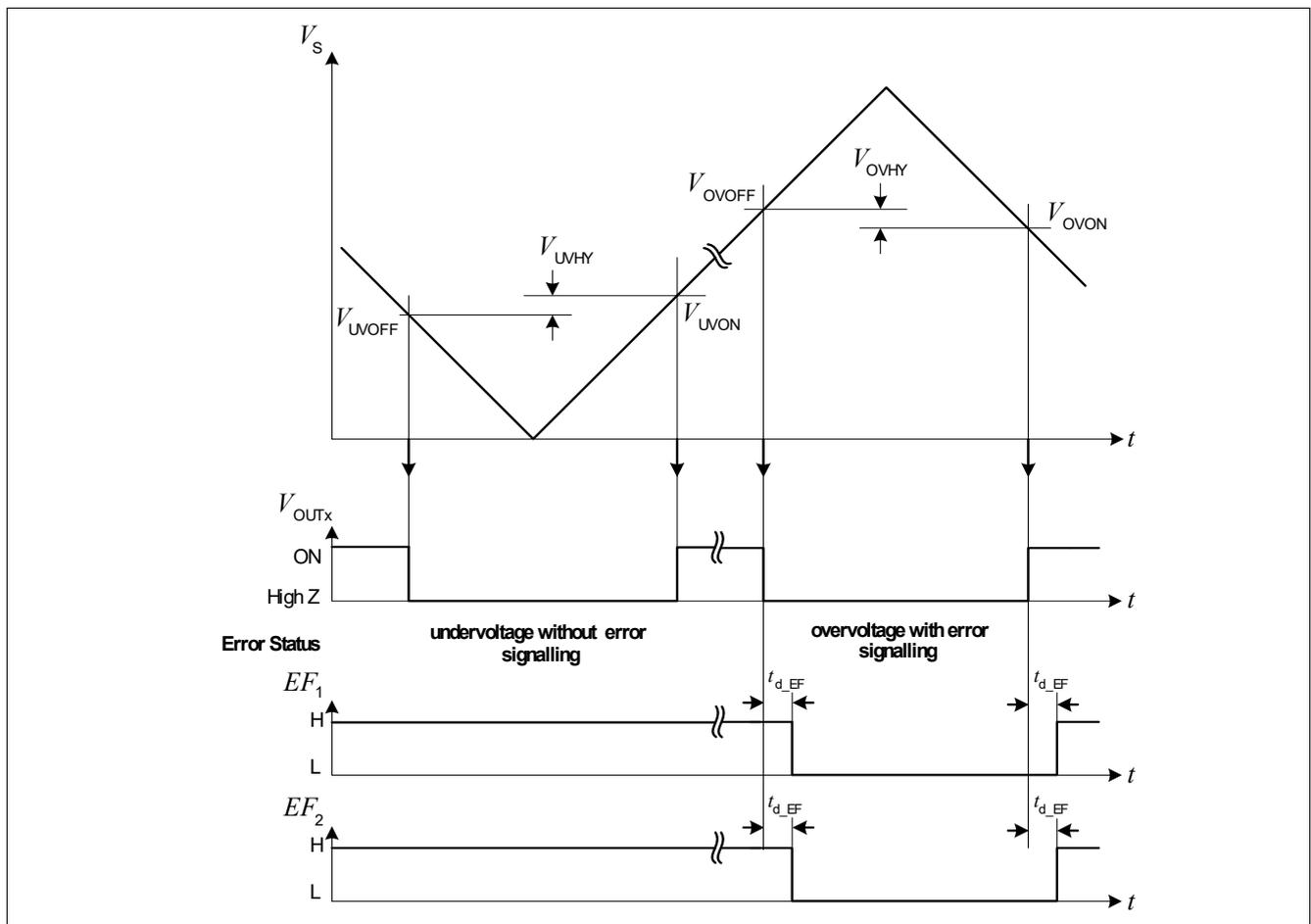


Figure 6 Error Flag behavior for the Over- and Undervoltage case

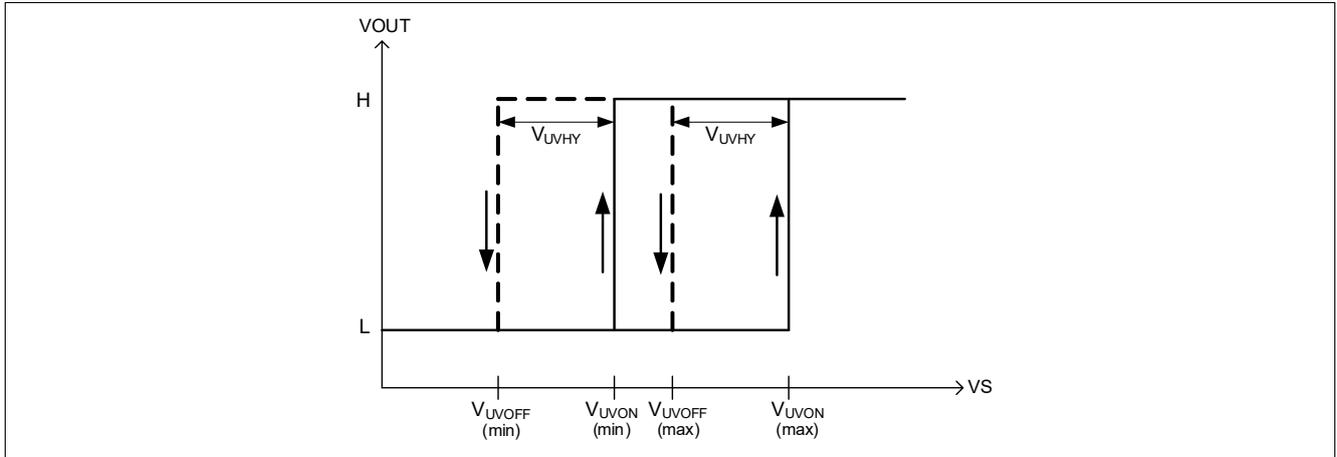


Figure 7 Undervoltage Hysteresis

### 5.3.3 Temperature Monitoring

Temperature sensors are integrated in the power stages. Each half bridge (HS+LS) is equipped with one temperature sensor. The temperature monitoring circuit compares the measured temperature to the shutdown thresholds. If one or more temperature sensors reach the shutdown temperature  $T_{jSD}$ , the overtemperature Error Flag is set to LOW. This Error Flag is not latched (i.e. if the temperature falls below the switch on threshold  $T_{jSO}$ , the Error Flag is automatically reset to HIGH again). This is shown in [Figure 8](#) below.

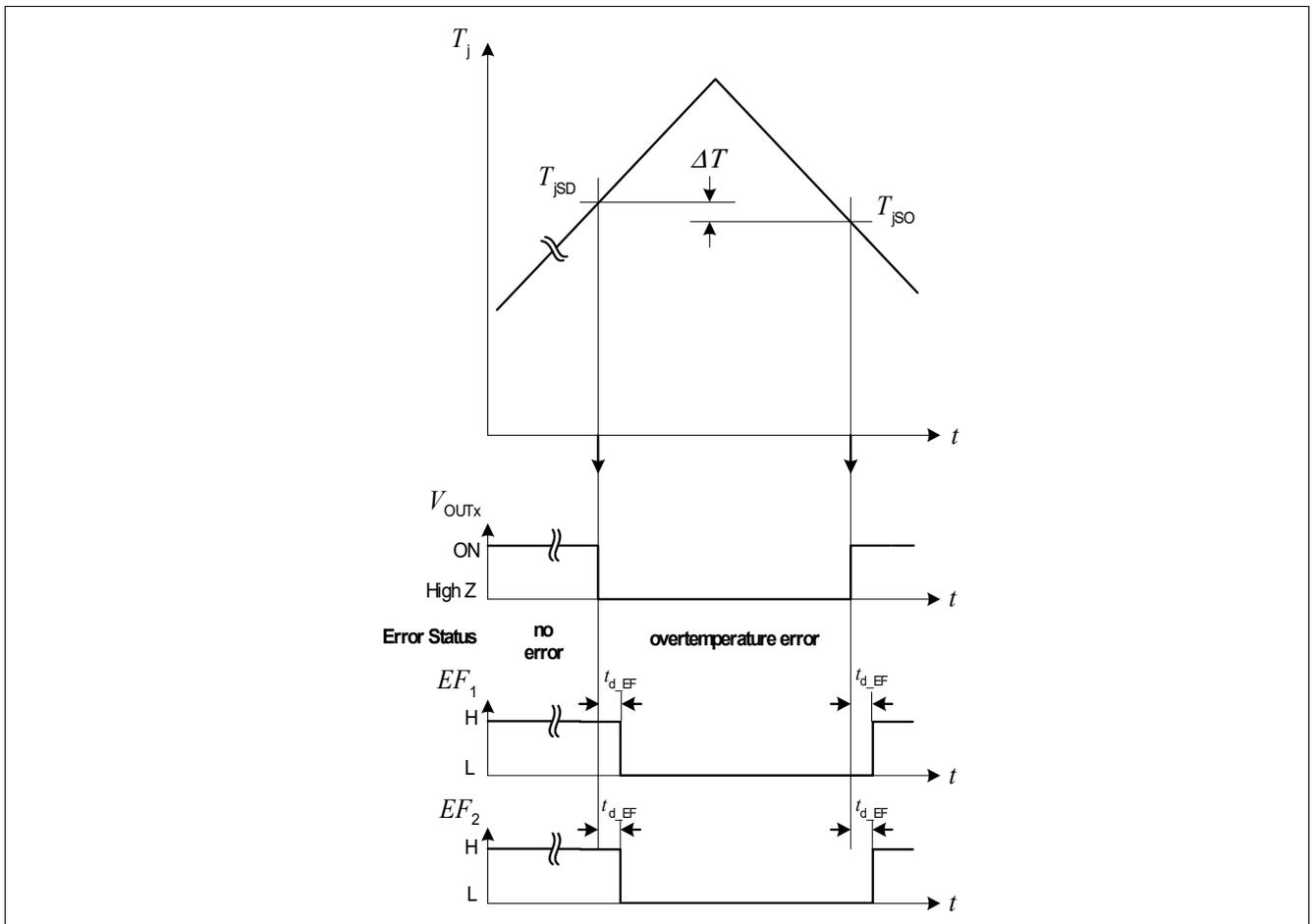


Figure 8 Overtemperature signalling

## 5.4 Power-Outputs 1-4 (Half Bridge Outputs)

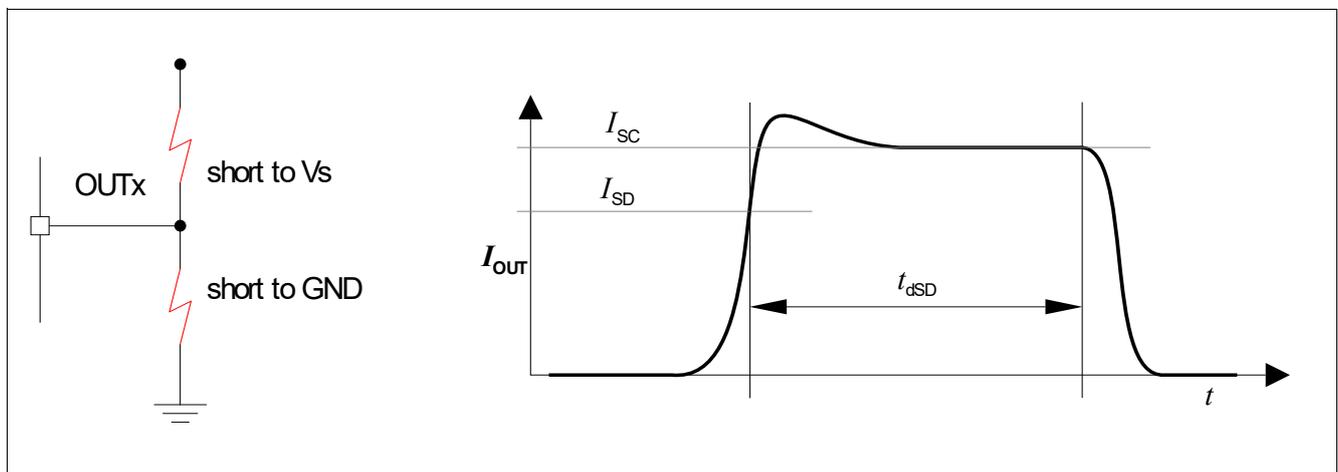
### 5.4.1 Protection and Diagnosis

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this target datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

#### 5.4.1.1 Short Circuit of Output to Ground or Vs

The low-side switches are protected against short circuit to supply and the high-side switches against short to GND.

If a switch is turned on and the current rises above the shutdown threshold  $I_{SD}$  for longer than the shutdown delay time  $t_{dSD}$ , the output transistor is turned off and the corresponding Error Flag is set. Within the delay time, the current is limited to  $I_{SC}$  as shown in [Figure 9](#).



**Figure 9 Short circuit protection**

The delay time is optimized to limit the power that is dissipated in the device during a short circuit event. This scheme allows high peak-currents as required in motor-applications during normal operations.

The output stage stays off and the corresponding diagnostics output information is set until INHIBIT toggles to low and high again or a power-on reset is performed. (refer to [Figure 13](#))

Block Description

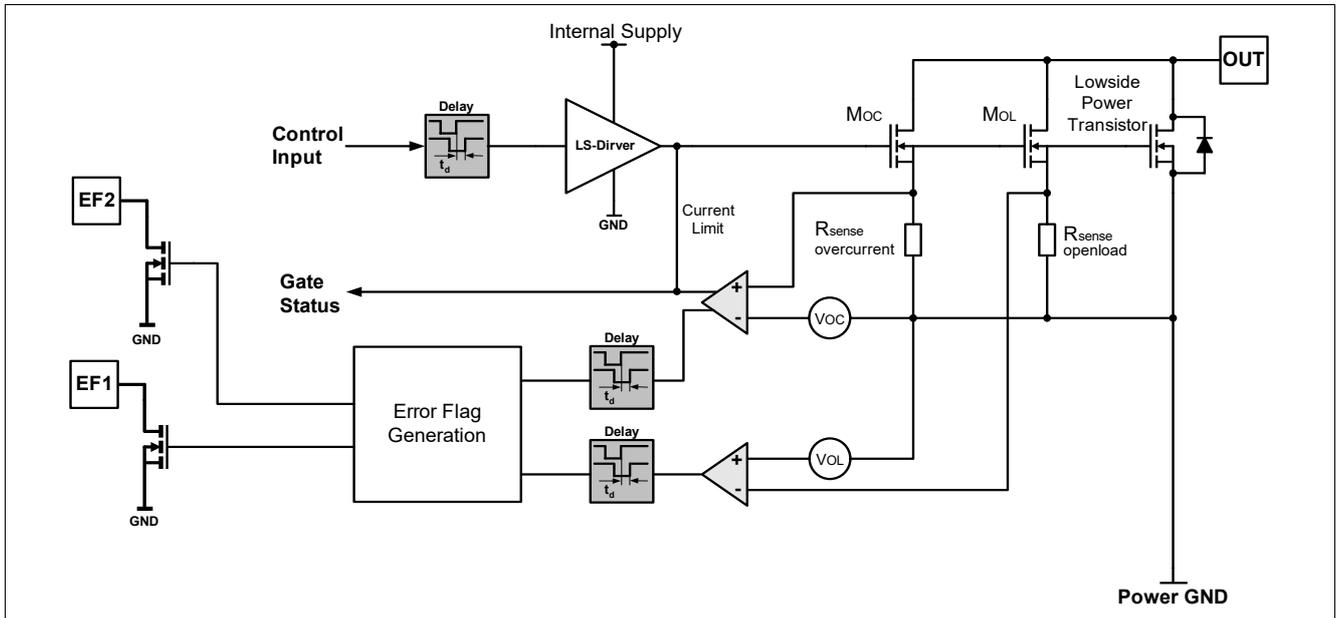


Figure 10 Simplified Schematic for Short circuit protection and Open Load detection in LS-switch

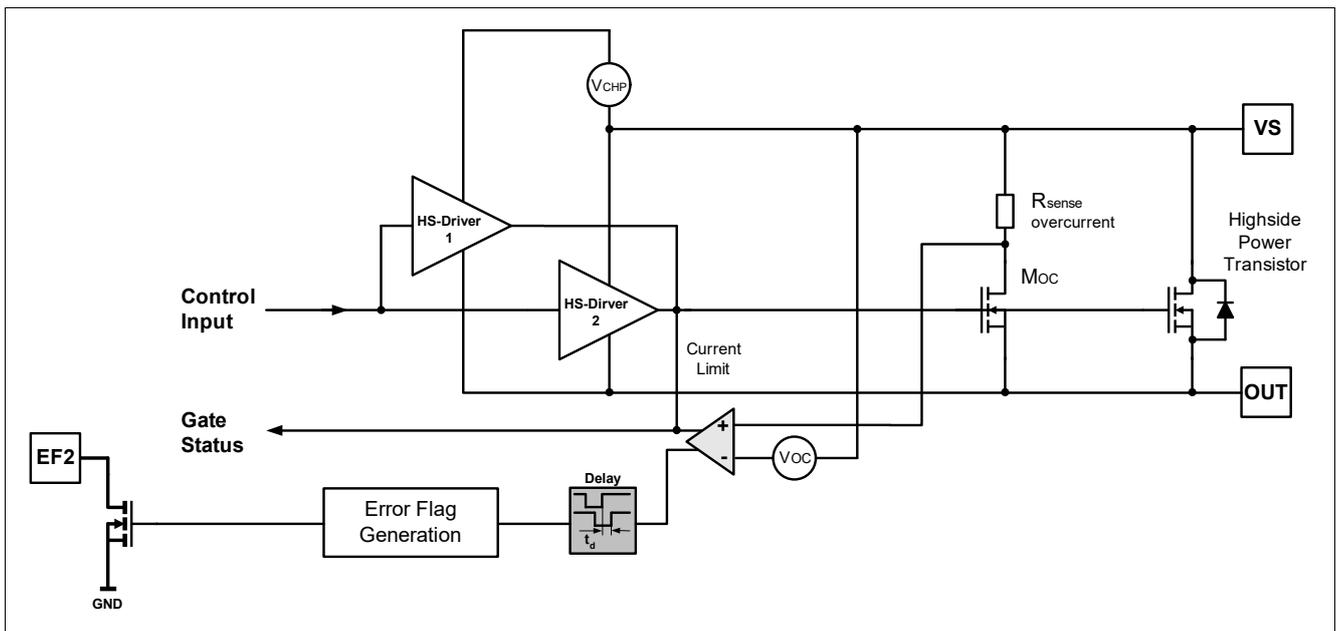


Figure 11 Simplified Schematic for short circuit protection in HS-switch

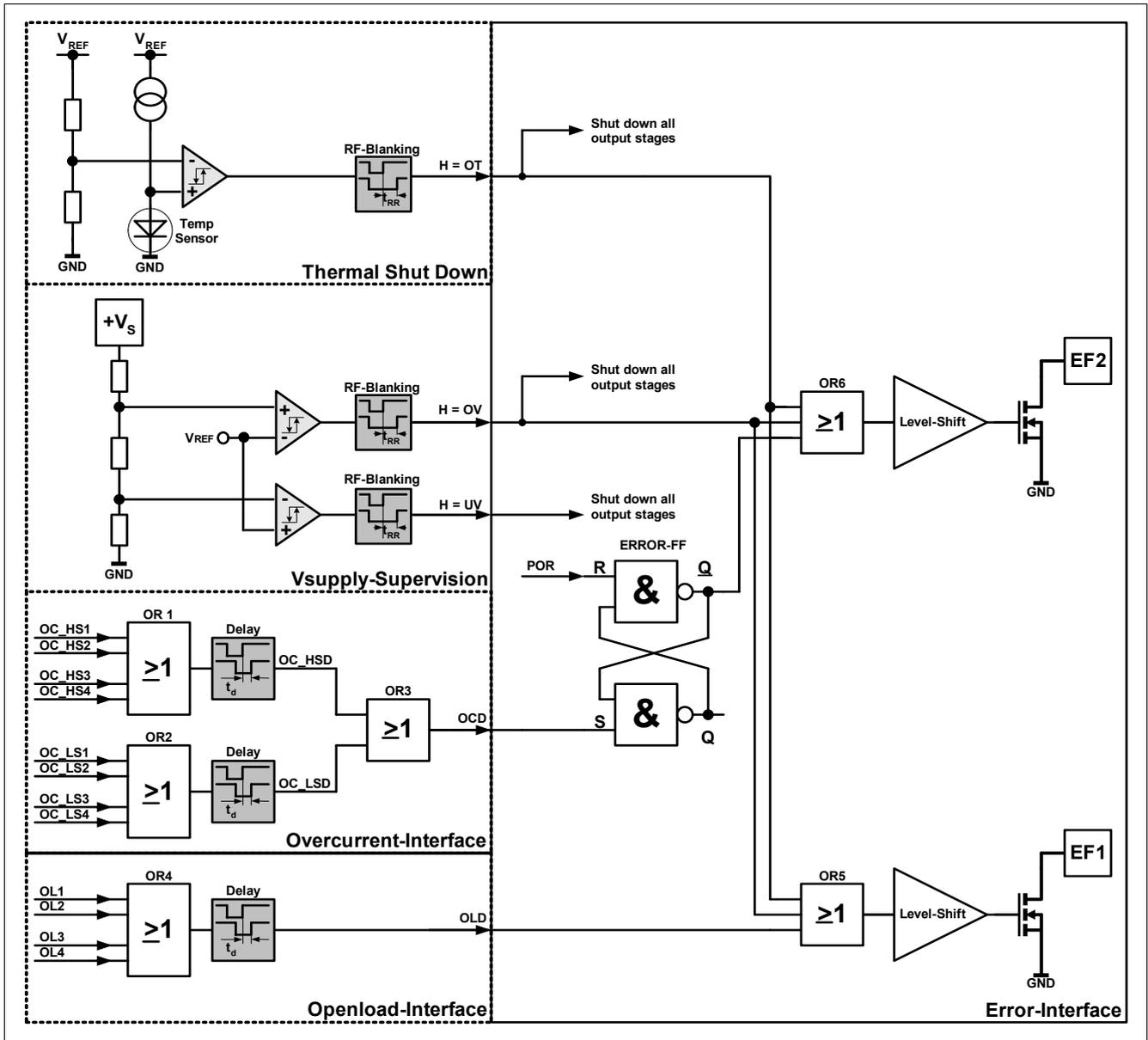
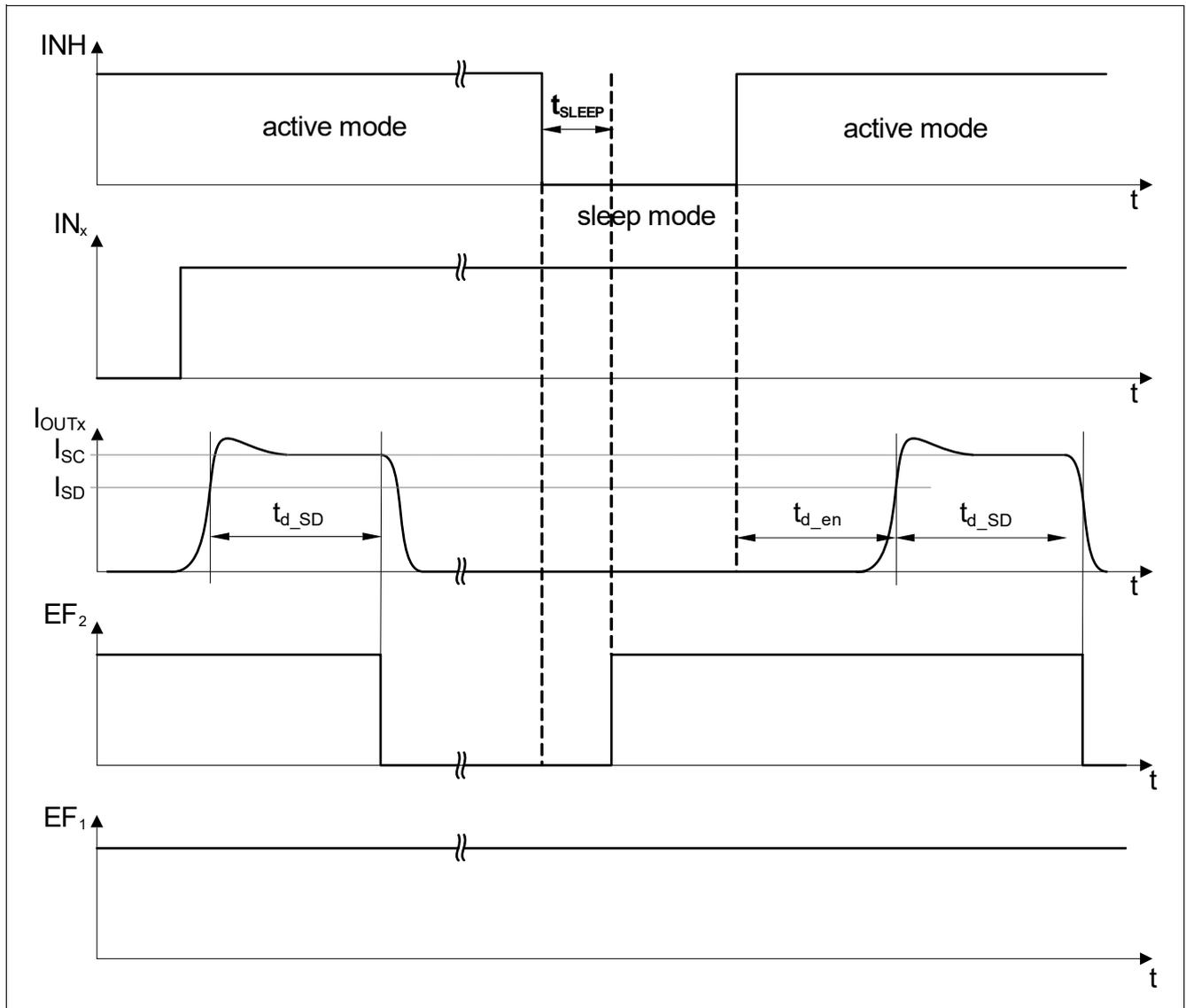


Figure 12 Simplified Schematic of the TLE8444 Error Flag Generation Concept

**Short Circuit Diagnosis**

If a short circuit of a halfbridge output to GND is present, the device will behave like displayed in **Figure 13** below.



**Figure 13** Overcurrent signalling

### 5.4.1.2 Open Load

Open-load detection in ON-state is implemented in the low-side transistors of the bridge outputs. If the current through the low side transistor is lower than the reference current  $I_{OLD}$  in ON-state for longer than the open-load detection delay time  $t_{d\_OLD}$ , the open-load error flag is set. The output transistor, however, remains ON. The open load Error Flag has an autorecovery behavior. Example of open load detection is shown below in [Figure 14](#), [Figure 15](#).

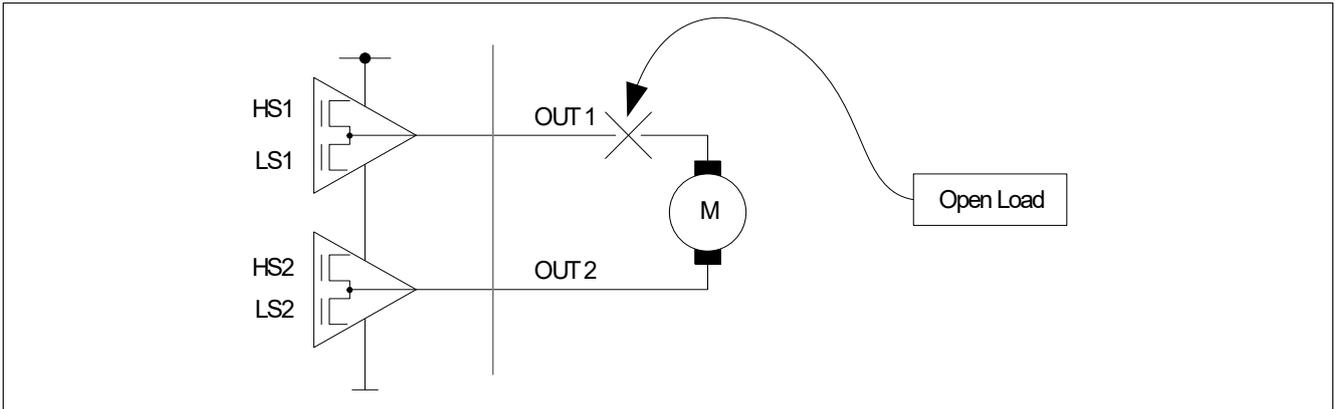


Figure 14 Open Load example

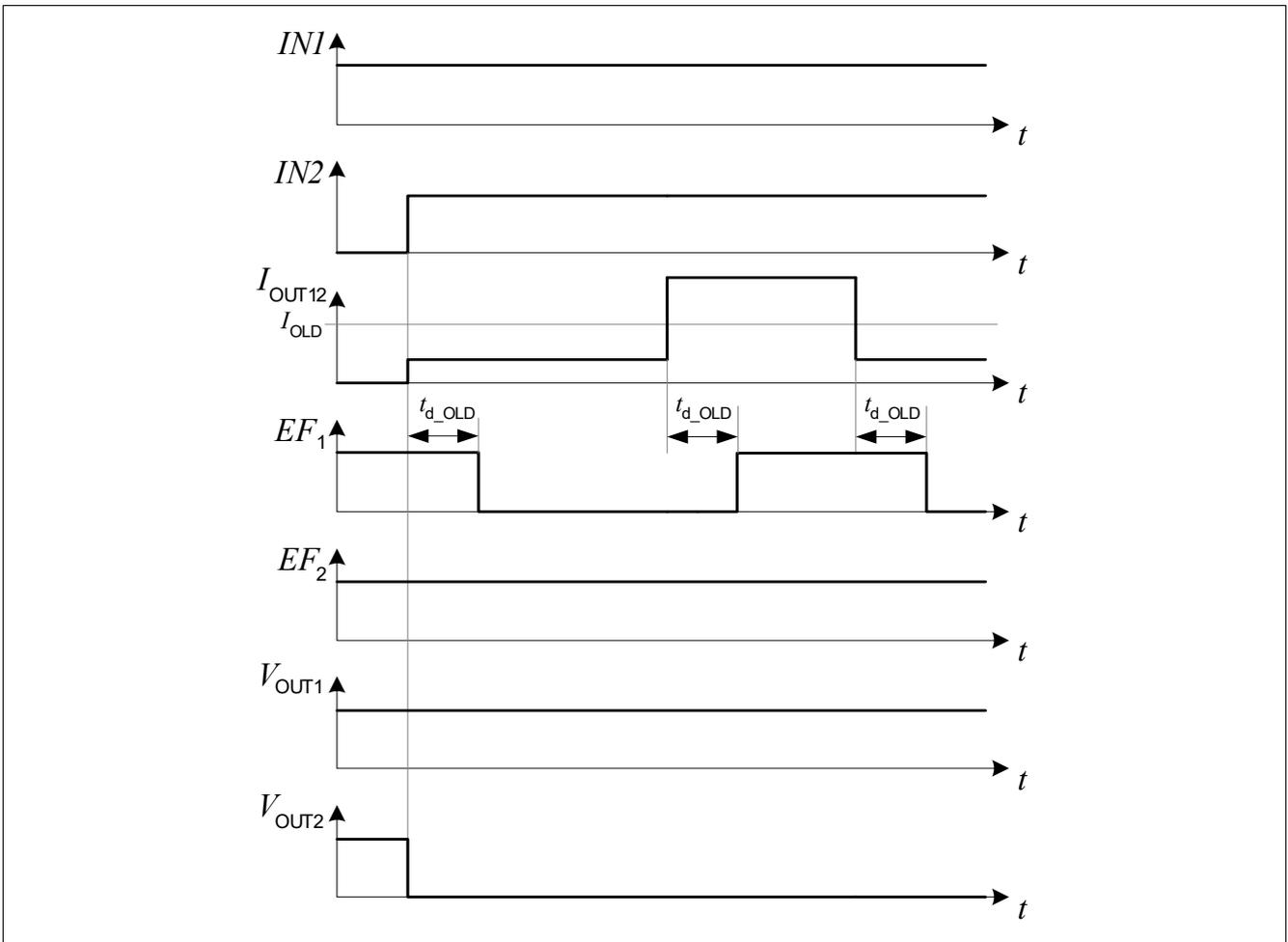


Figure 15 Open Load signalling

## 5.5 Output Switching Capability

### Dead Time to prevent Cross Currents

In bridge configurations the high-side and low-side power transistors are ensured never to be simultaneously “ON” to avoid cross currents. This is usually assured by the integration of delays in the driver stage for the power outputs, generating a so-called dead-time between switching off one Power Transistors while switching on the other Power Transistor of the same half-bridge.

To ensure that there is no overlap of the switching slopes that would lead to a cross current, a dead-time  $t_{db}$  is specified. Refer to [Figure 16](#) and the test circuit in [Figure 17](#).

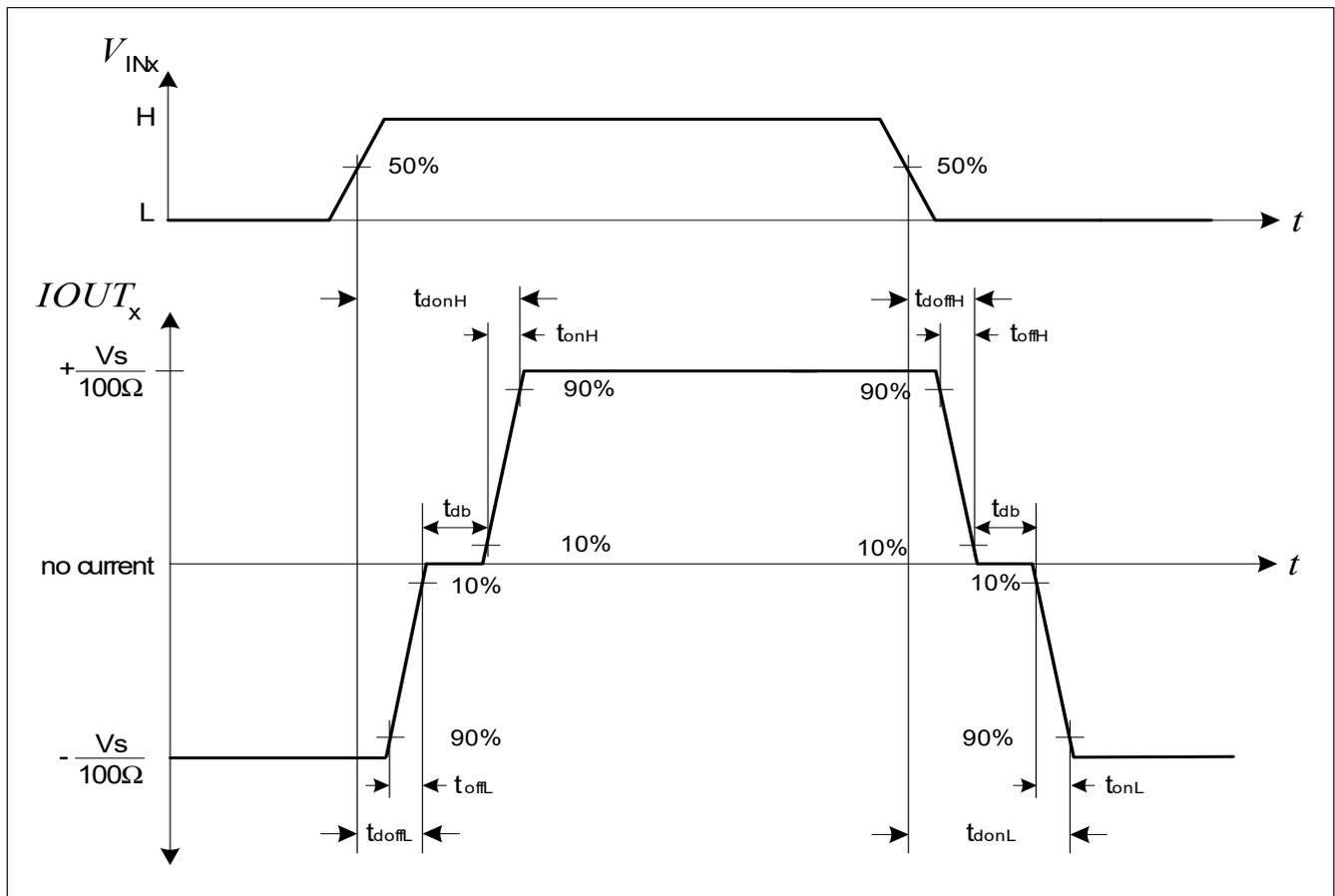


Figure 16 Switching Time Definitions

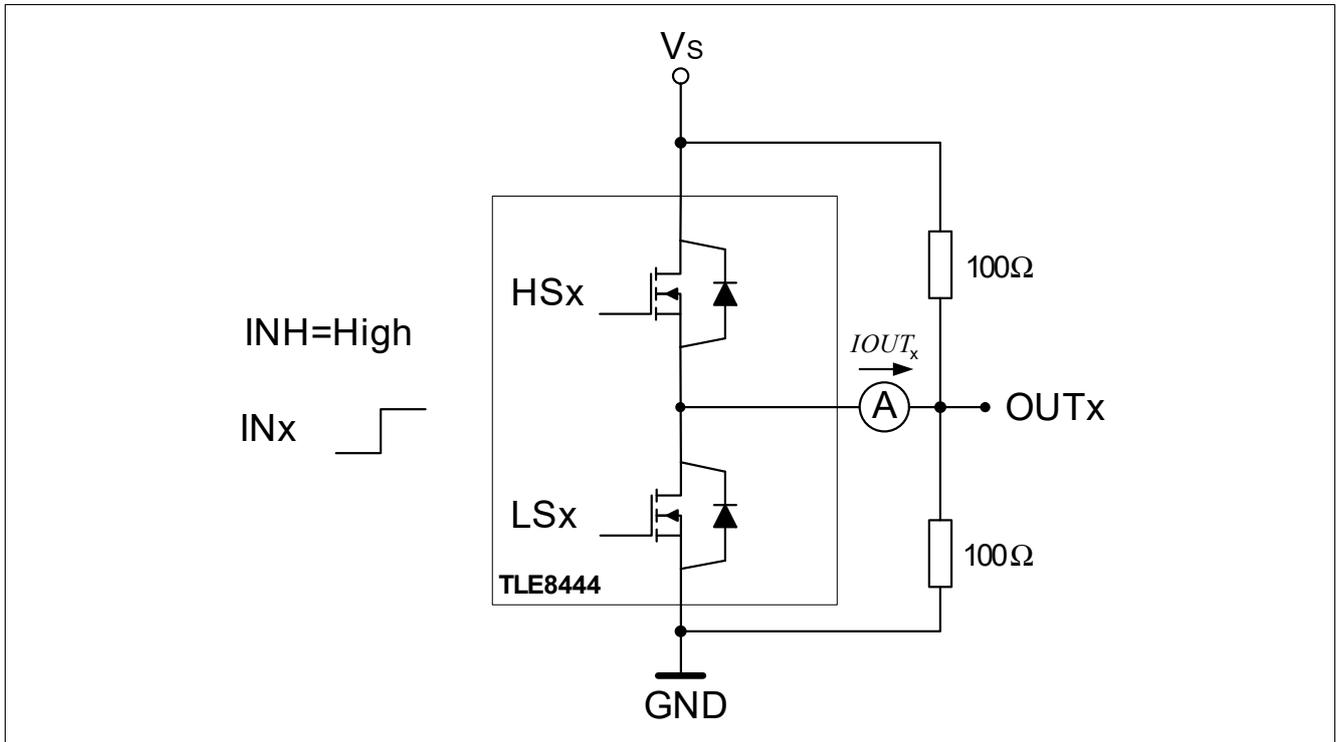


Figure 17 Switching Time Characterization Circuit



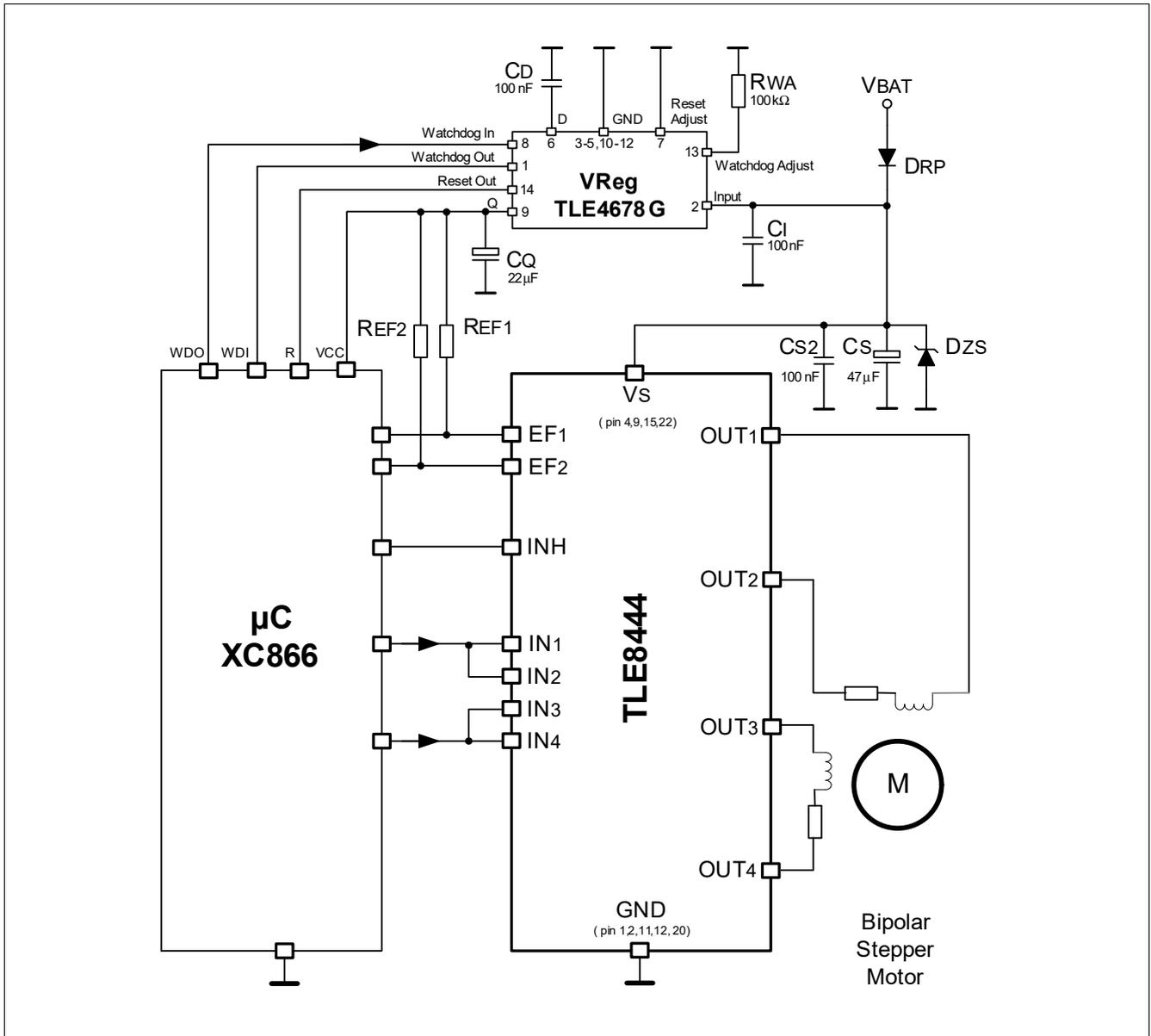


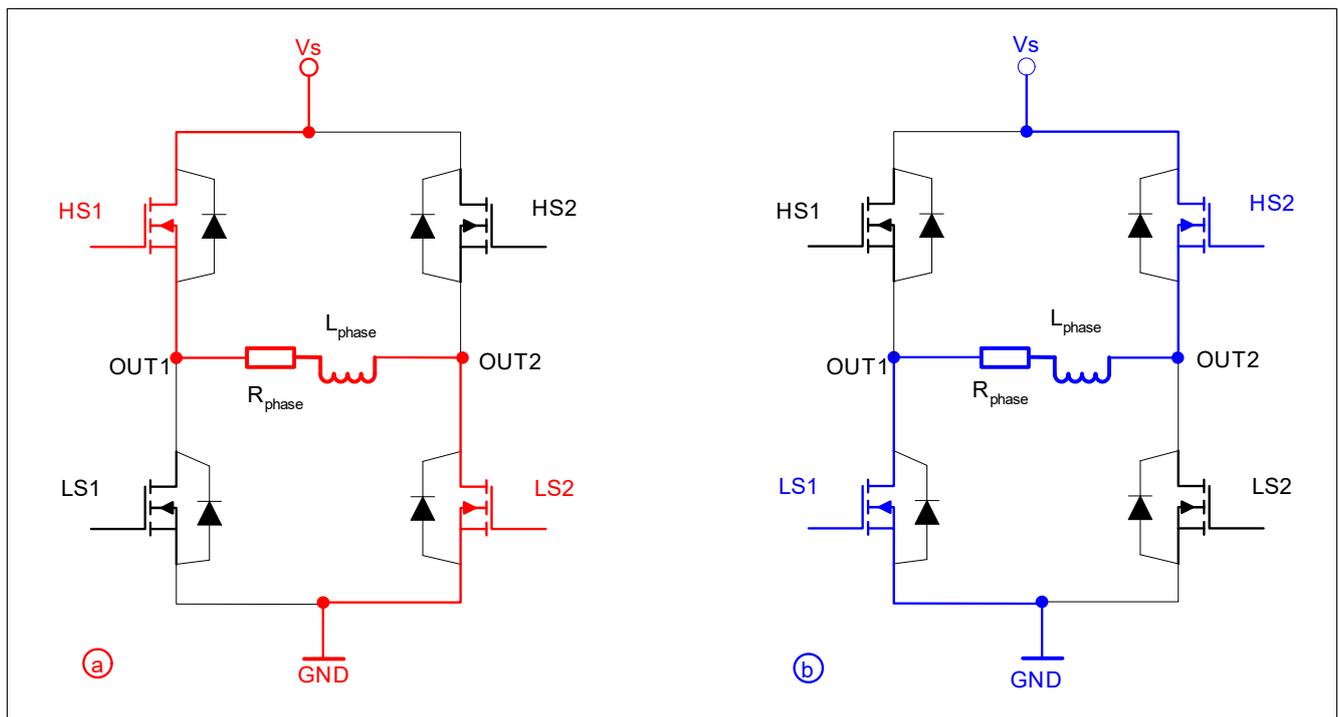
Figure 19 Application Circuit for bipolar stepper motor loads

Note : All VS and GND pins must be externally connected together. CS and CS2 capacitors must be placed as close as possible to the Vs pin for optimized EMC performance.

### 5.5.1 Application Note for Bipolar Stepper Motor Control

#### Current Flow In a H-Bridge for stepper motor control

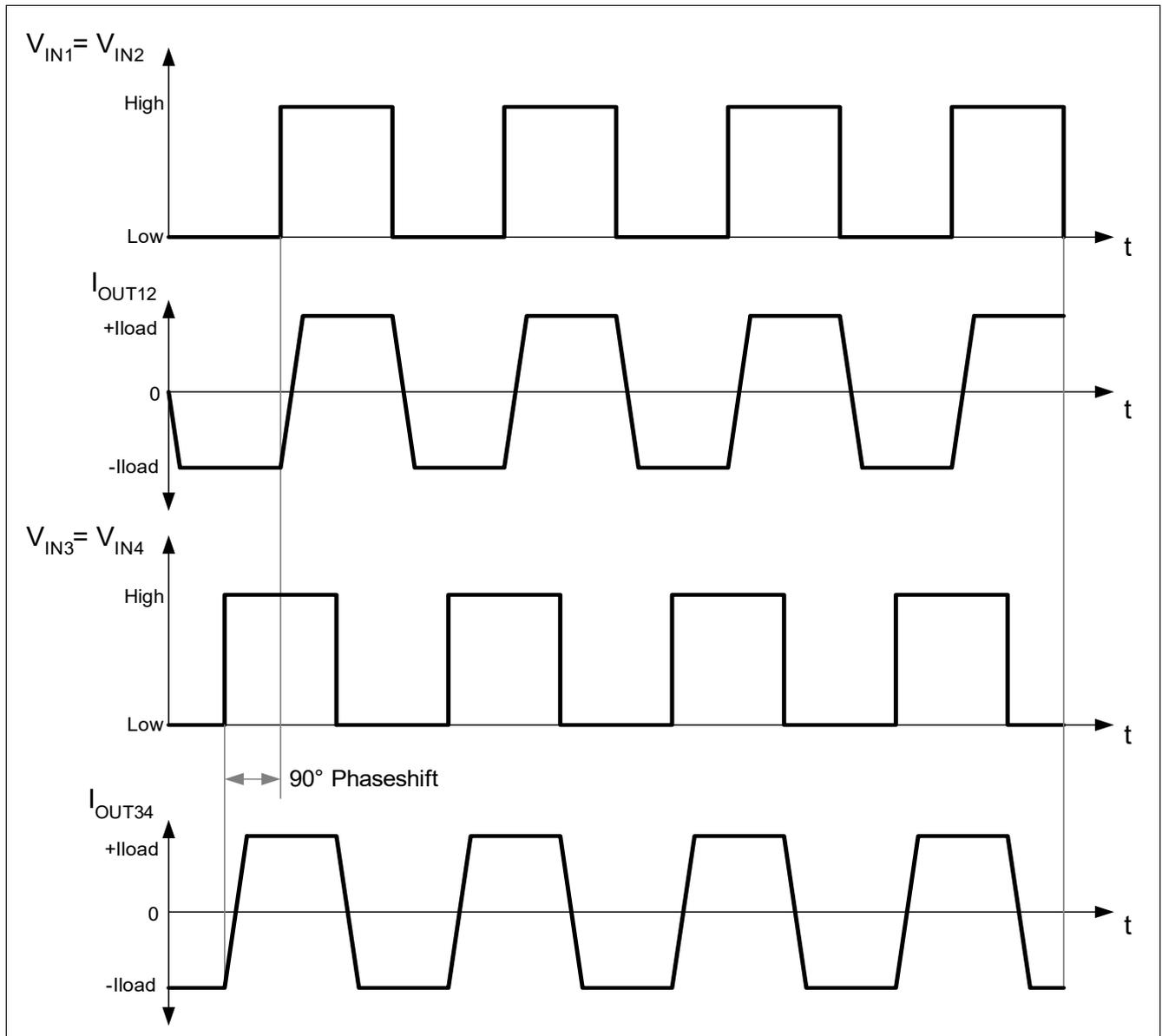
To achieve a continuous movement of a bipolar stepper motor rotor, the phase current has to be reversed step by step. The current flow through a fullbridge is displayed in **Figure 20** below. Picture a) on the left hand side shows a current flow over HS1 the phase coil of the stepper motor load, the LS2 to GND. The next step reverses the current flow through the phase coil of the motor by switching off HS1 and LS2 and activating HS2 and LS1 instead (Picture b).



**Figure 20** Reversing the current in fullbridge operation to achieve a stepper motor movement

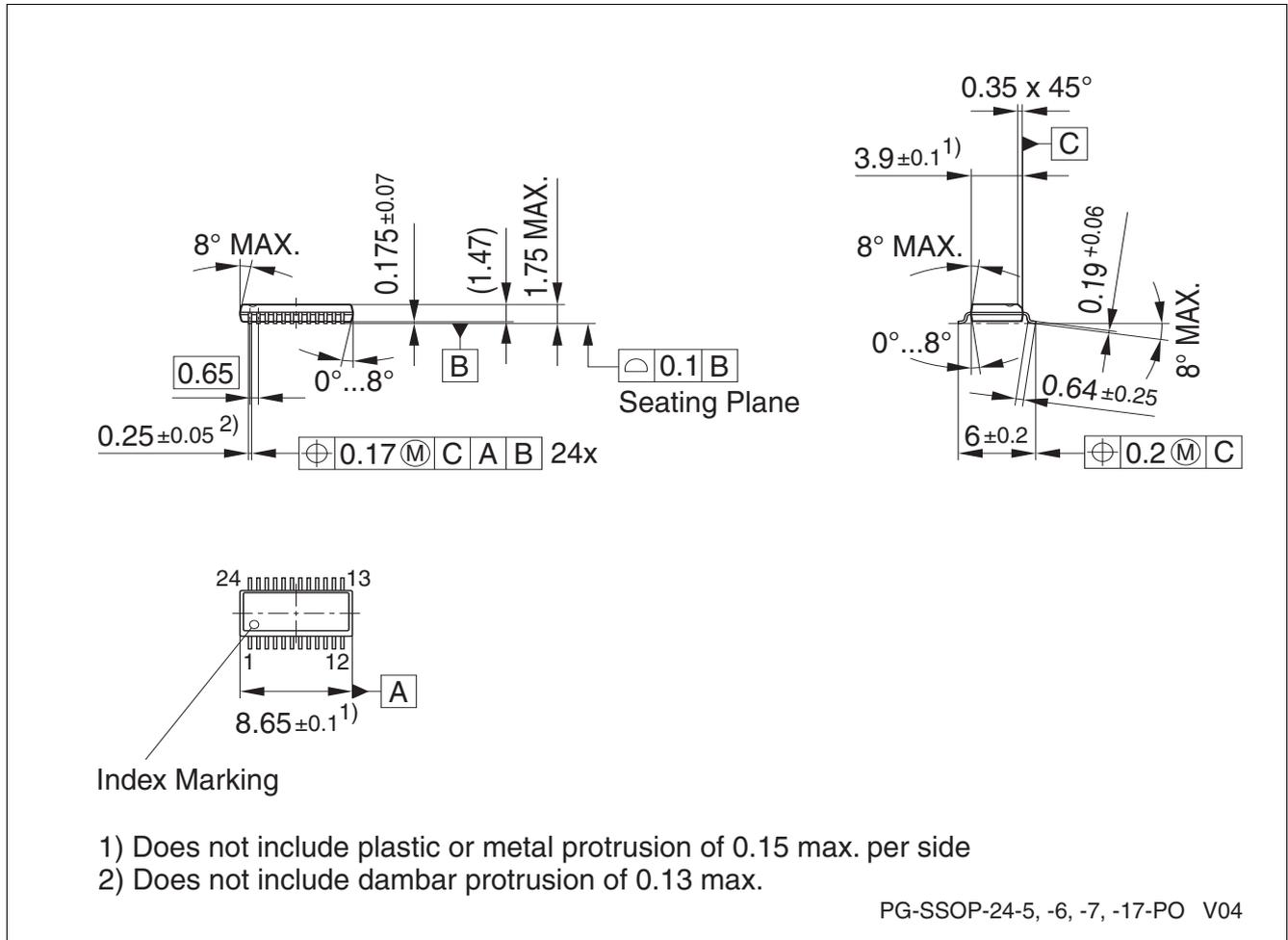
**Control pattern for bipolar stepper motor applications**

Bipolar stepper motors applications for linear positioning such as Idle Speed control requires a specific input signal pattern which is displayed in [Figure 21](#). Normally, the output switching frequency is lower (approx. < 2kHz). This depends on the used motorload (L/R ratio).



**Figure 21 Bipolar stepper motor control (full step mode)**

## 6 Package Outlines



**Figure 22 PG-SSOP-24 (Plastic/Plastic Green - Dual Small Outline Package)**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 7 Revision History

0.40.3

**TLE 8444SL****Revision History: Rev. 1.2, 2022-10-07**

<b>Version</b>	<b>Subjects (major changes since last revision)</b>
1.2	Package suffix deleted Package drawing with updated standoff
1.1	Package Illustration on overview sheet corrected from exposed pad to standard SSOP package
1.0	Final Data Sheet Release

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