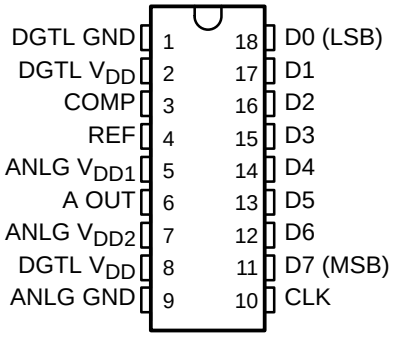
- **8-Bit Resolution**
- **±0.2% Linearity**
- **Maximum Conversion Rate**
  - **30 MHz Typ**
  - **20 MHz Min**
- **Analog Output Voltage Range V_{DD} to V_{DD} −1 V**
- **TTL Digital Input Voltage**
- **5-V Single Power-Supply Operation**
- **Low Power Consumption . . . 80 mW Typ**
- **Interchangeable With Fujitsu MB40778**

description

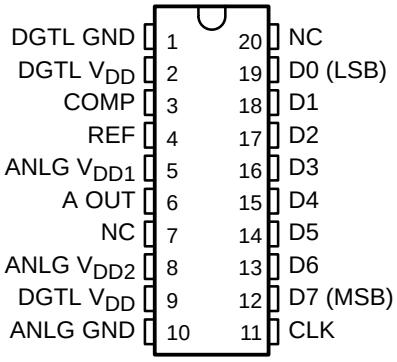
The TLC5602x devices are low-power, ultra-high-speed video, digital-to-analog converters that use the LinEPIC™ 1-µm CMOS process. The TLC5602x converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of high-speed operation, the TLC5602x devices are suitable for digital video applications such as digital television, video processing with a computer, and radar-signal processing.

The TLC5602C is characterized for operation from 0°C to 70°C. The TLC5602M is characterized over the full military temperature range of –55°C to 125°C.

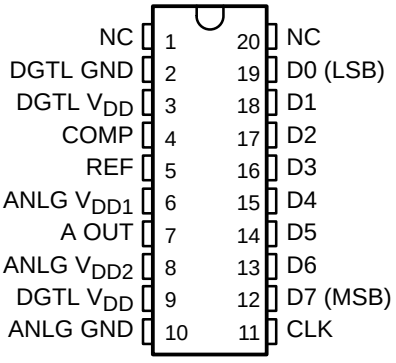
N PACKAGE
(TOP VIEW)



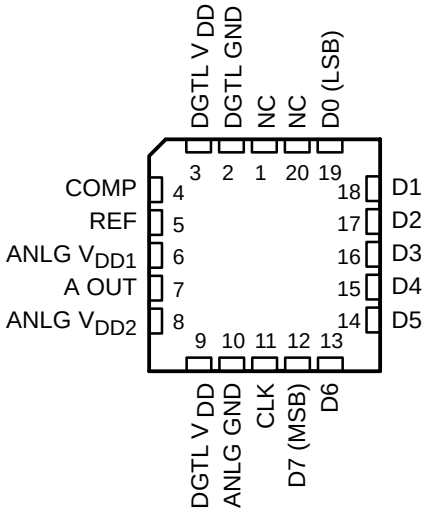
DW PACKAGE
(TOP VIEW)



J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

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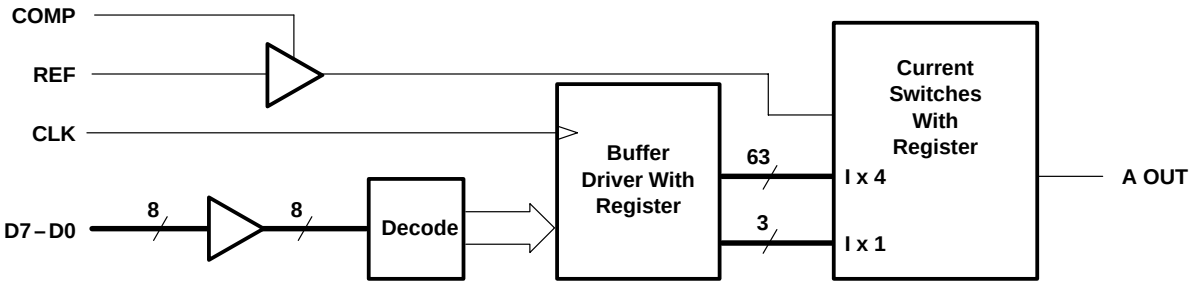
AVAILABLE OPTIONS

PACKAGE				
T_A	WIDE-BODY SMALL OUTLINE (DW)	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC5602CDW			TLC5602CN
–55°C to 125°C		TLC5602MFK	TLC5602MJ	

functional block diagram

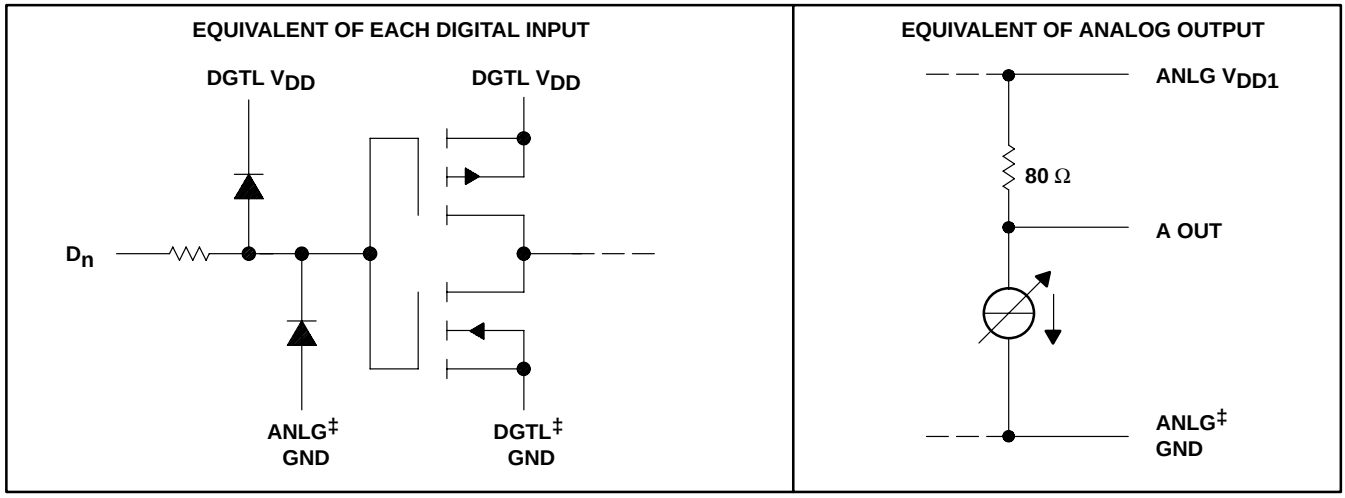


FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	H	3.984 V
⋮					⋮				⋮
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
⋮					⋮				⋮
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

† V_{DD} = 5 V and V_{ref} = 4.02 V

schematics of equivalent input and output



‡ ANLG GND and DGTL GND do not connect internally and should be tied together as close to the device terminals as possible.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, ANLG V_{DD}, DGTL V_{DD} . . . . . –0.5 V to 7 V
Digital input voltage range, V_I . . . . . –0.5 V to 7 V
Analog reference voltage range, V_{ref} . . . . . V_{DD} – 1.7 V to V_{DD} + 0.5 V
Operating free-air temperature range, T_A: TLC5602C . . . . . 0°C to 70°C
TLC5602M . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
Analog reference voltage, V_{ref}		3.8	4	4.2	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Pulse duration, CLK high or low, t_w		25			ns
Setup time, data before CLK↑, t_{su}		16.5			ns
Hold time, data after CLK↑, t_h		12.5			ns
Phase compensation capacitance, C_{comp} (see Note 1)		1			μF
Load resistance, R_L		75			Ω
Operating free-air temperature, T_A	TLC5602C	0		70	°C
	TLC5602M	–55		125	

NOTE 1: The phase compensation capacitor should be connected between COMP and ANLG GND.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current	Digital inputs	V_I = 5 V					±1	µA
I_{IL}	Low-level input current		V_I = 0 V					±1	µA
I_{ref}	Input reference current		V_{ref} = 4 V					10	µA
V_{FS}	Full-scale analog output voltage		V_{DD} = 5 V,	V_{ref} = 4.02 V		V_{DD}−15	V_{DD}	V_{DD}+15	mV
V_{ZS}	Zero-scale analog output voltage		V_{DD} = 5 V, T_A = full range§	V_{ref} = 4.02 V,	TLC5602C	3.919	3.98	4.042	V
					TLC5602M	3.919	3.98	4.042	
					TLC5602M	3.919	3.98	4.062	
r_o	Output resistance		T_A = 25°C		TLC5602C	60	80	120	Ω
			T_A = full range§		TLC5602M				
C_i	Input capacitance		f_{clock} = 1 MHz,	T_A = 25°C			15		pF
I_{DD}	Supply current		f_{clock} = 20 MHz,	V_{ref} = V_{DD} − 0.95 V			16	25	mA

‡ All typical values are at V_{DD} = 5 V and T_A = 25°C.
§ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is –55°C to 125°C.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$E_{L(adj)}$	Linearity error, best-straight-line	T_A = full range‡	TLC5602C			±0.2%	
		T_A = 25°C	TLC5602M			±0.2%	
		T_A = full range‡				±0.4%	
E_L	Linearity error, end point				±0.15%		
E_D	Linearity error, differential					±0.2%	
G_{diff}	Differential gain	NTSC 40-IRE modulated ramp, f_{clock} = 14.3 MHz, Z_L ≥ 75 kΩ			0.7%		
f_{diff}	Differential phase				0.4°		
t_{pd}	Propagation delay time, CLK to analog output	C_L = 10 pF			25		ns
t_s	Settling time to within 1/2 LSB	C_L = 10 pF			30		ns

† All typical values are at V_{DD} = 5 V and T_A = 25°C.
‡ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is –55°C to 125°C.

PARAMETER MEASUREMENT INFORMATION

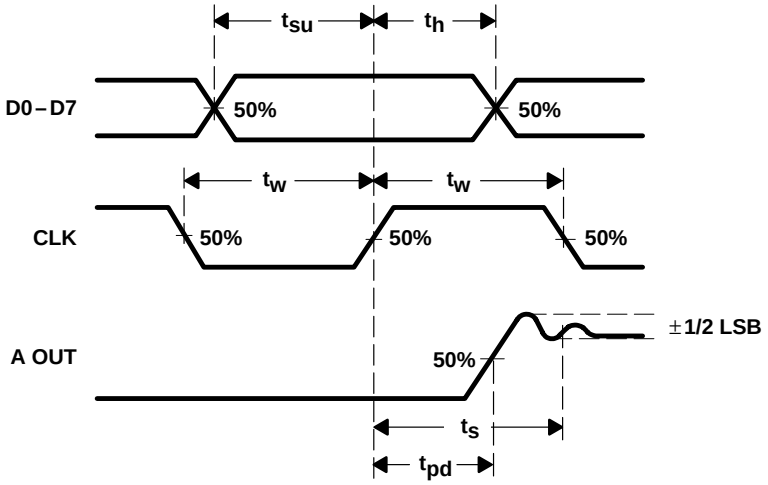


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS

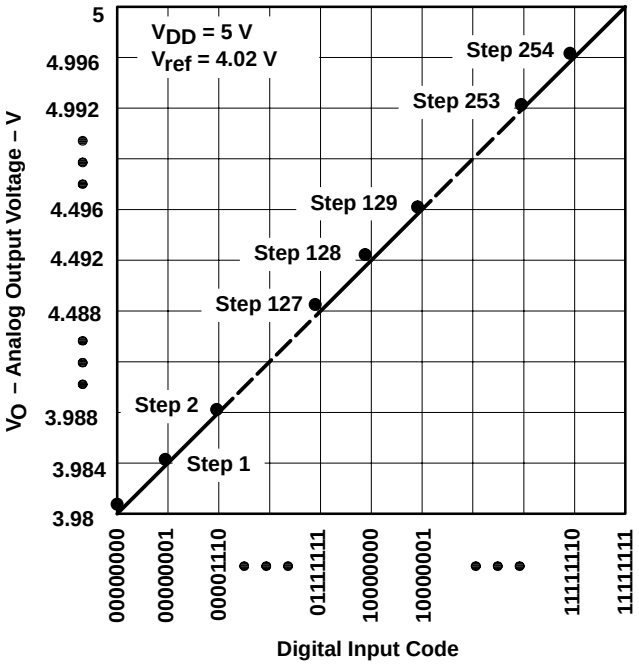


Figure 2

BEST-STRAIGHT-LINE LINEARITY ERROR

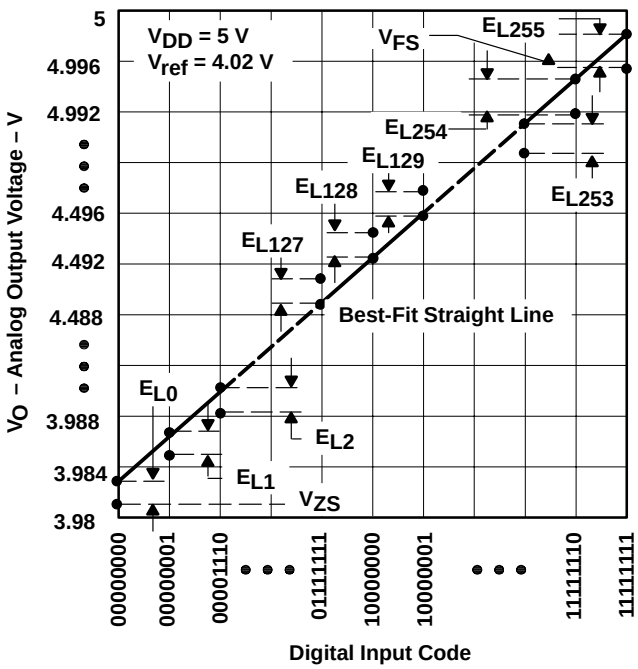
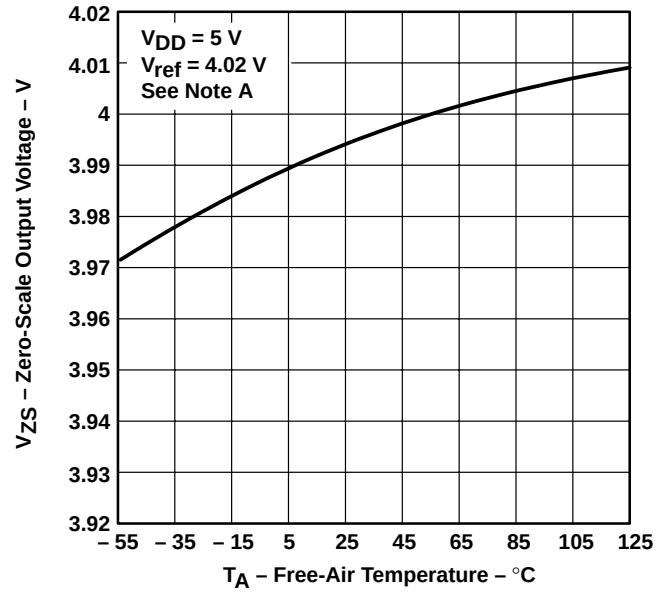


Figure 3

ZERO-SCALE OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE



NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 4

OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE

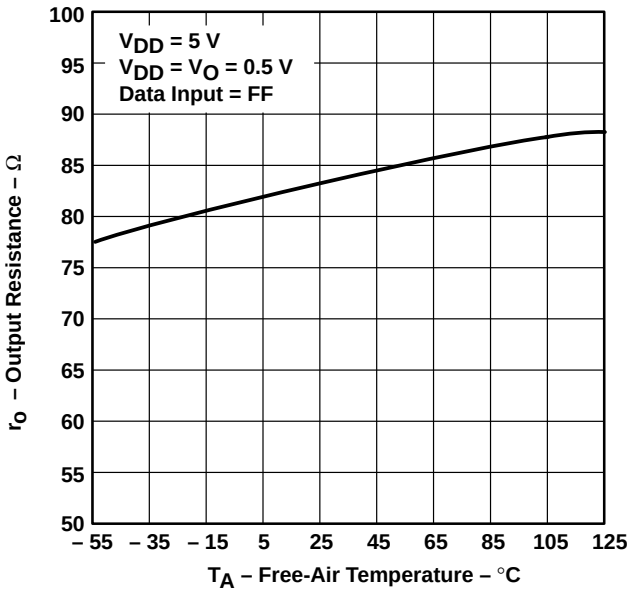


Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

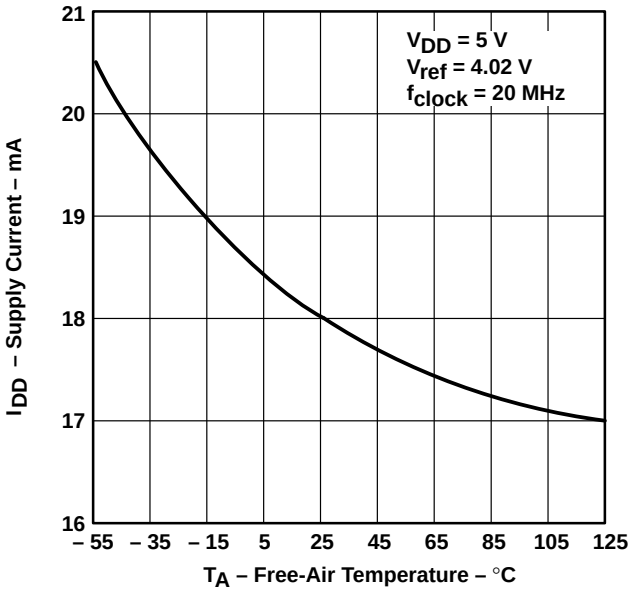
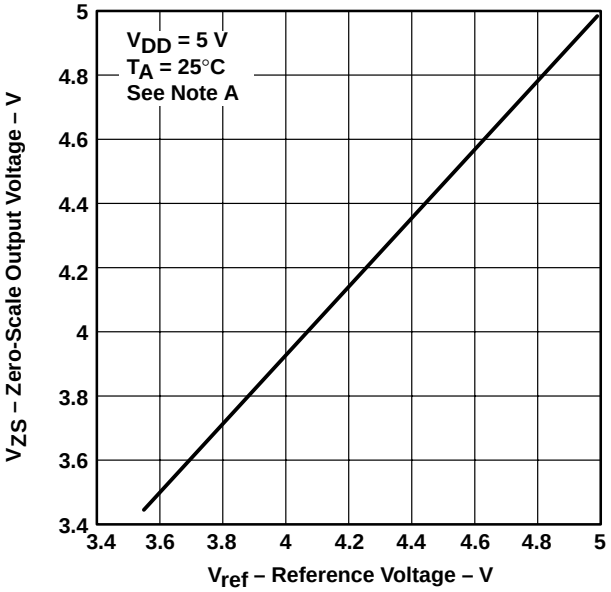


Figure 6

ZERO-SCALE OUTPUT VOLTAGE vs REFERENCE VOLTAGE



NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 7

APPLICATION INFORMATION

The following design recommendations benefit the TLC5602 user:

- Physically separate and shield external analog and digital circuitry as much as possible to reduce system noise.
- Use RF breadboarding or RF printed-circuit-board (PCB) techniques throughout the evaluation and production process.
- Since ANLG GND and DGTL GND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should connect to the power-supply ground through separate leads with proper supply bypassing. A good method is to use a separate twisted pair for the analog and digital supply lines to minimize noise pickup.

  Use wide ground leads or a ground plane on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- ANLG V_{DD} and DGTL V_{DD} are also separated internally, so they must connect externally. These external PCB leads should also be made as wide as possible. Place a ferrite bead or equivalent inductance in series with ANLG V_{DD} and the decoupling capacitor as close to the device terminals as possible before the ANLG V_{DD} and DGTL V_{DD} leads are connected together on the board.
- Decouple ANLG V_{DD} to ANLG GND and DGTL V_{DD} to DGTL GND with a 1-μF and 0.01-μF capacitor, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01-μF capacitor.
- Connect the phase compensation capacitor between COMP and ANLG GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to ANLG GND.
- Shield ANLG V_{DD}, ANLG GND, and A OUT from the high-frequency terminals CLK and D7–D0. Place ANLG GND traces on both sides of the A OUT trace on the PCB.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5602CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC5602C	Samples
TLC5602CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC5602C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

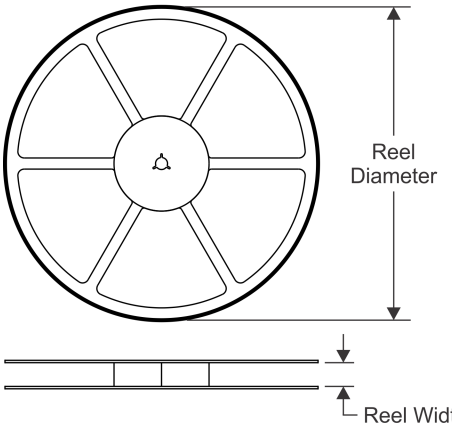
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

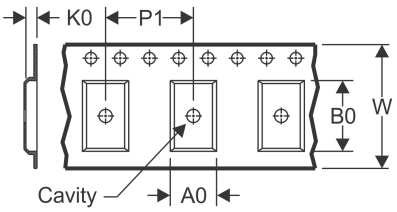
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

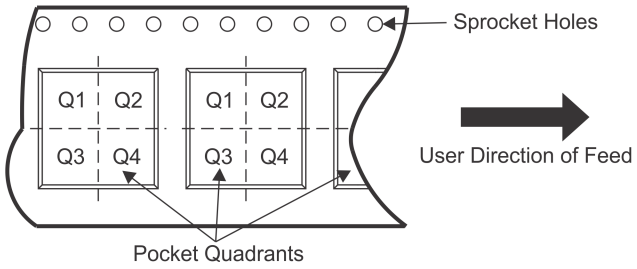


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

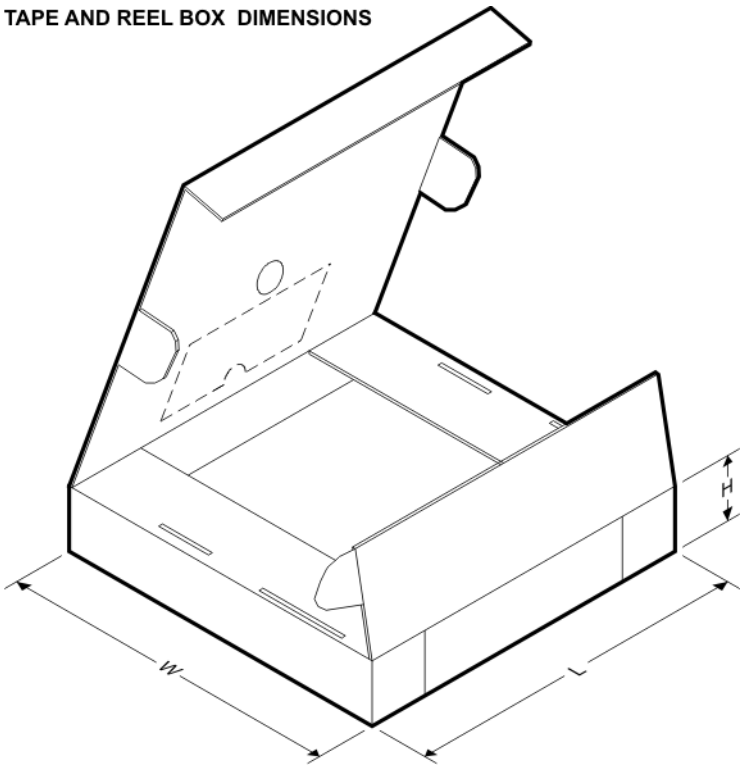
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

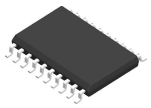
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5602CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5602CDWR	SOIC	DW	20	2000	535.4	167.6	48.3

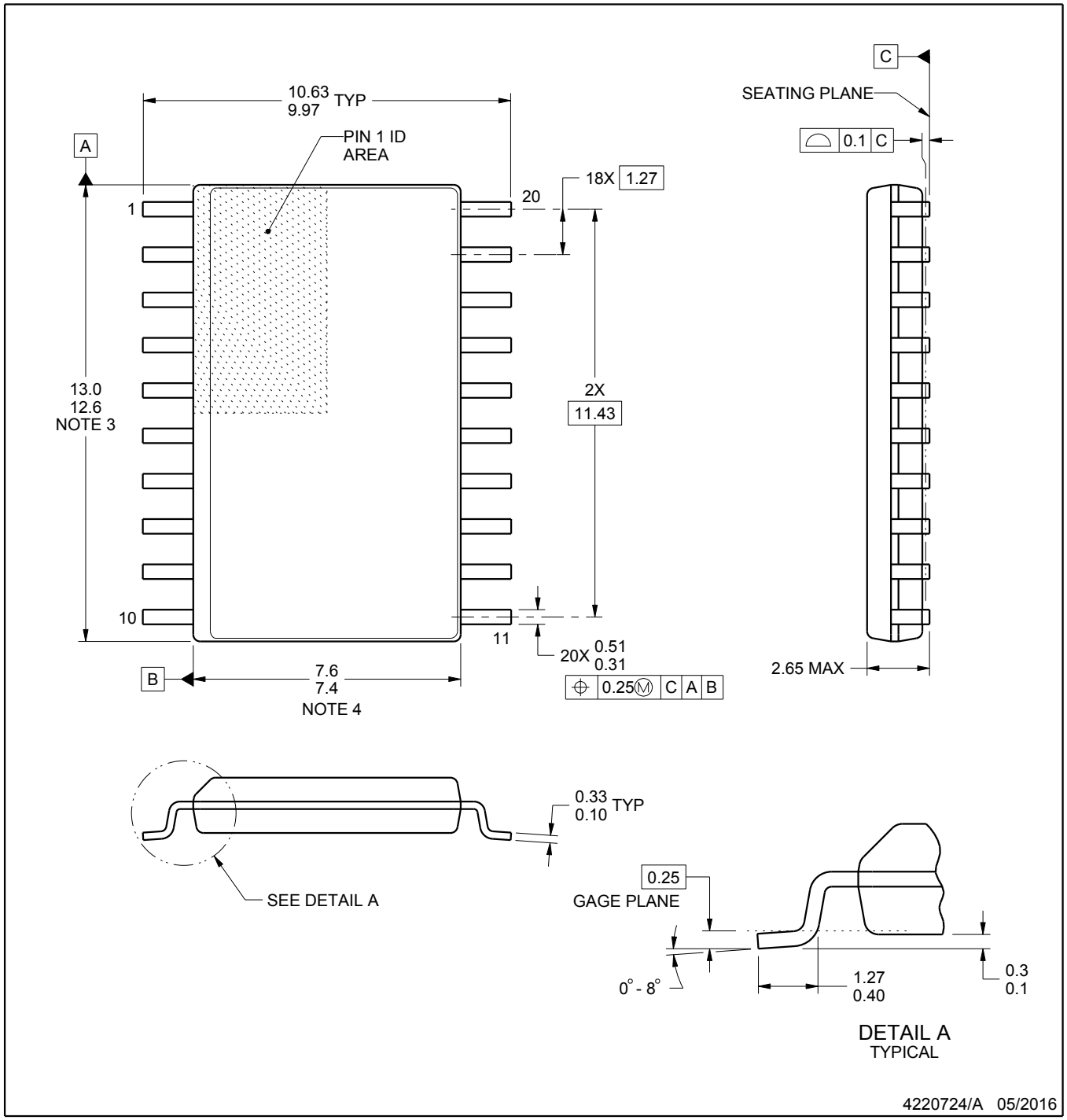


PACKAGE OUTLINE

DW0020A

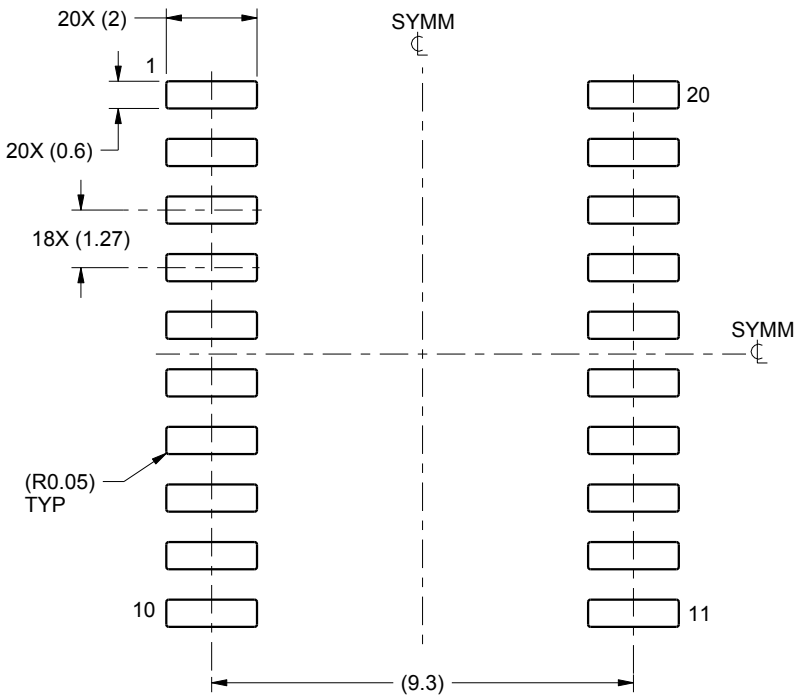
SOIC - 2.65 mm max height

SOIC

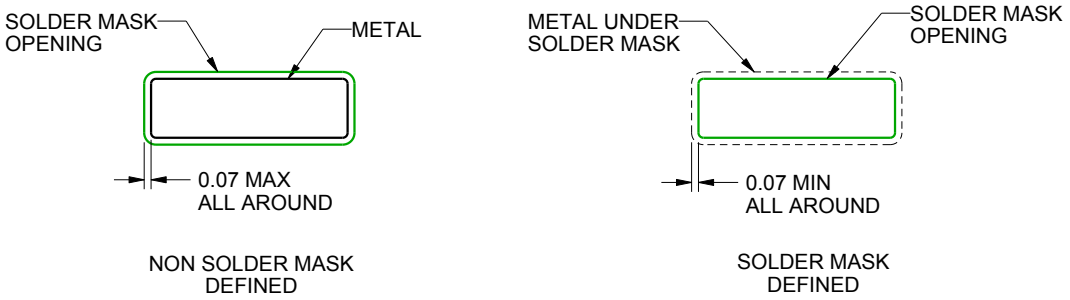


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

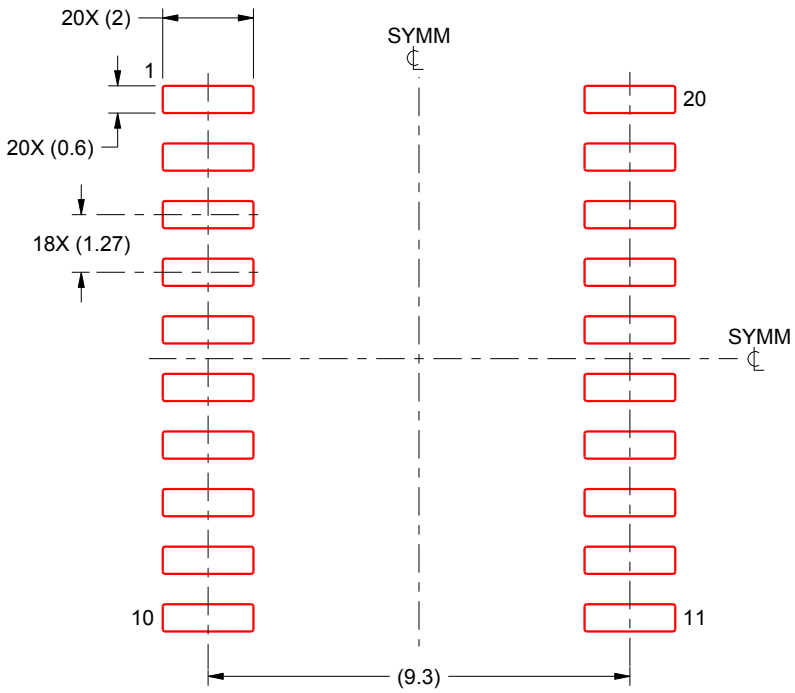


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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