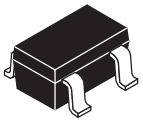


Actual Size
(3,00 mm x 3,00 mm)

LOW INPUT VOLTAGE, CAP FREE 150 mA LOW-DROPOUT (LDO) LINEAR REGULATOR

FEATURES

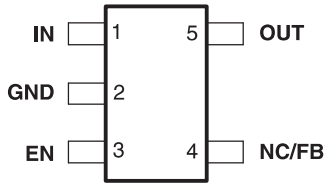
- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **150 mA Low-Dropout (LDO)**
- **Available in 1.8 V Fixed-Output Version**
- **Low Input Voltage Requirement (Down to 1.8 V)**
- **Small Output Capacitor, 0.1 μF**
- **Dropout Voltage Typically 200 mV at 150 mA**
- **Less Than 3μA Quiescent Current in Shutdown Mode**
- **Thermal Protection**
- **Over Current Limitation**
- **5-Pin SOT-23 (DBV) Package**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Portable Communication Devices**
- **Battery-Powered Equipment**
- **PCMCIA Cards**
- **Personal Digital Assistants**
- **Modems**
- **Bar Code Scanners**
- **Backup Power Supplies**
- **SMPS Post Regulation**
- **Internet Audio**

DBV PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TPS72118 family of LDO regulators is available in fixed voltage options that are commonly used to power the latest DSPs and microcontrollers with a fixed output to 1.8 V. These regulators can be used in a wide variety of applications ranging from portable, battery-powered equipment to PC peripherals. The family features operation over a wide range of input voltages (1.8 V to 5.5 V) and low dropout voltage (150 mV at full load). Therefore, compared to many other regulators that require 2.5 V or higher input voltages for operation, these regulators can be operated directly from two AAA batteries. Also, the typical quiescent current (ground pin current) is low, starting at 85 μA during normal operation and 3 μA in shutdown mode. These regulators can be operated very efficiently and, in a battery-powered application, help extend the longevity of the device.

Similar LDO regulators require 1 μF or larger output capacitors for stability. However, this regulator uses an internal compensation scheme that stabilizes the feedback loop over the full range of input voltages and load currents with output capacitances as low as 0.1 μF. Ceramic capacitors of this size are relatively inexpensive and available in small footprints.

This family of regulators is particularly suited as a portable power supply solution due to its minimal board space requirement and 1.8 V minimum input voltage. Being able to use two off-the-shelf AAA batteries makes system design easier and also reduces component cost. Moreover, the solution is more efficient than if a regulator with a higher input voltage is used.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	VOLTAGE	PACKAGE(2)	PART NUMBER	SYMBOL
–55°C to 125°C	1.8 V	DBV	TPS72118MDBVREP(3)	CKZ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The DBVR indicates tape and reel of 3000 parts.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

	TPS72118
Voltage range at IN	–0.3 V to 7 V
Voltage range at EN	–0.3 V to 7 V
Voltage on OUT, FB, NC	–0.3 V to V_I + 0.3 V
Peak output current	Internally limited
ESD rating, HBM	3 kV
Continuous total power dissipation	See Dissipation Rating Table
Operating junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.
(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATING

BOARD	PACKAGE	$R_{\Theta JC}$	$R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low-K(1)	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High-K(2)	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C	555 mW	305 mW	222 mW

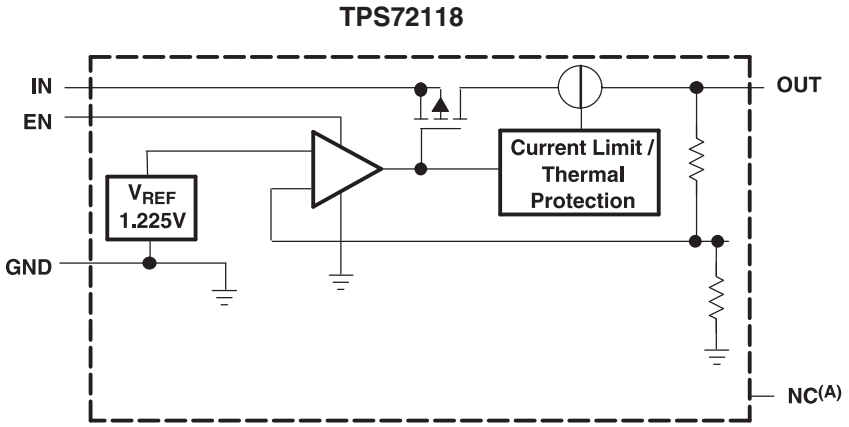
(1) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch x 3 inch, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range $V_{IN} = V_{OUT(Nom)} + 1$ V, $I_{OUT} = 1$ mA, EN = V_{IN}, $C_{OUT} = 1$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)			1.8		5.5	V
I_{OUT}	Continuous output current			0		150	mA
T_J	Operating junction temperature			–55		125	°C
V_{OUT}	Output voltage	T_J = 25°C	1mA < I_{OUT} < 150 mA 2.8 V ≤ V_{IN} ≤ 5.5 V		1.8		V
		T_J = Full Temp		1.728		1.872	
$I_{(Q)}$	Quiescent current (GND current)	I_{OUT} = 1 mA	T_J = 25°C		85		µA
		I_{OUT} = 1 mA	T_J = Full Temp			125	
		I_{OUT} = 150 mA	T_J = 25°C		570		
		I_{OUT} = 150 mA	T_J = Full Temp			850	
	Standby current	EN < 0.5 V	T_J = 25°C		0.01		µA
		EN < 0.5 V	T_J = Full Temp			3	
V_{ref}	Reference voltage	T_J = 25°C			1.225		V
PSRR	Ripple rejection	f = 100 Hz, C_O = 10 µF, I_{OUT} = 150 mA	T_J = 25°C (1)		48		dB
	Current limit	See (2)		120		525	mA
	Output voltage line regulation ($\Delta V_{OUT}/V_{OUT}$)(1)	V_O + 1 V < V_{IN}≤ 5.5 V, I_{OUT} = 150 mA	T_J = 25°C		0.03	0.20	%/V
			T_J = Full Temp			0.35	
	Output voltage load regulation	0 < I_{OUT} < 150 mA	T_J = 25°C		1.5		mV
V_{IH}	EN high level input			1.4			V
V_{IL}	EN low level input					0.4	
I_I	EN input current	EN = 0 V			–0.01		µA
		EN = IN			–0.01		
V_{DO}	Dropout voltage(3)	I_{OUT} = 150 mA	T_J = 25°C		150		mV
	Thermal shutdown temperature				170		°C
	Thermal shutdown hysteresis				20		°C

(1) Minimum IN operating voltage is 1.8 V or $V_{OUT} + V_{DO}$, whichever is greater.
(2) Test condition includes output voltage V_O = 1 V and pulse duration = 10 ms.
(3) Dropout voltage is defined as the differential voltage between V_O and V_I when V_O drops 100 mV below the value measured with $V_{IN} = V_{OUT} + V_{DO}$.



A. This pin must be left floating and not connected to GND.

Figure 1. Functional Block Diagram—Fixed Version

Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
GND	2	Ground
EN	3	Enable input
IN	1	Input supply voltage
NC/FB	4	NC = Not connected (see (A)); FB = Feedback (adjustable option TPS72101)
OUT	5	Regulated output voltage

TYPICAL CHARACTERISTICS

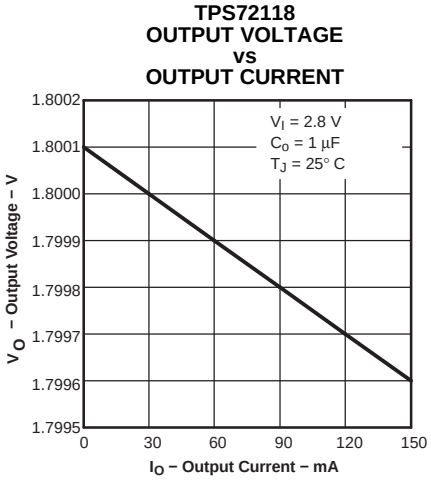


Figure 2.

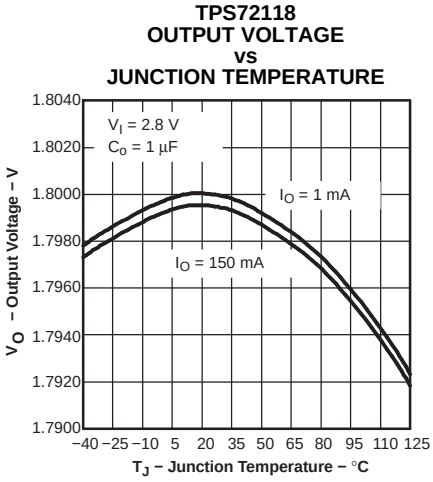


Figure 3.

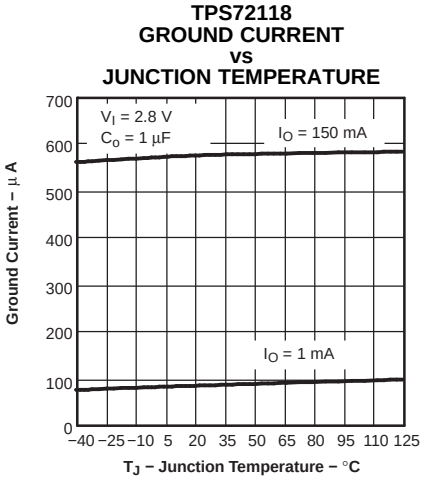


Figure 4.

TYPICAL CHARACTERISTICS (continued)

TPS72118
GROUND CURRENT
vs
OUTPUT CURRENT

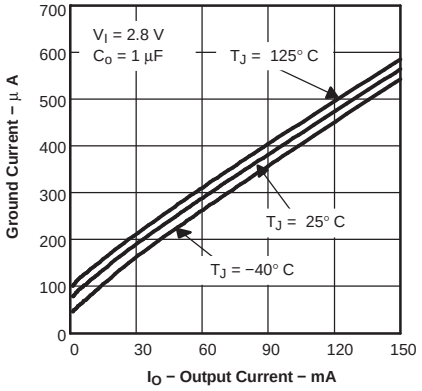


Figure 5.

TPS72118
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

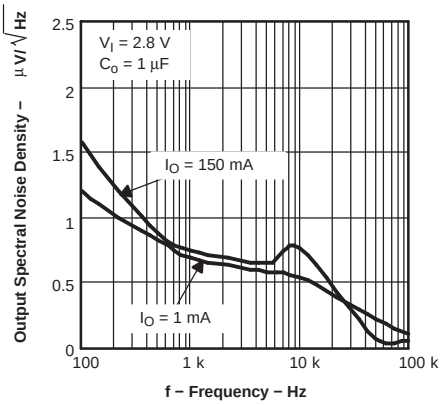


Figure 6.

TPS72118
OUTPUT IMPEDANCE
vs
FREQUENCY

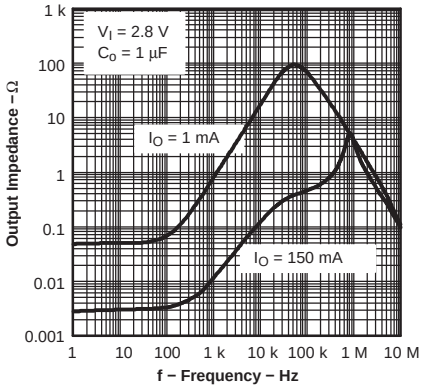


Figure 7.

TPS72118
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

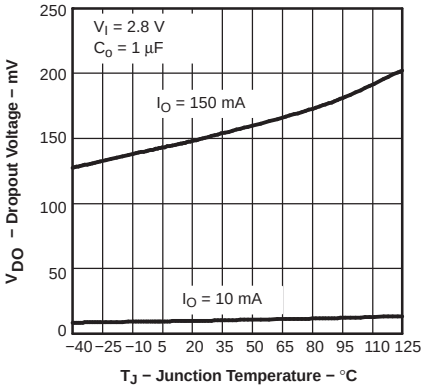


Figure 8.

TPS72118
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

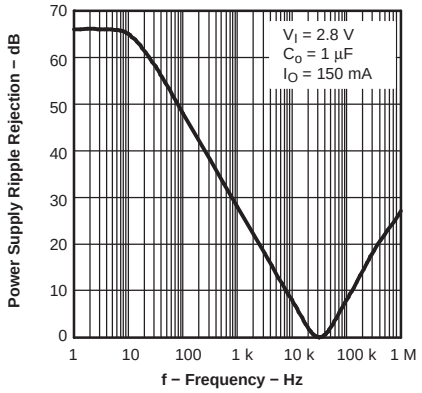


Figure 9.

TPS72118
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

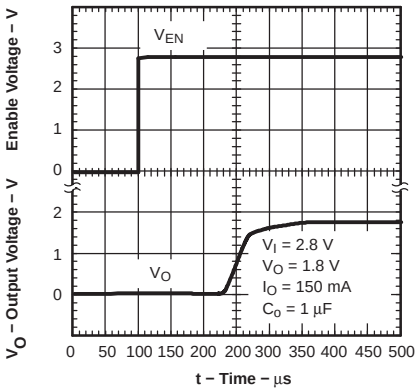


Figure 10.

TPS72118
LINE TRANSIENT RESPONSE

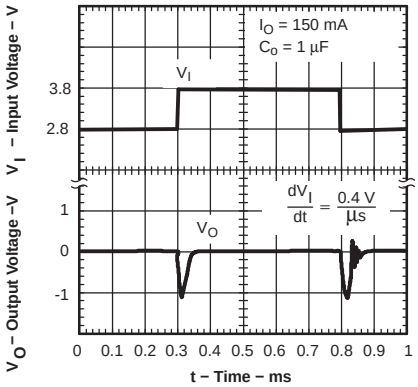


Figure 11.

TPS72118
LOAD TRANSIENT RESPONSE

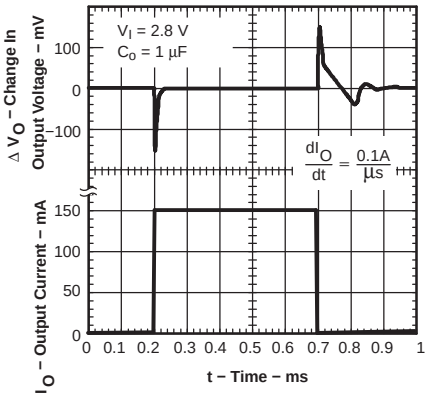


Figure 12.

POWER UP / POWER DOWN

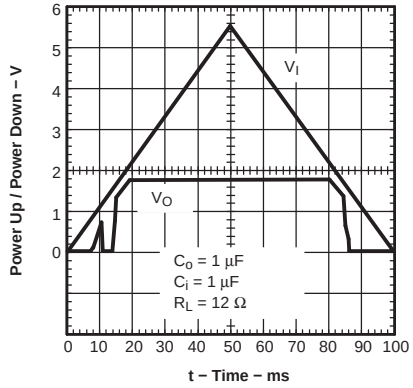


Figure 13.

TYPICAL CHARACTERISTICS (continued)

DC DROPOUT VOLTAGE vs OUTPUT CURRENT

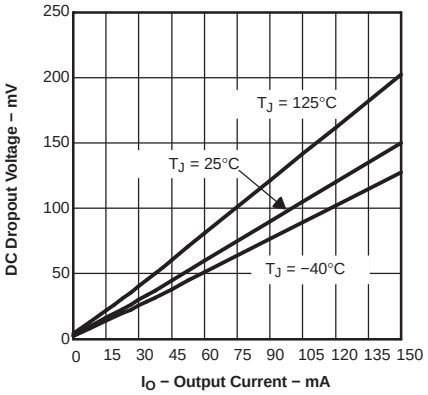


Figure 14.

TPS72101 DROPOUT VOLTAGE vs INPUT VOLTAGE

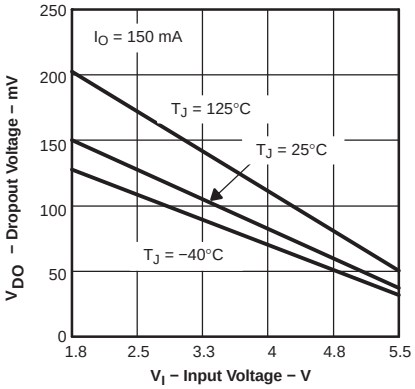


Figure 15.

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

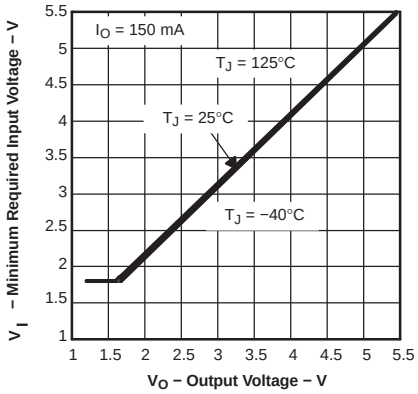


Figure 16.

APPLICATION INFORMATION

The TPS72118 family of low-dropout (LDO) regulators functions with a very low input voltage (>1.8 V). The dropout voltage is typically 150 mV at full load. Typical quiescent current (ground pin current) is only 85 μA and drops to 3 μA in the shutdown mode.

DEVICE OPERATION

The TPS72118 family can be operated at low input voltages due to low voltage circuit design techniques and a PMOS pass element that exhibits low dropout.

A logic low on the enable input, EN, shuts off the output and reduces the supply current to less than 3 μA. EN may be tied to V_{IN} in applications where the shutdown feature is not used.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 170°C. Recovery is automatic when the junction temperature drops approximately 20°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A typical application circuit is shown in Figure 17.

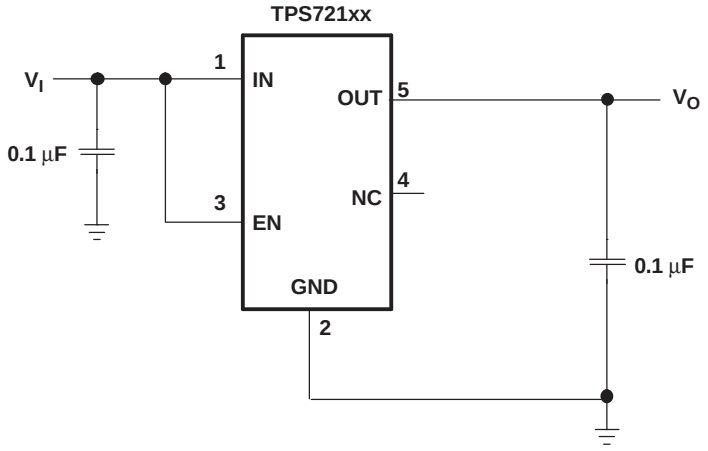


Figure 17. Typical Application Circuit

DUAL SUPPLY APPLICATION

In portable, battery-powered electronics, separate power rails for the DSP or microcontroller core voltage, $V_{(CORE)}$, and I/O peripherals (V_{IO}) are usually necessary. The TPS72118 family of LDO linear regulators is ideal for providing $V_{(CORE)}$ for the DSP or microcontroller. As shown in Figure 18, two AAA batteries provide an input voltage to a boost converter. The batteries combine input voltage ranges from 3.0 V down to 1.8 V near the end of their useful lives. Therefore, a boost converter is necessary to provide the typical 3.3 V needed for V_{IO}. Although there is no explicit circuitry to perform power-up sequencing of first $V_{(CORE)}$ then V_{IO}, the output of the linear regulator reaches its regulated voltage much faster (< 400 μs) than the output of any switching type boost converter due to the inherent slow start up of those types of converters. Assuming a boost converter with minimum V_I of 1.8 V is appropriately chosen, this power supply solution can be used over the entire life of the two off-the-shelf AAA batteries. Thus, this solution is very efficient and the design time and overall cost of the solution is minimized.

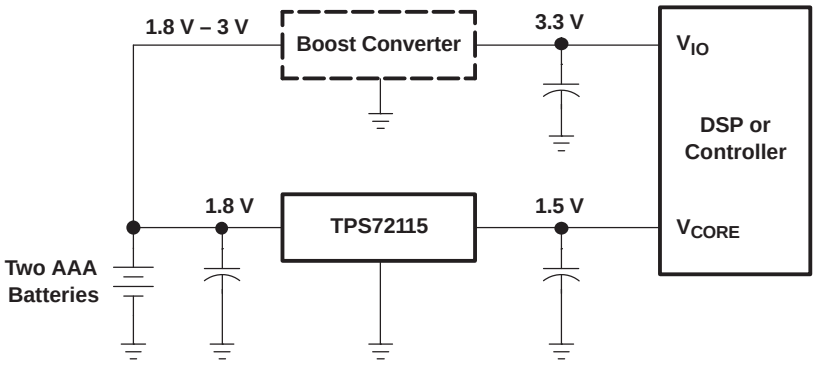


Figure 18. Dual Supply Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

A 0.1-µF ceramic bypass capacitor is required on both the input and output for stability. Larger capacitors improve transient response, noise rejection, and ripple rejection. A higher value electrolytic input capacitor may be necessary if large, fast rise time load transient are anticipated, and/or there is significant input resistance from the device to the input power supply.

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is ensured to a junction temperature of 125°C; the maximum junction temperature allowable without damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using Equation 1 :

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package; see the package dissipation rating table.
- T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 2:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

REGULATOR PROTECTION

The TPS72118 pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS72118 also features internal current limiting and thermal protection. During normal operation, the TPS72118 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 170°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 150°C, regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72118MDBVREP	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKZ	Samples
V62/07636-01XE	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS72118-EP :

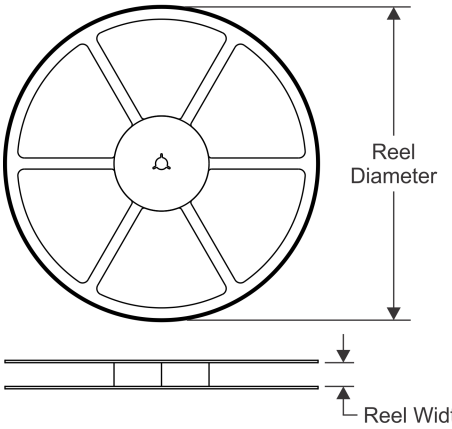
- Catalog: TPS72118

NOTE: Qualified Version Definitions:

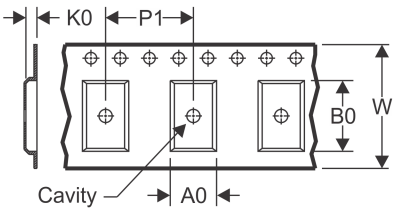
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

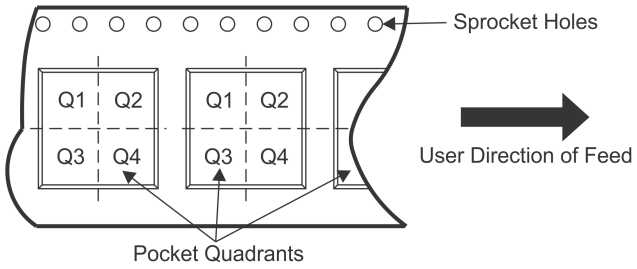


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

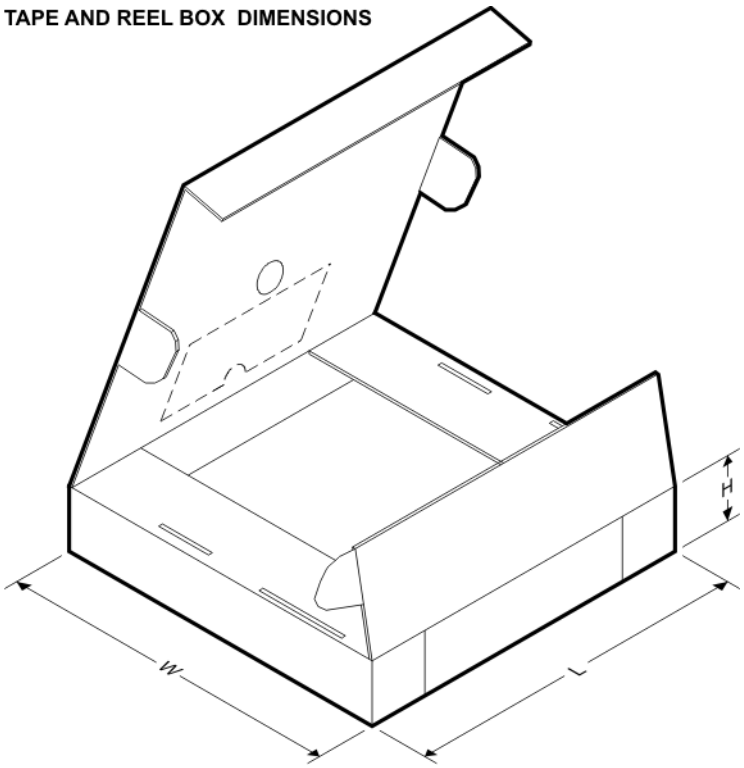
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72118MDBVREP	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

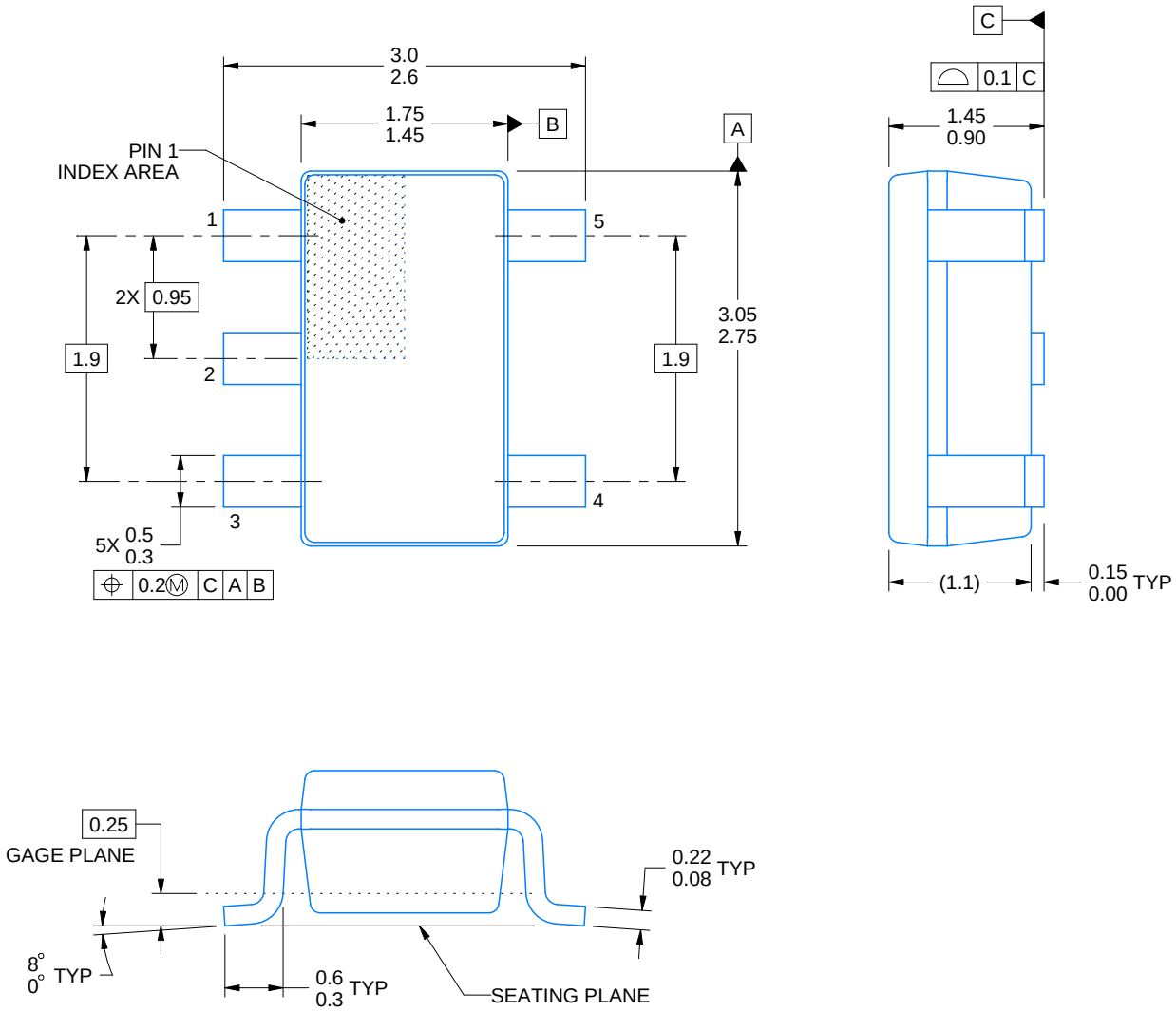
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72118MDBVREP	SOT-23	DBV	5	3000	203.0	203.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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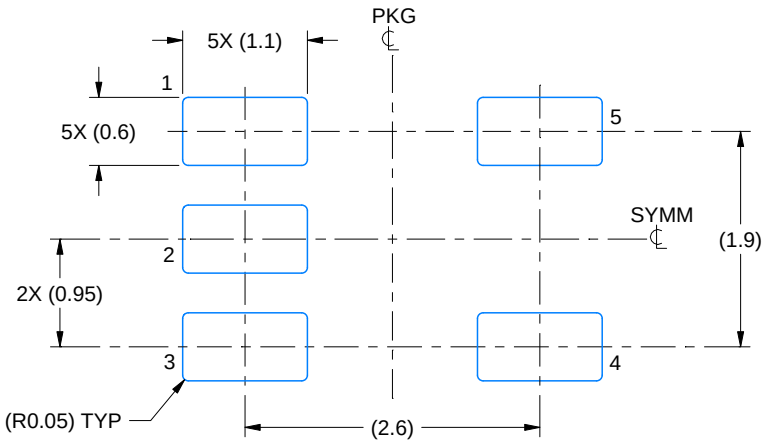
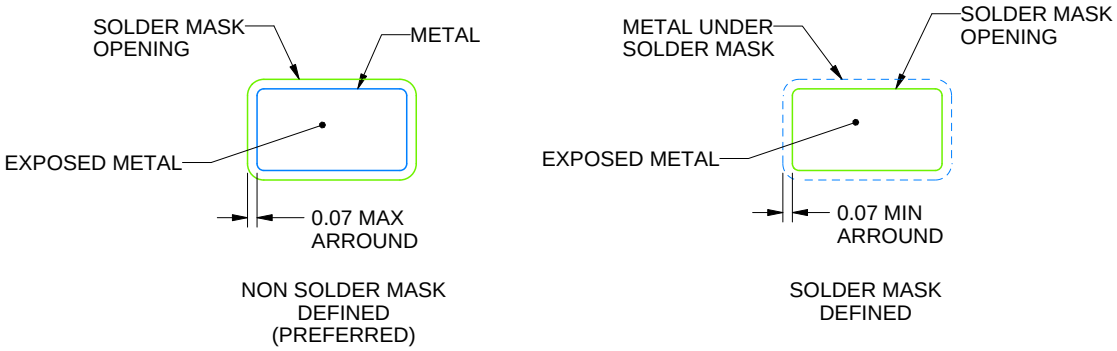
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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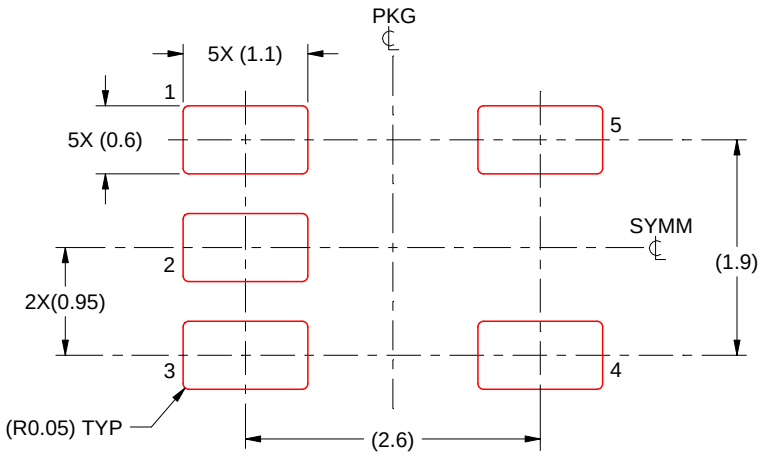
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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