

VBL1154N Datasheet

N-Channel 150V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
150	0.035 at $V_{GS} = 10$ V	45
	0.042 at $V_{GS} = 7.5$ V	42

FEATURES

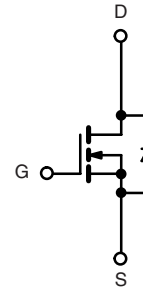
- TrenchFET[®] Power MOSFETs
- 175 °C Junction Temperature
- New Low Thermal Resistance Package
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT

APPLICATIONS

- Primary Side Switch

TO-263



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	45	A
		31	
Pulsed Drain Current	I_{DM}	140	
Avalanche Current	I_{AR}	50	mJ
Repetitive Avalanche Energy ^a	E_{AR}	80	
Maximum Power Dissipation ^a	P_D	160 ^b	W
		3.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount TO-263 ^c)	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.9	

Notes:

a. Duty cycle ≤ 1 %.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{DS} = 0 V, I _D = 250 μA	150			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	4		6	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 150 V, V _{GS} = 0 V			1	μA
		V _{DS} = 120 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 120 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	80			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		0.035		Ω
		V _{GS} = 7.5 V, I _D = 10 A		0.042		
		V _{GS} = 10 V, I _D = 15 A, T _J = 125 °C		0.060		
		V _{GS} = 10 V, I _D = 15 A, T _J = 175 °C		0.080		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A	10			S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		2200		pF
Output Capacitance	C _{oss}			290		
Reverse Transfer Capacitance	C _{rss}			190		
Gate Resistance	R _g			2		Ω
Total Gate Charge ^c	Q _g	V _{DS} = 75 V, V _{GS} = 10 V, I _D = 40 A		38	60	nC
Gate-Source Charge ^c	Q _{gs}			13		
Gate-Drain Charge ^c	Q _{gd}			13		
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 75 V, R _L = 1.80 Ω I _D ≅ 40 A, V _{GEN} = 10 V, R _g = 2.5 Ω		15	25	ns
Rise Time ^c	t _r			130	200	
Turn-Off Delay Time ^c	t _{d(off)}			30	45	
Fall Time ^c	t _f			90	140	
Source-Drain Diode Ratings and Characteristics T _C = 25 °C ^b						
Continuous Current	I _S				40	A
Pulsed Current	I _{SM}				80	
Forward Voltage ^a	V _{SD}	I _F = 40 A, V _{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 40 A, dI/dt = 100 A/μs		100	150	ns
Peak Reverse Recovery Current	I _{RM(REC)}			5	8	A
Reverse Recovery Charge	Q _{rr}				0.25	0.6

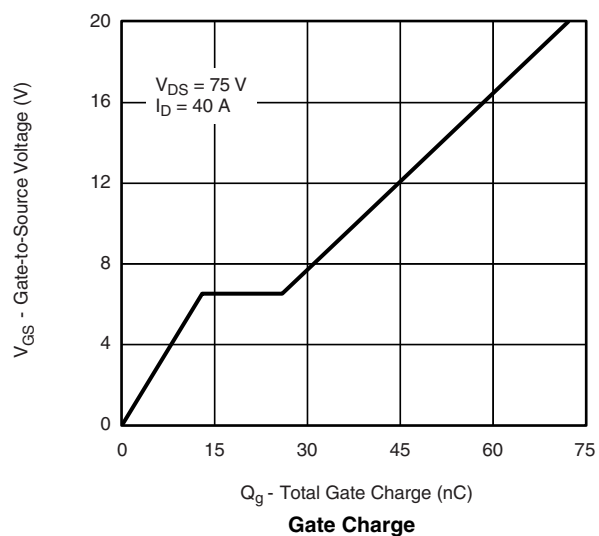
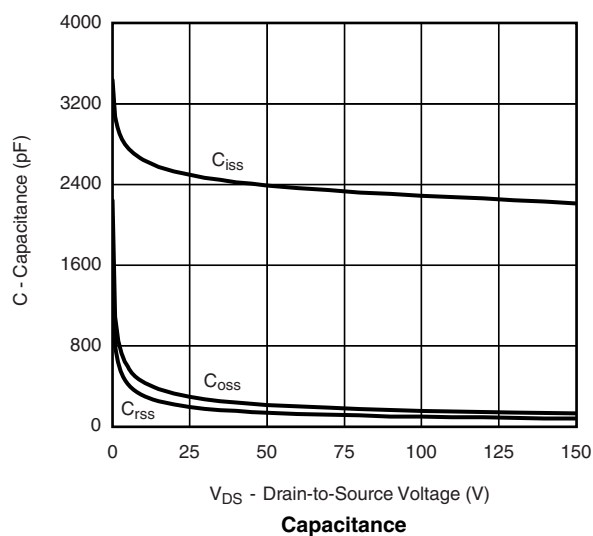
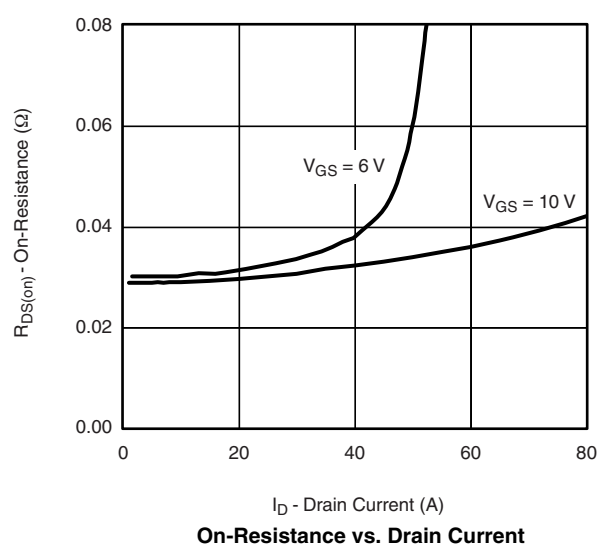
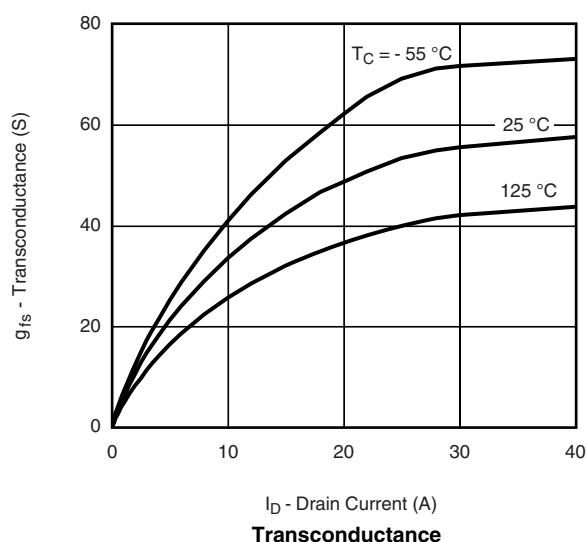
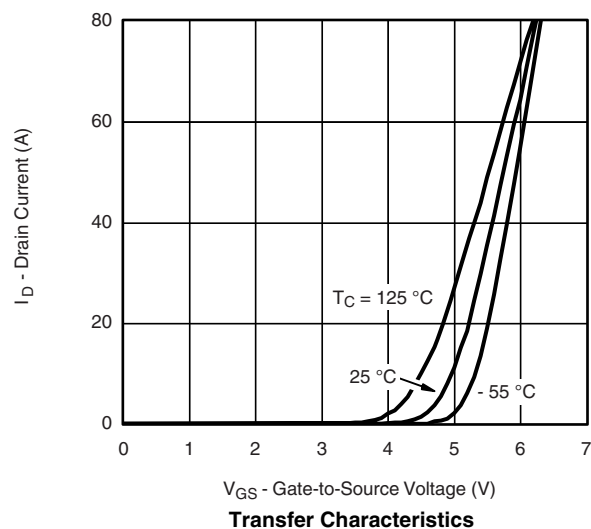
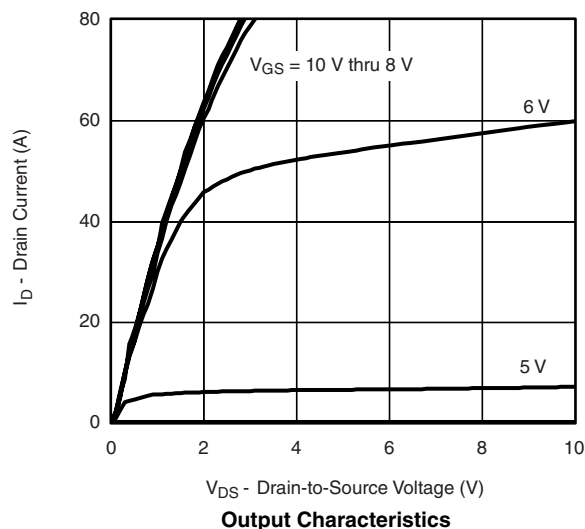
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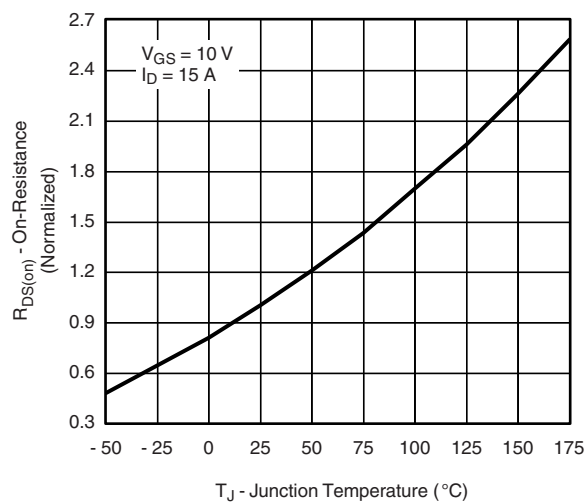
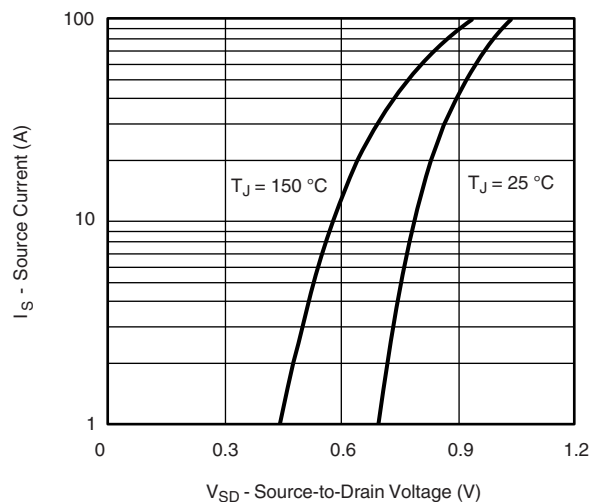
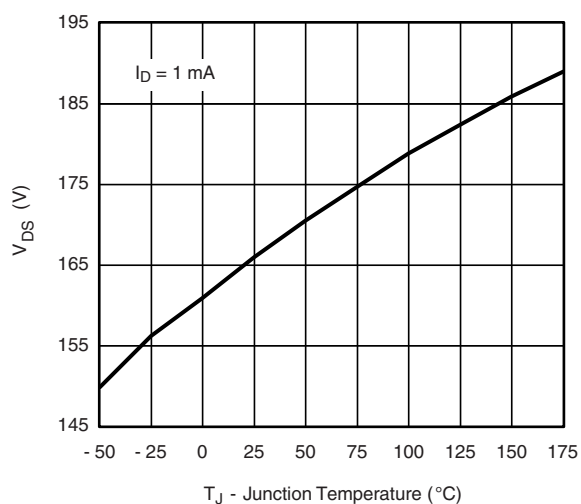
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

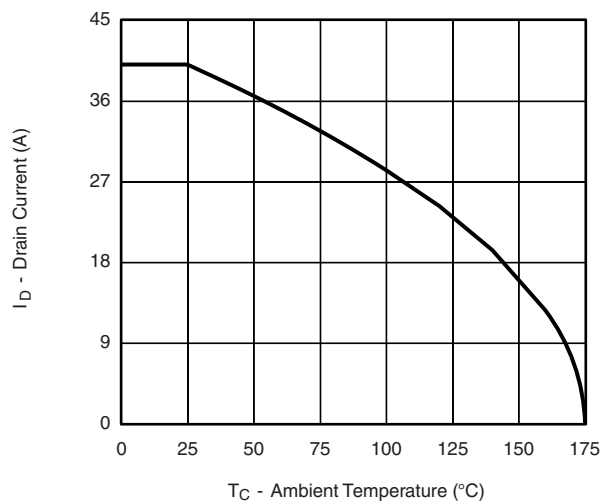
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

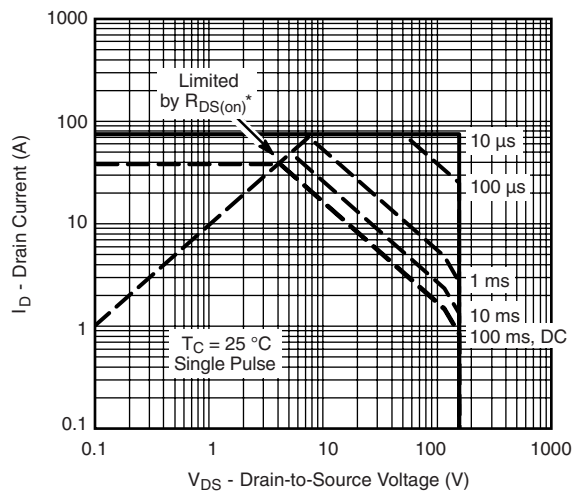
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

**Drain Source Breakdown
vs. Junction Temperature**

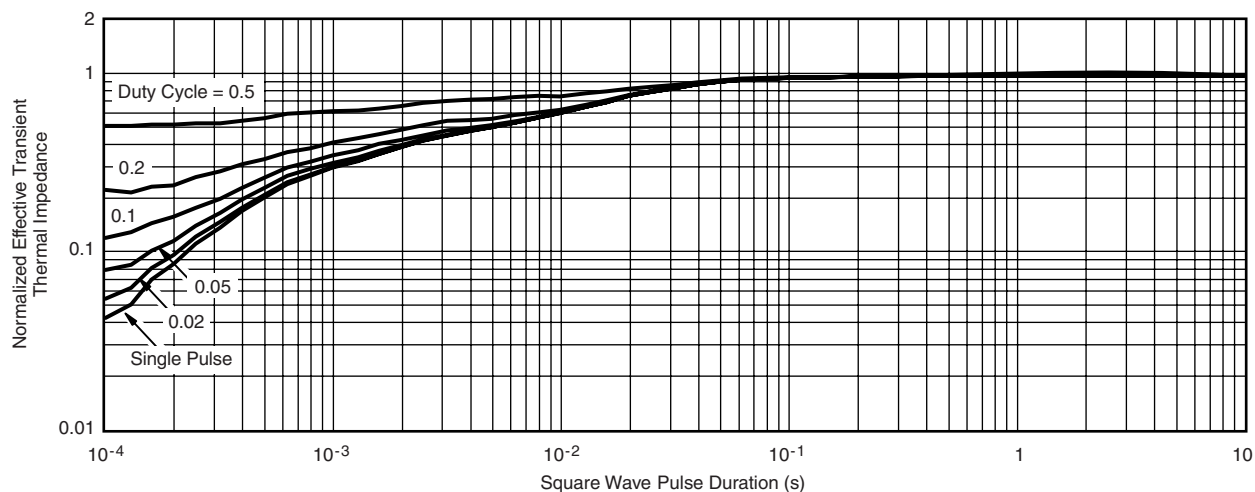
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature

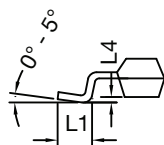
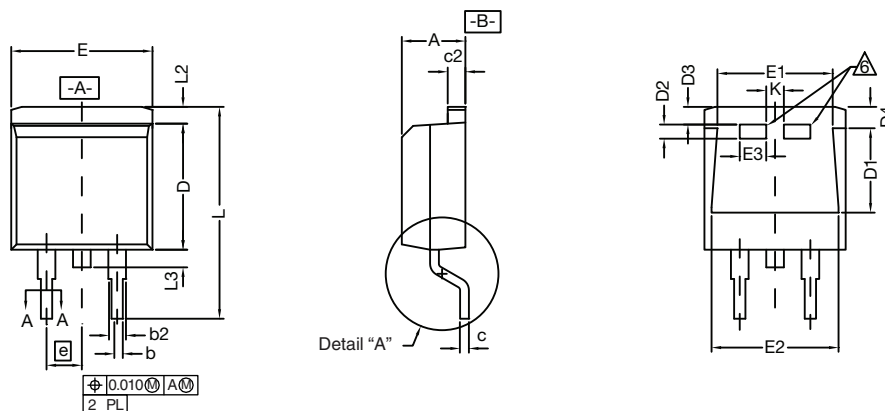


Safe Operating Area
 * $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

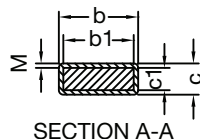


Normalized Thermal Transient Impedance, Junction-to-Case

TO-263 (D²PAK): 3-LEAD



DETAIL A (ROTATED 90°)

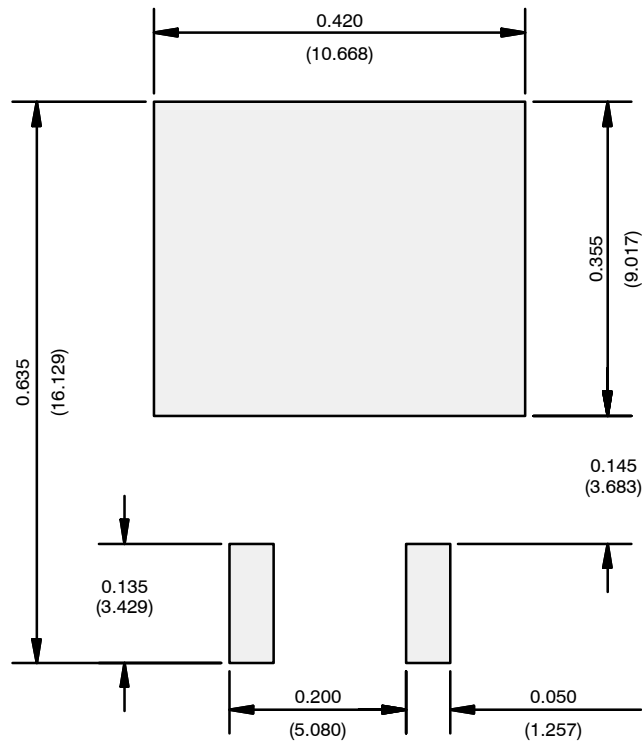


SECTION A-A

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
-  This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

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