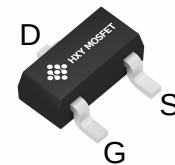


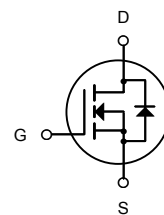


Description

The SI2318CDS-T1-GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOT-23



N-Channel MOSFET

General Features

$V_{DS} = 40V$ $I_D = 5A$
 $R_{DS(ON)} < 38m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)} < 52m\Omega$ @ $V_{GS} = 4.5V$

Application

Battery protection
Load switch
Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
SI2318CDS-T1-GE3	SOT-23	2318	3000

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous ($T_C = 25^\circ C$)	5	A
	Drain Current – Continuous ($T_C = 70^\circ C$)	4.2	A
P_D	Power Dissipation ($T_C = 25^\circ C$)	1.56	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction to ambient	80	$^\circ C/W$



Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics @ T _J = 25℃ (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _A =25℃)	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _A =125℃)	V _{DS} =40V, V _{GS} =0V	--	--	100	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.7	1.9	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance②	V _{GS} =10V, I _D =5A	--	30	38	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance②	V _{GS} =4.5V, I _D =4A	--	36	52	mΩ
Dynamic Electrical Characteristics @ T _J = 25℃ (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	--	340	--	pF
C _{oss}	Output Capacitance		--	60	--	pF
C _{rss}	Reverse Transfer Capacitance		--	30	--	pF
R _g	Gate Resistance	f=1MHz		7.8		Ω
Q _g	Total Gate Charge	V _{DS} =20V I _D =5A, V _{GS} =10V	--	5.8	--	nC
Q _{gs}	Gate Source Charge		--	0.4	--	nC
Q _{gd}	Gate Drain Charge		--	2	--	nC
Switching Characteristics @ T _J = 25℃ (unless otherwise stated)						
t _{d(on)}	Turn on Delay Time	V _{DD} =20V, I _D =3.5A, R _G =1Ω, V _{GS} =4.5V	--	4.1	--	ns
t _r	Turn on Rise Time		--	11.6	--	ns
t _{d(off)}	Turn Off Delay Time		-	24	--	ns
t _f	Turn Off Fall Time		--	7.6	--	ns
Source Drain Diode Characteristics @ T _J = 25℃ (unless otherwise stated)						
I _{SD}	Source drain current(Body Diode)	T _A =25℃	--	--	1.75	A
V _{SD}	Forward on voltage②	T _J =25℃, I _{SD} =3.5A, V _{GS} =0V	--	0.79	1.2	V

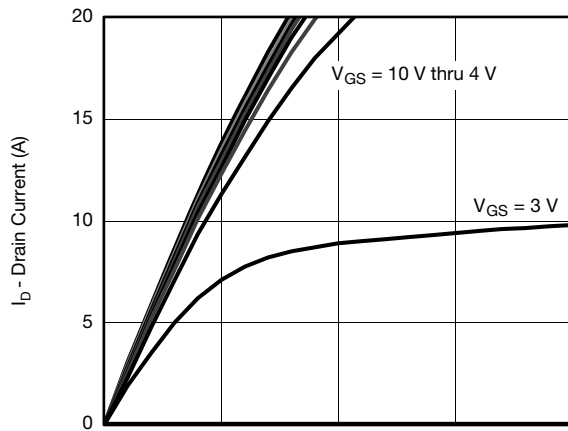
Notes:

① Pulse width limited by maximum allowable junction temperature

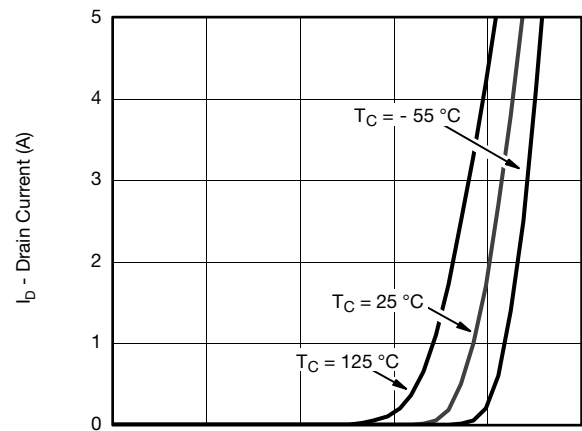
②Pulse test ; Pulse width≤300μs, duty cycle≤2%.



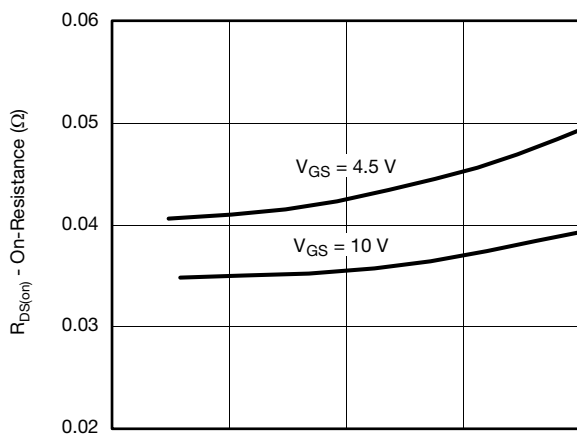
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



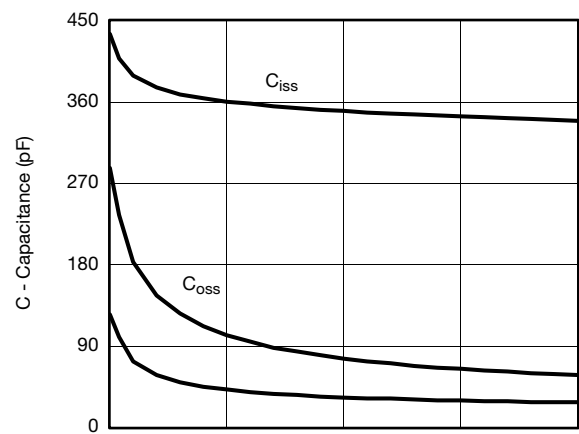
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



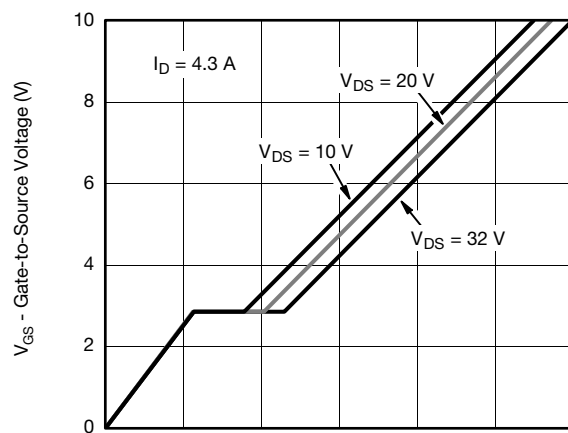
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



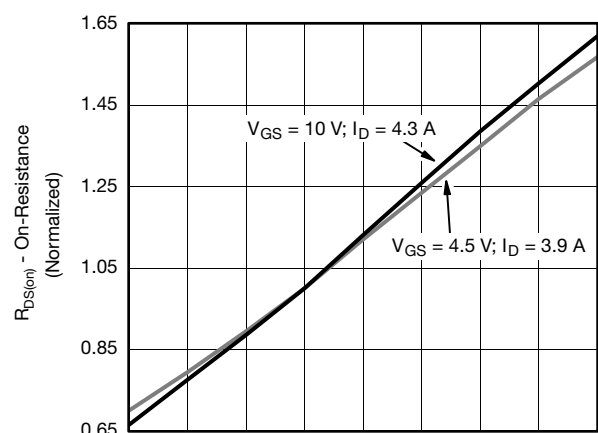
I_D - Drain Current (A)
On-Resistance vs. Drain Current and Gate Voltage



V_{DS} - Drain-to-Source Voltage (V)
Capacitance



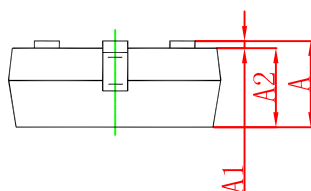
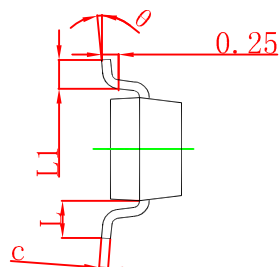
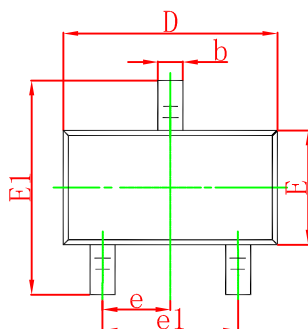
Q_g - Total Gate Charge (nC)
Gate Charge



T_J - Junction Temperature ($^{\circ}\text{C}$)
On-Resistance vs. Junction Temperature

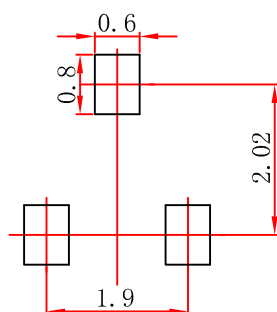


SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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