Dual Channel Digital Audio System with EQ and Frequency DRC Control

General Description

The RT9119 is a high efficiency, I^2S-input, stereo channel audio power amplifier delivering 2x20W into 8Ω BTL speaker loads. It can deliver over 90% power efficiency and eliminate the need for heat-sink.

The built-in anti-pop functions can reduce the speaker's pop noise under all kind of scenarios. Built-in protection circuits can provide over-temperature, over-current, over-voltage, DC and under-voltage protections and report error status.

The RT9119 is an I^2S device receiving all clocks from external sources. It can support both master and slave mode with wide input sampling rate from 8kHz to 96kHz. A fully programmable data path routes these channels to the internal speaker drivers.

The RT9119 features three band DRC and flexible multi-band biquads for anti-clipping, power limiting, and speaker equalization.

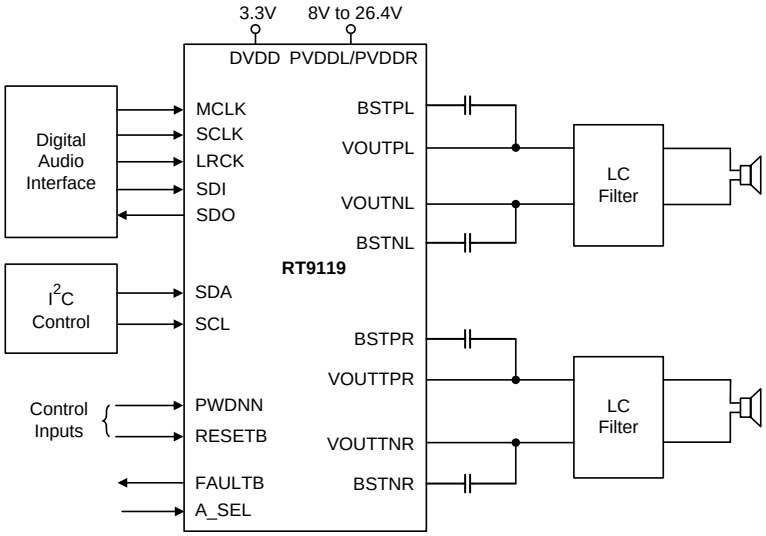
Features

- **Wide Input Supply Range : 8V to 26.4V**
- **2x20W at into 8Ω BTL at 20V**
- **2x9W at into 8Ω BTL at 12V**
- **Support Stereo Channels Output**
- **Sampling Frequency from 8kHz to 96kHz**
- **Built-In Anti-Pop Function for BTL BD Modulations**
- **36 Programmable Biquads for Speaker Equalization**
- **Programmable Coefficients for DRC Filters and Supporting Multi-Compression Ratios**
- **Built-In DC Blocking Filters**
- **Protection Features : UVLO, OVP, OCP, OTP and DCP**
- **Filter-Less Application**
- **VQFN-28L Thermally-Enhanced Package**
- **RoHS Compliant and Halogen Free**

Applications

- LCD-TV
- Monitors
- Home Audio
- Amusement Equipment
- Electronic Music Equipment

Simplified Application Circuit



Ordering Information

RT9119 □□

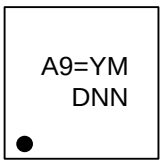
- Package Type
  QV : VQFN-28L 4x5 (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

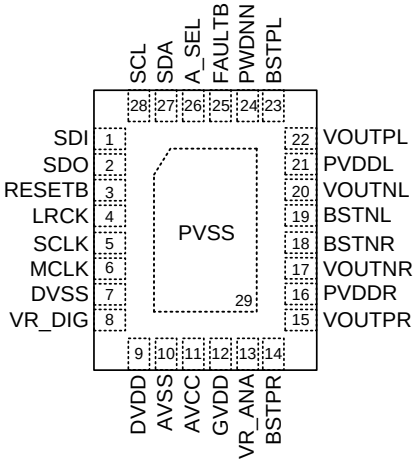
Marking Information



A9= : Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



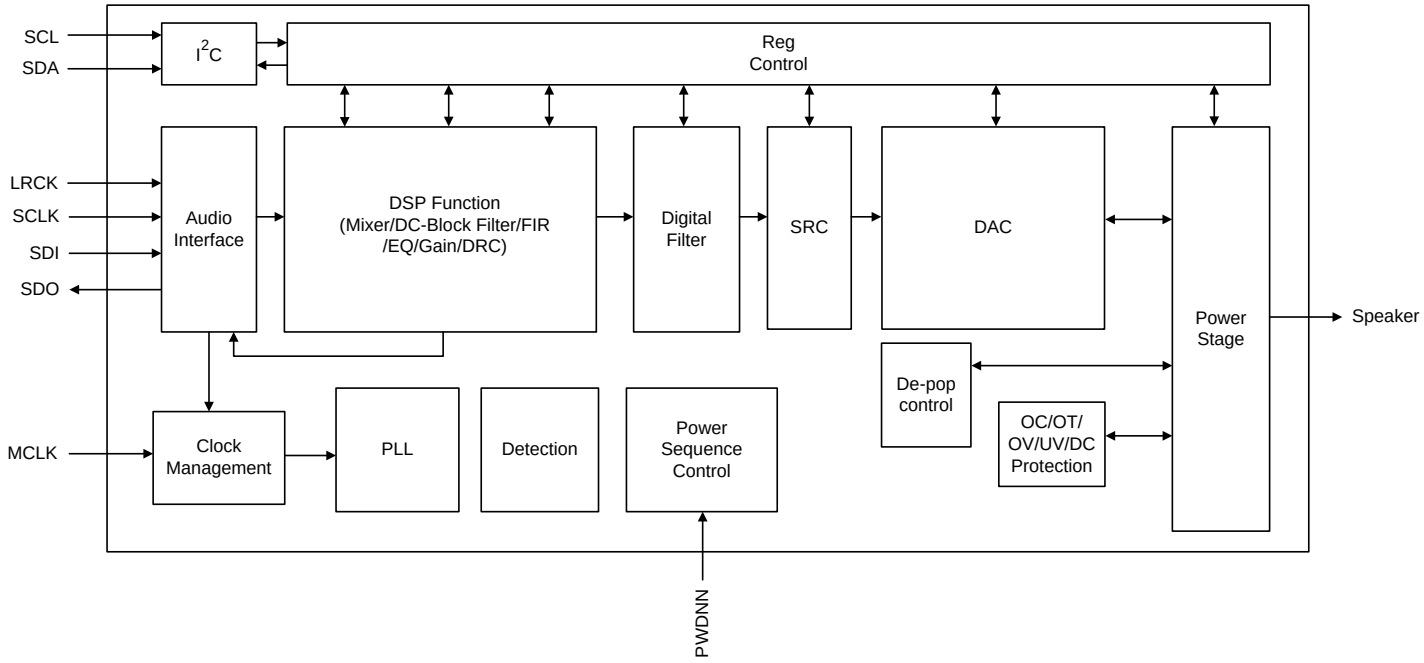
VQFN-28L 4x5

Functional Pin Description

Pin No.	Pin Name	IO	Pin Function
1	SDI	DI	I^2S data input.
2	SDO	DO	I^2S data output.
3	RESETB	DI	Reset, low active.
4	LRCK	DI	I^2S L/R clock input.
5	SCLK	DI	I^2S bit clock input.
6	MCLK	DI	Master clock input.
7	DVSS	P	Ground for digital circuits.
8	VR_DIG	P	1.8V digital supply voltage generated by internal LDO.
9	DVDD	P	3.3V power supply for I/O and HP.
10	AVSS	P	Ground for analog circuits.
11	AVCC	P	26.4V power supply for analog circuits.
12	GVDD	P	Internal power supply generated by LDO.
13	VR_ANA	P	Analog reference voltage.
14	BSTPR	P	Bootstrap supply for VOUTPR.
15	VOUTPR	AO	Positive output of RCH.
16	PVDDR	P	26.4V power supply for RCH.
17	VOUTNR	AO	Negative output of RCH.
18	BSTNR	P	Bootstrap supply of VOUTNR.

Pin No.	Pin Name	IO	Pin Function
19	BSTNL	P	Bootstrap supply of VOUTNL.
20	VOUTNL	AO	Negative output of LCH.
21	PVDDL	P	26.4V power supply for LCH.
22	VOUTPL	AO	Positive output of LCH.
23	BSTPL	P	Bootstrap supply for VOUTPL.
24	PWDNN	DI	Power down pin, low active.
25	FAULTB	DO	Fault indicator (low active).
26	A_SEL	DI	Slave address selection.
27	SDA	DIO	I^2C data input/output.
28	SCL	DI	I^2C clock input.
29 (Exposed Pad)	PVSS	P	Ground.

Functional Block Diagram



Operation

Error Reporting

The FAULTB pin is error report output pin. Any fault will pull FAULTB to low. This pin is open-drain configuration, need pull-up resistor.

Clock Detection

The RT9119 can accept SCLK to be as 32fs, 48fs and 64fs and support only a 1xfs LRCK. The internal oscillator will check MCLK or SCLK input constantly. If clock is lost, the RT9119 will mute and shutdown the power stage automatically.

Volume Control

The RT9119 have master volume MS_VOL and each channel volume CH1_VOL, CH2_VOL control. The step of each volume is 0.0625dB per step, from 24dB to mute. CH1 and CH2 also have each mute control, CH1_MUTE and CH2_MUTE.

Built-In Anti-POP Function

An internal soft-start function controls the Duty ramp-up rate of the output PWM voltage to minimize the POP noise during start-up. Similarly, when power shut-down, the duty also ramp-down to eliminate the POP noise. This function also acts when the PWDNN pin turns-ON/OFF.

Over-Current Protection

The RT9119 provides OCP function to prevent the device from damages during overload or short-circuit conditions. The current are detected by an internal sensing circuit. Once overload happens, the OCP function is designed to operate in auto-recovery mode by default. Or can choose the latch mode.

Under-Voltage Protection

The RT9119 monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin falls below the under-voltage threshold, 6.5V (typ.), the UVP circuit turns off the output immediately. Or the latch mode can be configured to use.

Over-Voltage Protection

The RT9119 monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin rise behind the over-voltage threshold, 30V, the OVP circuit turns off the output immediately and operates in cycle by cycle auto-recovery mode. Or the latch mode can be configured to use.

Over-Temperature Protection

The over-temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation. Or the latch mode can be configured to use.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, AVCC, PVDDL, PVDDR ---------- –0.3V to 32V
- Supply Voltage, DVDD ---------- –0.3V to 9V
- Speaker Amplifier Output Voltage, VOUTXX ---------- –0.3V to 32V
- BSTXX to PVSS DC ---------- –0.3V to 36V
- SCL, SDA, FAULTB ---------- –0.3V to 6V
- LRCK, SCLK, SDI, MCLK, PWDNN, A_SEL, RESETB ---------- –0.3V to DVDD + 0.3V
- GND to PVSS, DVSS and AVSS ---------- –0.3V to 0.3V
- VOUTPR, VOUTNR, VOUTPL, VOUTNL ---------- –10V to 37V (Note 5)
- SDO ---------- –0.3V to 9V
- VR_DIG ---------- –0.3V to 4V
- VRANA, GVDD ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  VQFN-28L 4x5 ---------- 3.64W
- Package Thermal Resistance (Note 2)

  VQFN-28L 4x5, θ_{JA} ---------- 27.4°C/W

  VQFN-28L 4x5, θ_{JC} ---------- 1.7°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, DVDD ---------- 3.0V to 3.6V
- Supply Input Voltage, PVDDL, PVDDR, AVCC ---------- 8V to 26.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(PVDD = 12V, DVDD = 3.3V, R_L = 8Ω, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWDNN, A_SEL	VIH : High-Level-Input Voltage	V_{IH}		DVDD x0.7	--	--	V
	VIL : Low-Level-Input Voltage	V_{IL}		--	--	DVDD x0.3	
FAULTB	VOL : Low-Level-Output Voltage	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DVDD Quiescent Current (Normal Mode)	I_{Q_D}	PWDNN = 3.3V, 0dBFS input, for DVDD, no load, no LC filter		--	15	25	mA
		PWDNN = 3.3V, switch 50% duty for DVDD, no load, no LC filter		--	12	20	
DVDD Shutdown Current	I_{SD_D}	PWDNN = 0.8V, for DVDD, no load, no LC filter		--	--	1	mA
PVDD Quiescent Current (Normal Mode)	I_{Q_P}	PWDNN = 3.3V,switch 50% duty for PVDD, no load, no LC filter		--	25	40	mA
PVDD Shutdown Current	I_{SD_P}	PWDNN = 0.8V,no load for PVDD, no load, no LC filter		--	--	2	mA
Drain-Source On-State Resistance	$R_{DS(ON)}$	PVDD = 12V, I_O = 500mA, T_J = 25°C	High side	110	150	185	mΩ
			Low side	100	130	155	
GVDD		1mA		--	5	--	V
VR_ANA				--	5	--	V
Speaker Gain variation	$\Delta A_{V(SPK\_AMP)}$			–0.5	--	0.5	dB
Startup Time from Shutdown	t_{ON}			--	75	--	ms
Shut Down Time from Enable	t_{OFF}			--	60	--	ms
PWM Switching Frequency		400kHz mode		300	--	500	kHz
		800kHz mode		600	--	1000	
RMS Output Power BD Modulation	P_O	THD + N = 10%, (BTL)		8	9	--	W
		THD + N = 1%, (BTL)		--	6.5	--	
		PVCC = 20V, THD + N = 1%, (BTL)		--	20	--	
Total Harmonic Distortion + Noise	THD+N	P_O =1W (BTL)		--	0.03	0.1	%
Output Integrated Noise	Vn	20Hz to 20kHz, A-weighted	4x Gain	--	100	200	μV
			8x Gain	--	120	240	
Output Offset Voltage	V_{OS}		4x Gain	--	--	20	mV
			8x Gain	--	--	35	
Cross-Talk	X_{TALK}	Output power = 1W		--	–75	--	dB
Signal-to-Noise Ratio	SNR	1% THD + N		--	100	--	dB
Power Supply Rejection Ratio	PSRR	Frequency @1kHz		--	–70	--	dB
Dynamic Range	DR	Input level –60dBFS		--	100	--	dB
Efficiency	η	Output power = 10W+10W		--	90	--	%
Over-Temperature Protection	OTP	Guaranteed by design		150	160	175	°C
Thermal Hysteresis				--	30	--	°C
Over-Current Protection	OCP			5	6.3	7.5	A
PVDDL/PVDDR Over-Voltage	OVP			29.5	30	30.9	V
PVDDL/PVDDR Under-Voltage	UVP			6	6.5	7	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Load Impedance			Inductor = 22μH, PVDD < 16V	3.6	--	--	Ω
			Inductor = 22μH, PVDD = 24V	5.4	--	--	
			Inductor = 10μH, PVDD < 15V	3.6	--	--	
			Inductor = 10μH, PVDD = 20V	5.3	--	--	
			Inductor = 10μH, PVDD = 24V	7	--	--	
			Inductor = 4.7μH, PVDD = 24V, for 800kHz	7	--	--	
I²C Interface Electrical Characteristics							
Pull-Down Current		I_{FO2}	(Note 6)	--	2	--	μA
Digital Output Low (SDA)		V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency		f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition		t_{BUF}		1.3	--	--	μs
Hold Time After (Repeated) Start Condition		$t_{HD,STA}$		0.6	--	--	μs
Repeated Start Condition Setup Time		$t_{SU,STA}$		0.6	--	--	μs
Stop Condition Time		$t_{SU,STD}$		0.6	--	--	μs
Data Hold Time		$t_{HD,DAT\ (OUT)}$		225	--	--	ns
Input Data Hold Time		$t_{HD,DAT\ (IN)}$		0	--	900	ns
Data Setup Time		$t_{SU,DAT}$		100	--	--	ns
Clock Low Period		t_{LOW}		1.3	--	--	μs
Clock High Period		t_{HIGH}		0.6	--	--	μs
Clock Data Fall Time		t_F		20	--	300	ns
Clock Data Rise Time		t_R		20	--	300	ns
Spike Suppression Time		t_{SP}		--	--	20	ns
Slave Mode I²S Interface Electrical Characteristics							
High-level input voltage		V_{IH}		2	--	--	V
Low-level input voltage		V_{IL}		--	--	0.8	V
SDO	VOH : High-Level Output Voltage	V_{OH}	--	--	3.3	--	V
	VOL : Low-Level Output Voltage	V_{OL}		--	--	0.4	
Frequency		f_{SCLKIN}		1.024	--	12.288	MHz
Setup Time, LRCK to SCLK Rising Edge		t_{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge		t_{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge		t_{su2}		10	--	--	ns
Hold Time, SDIN from SCLK Rising Edge		t_{h2}		10	--	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Rise/Fall Time for SCLK/LRCK	t_r/t_f		--	--	8	ns
I^2S Duty Cycle	%		40	--	60	%

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is measured at the top of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

Note 6. The capability of the receiver to pull down the SDA line when during the acknowledge clock pulse.

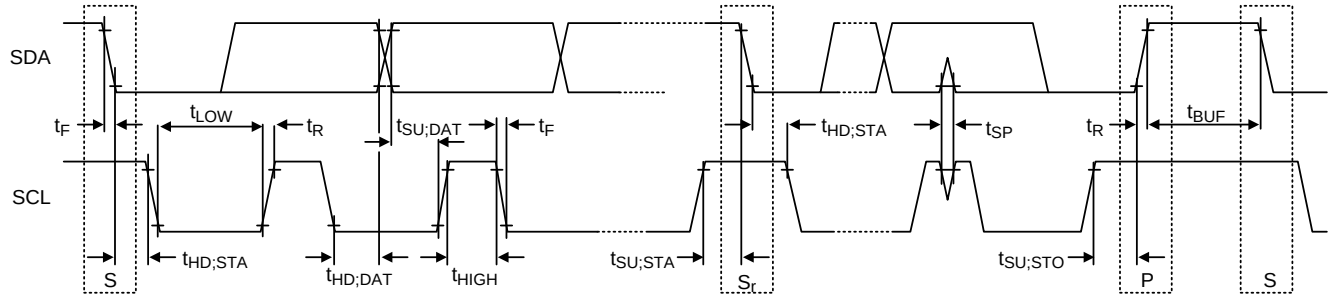


Figure 1. I^2C Interface Trimming Diagram

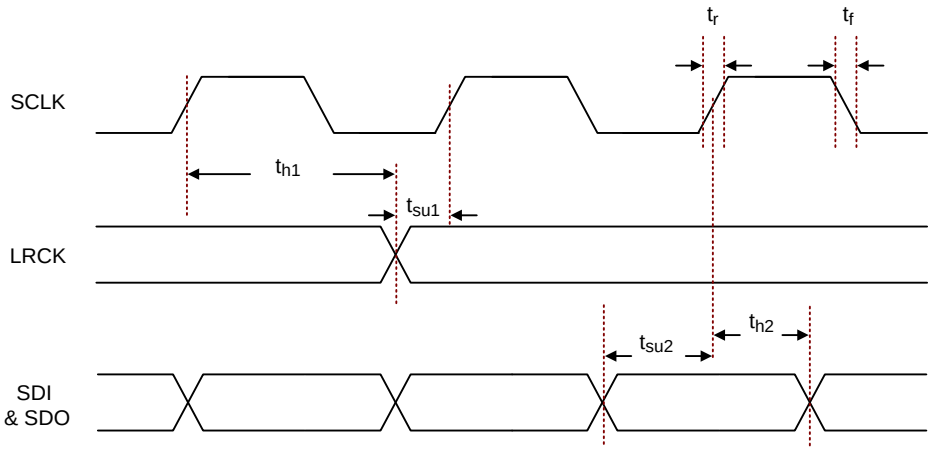
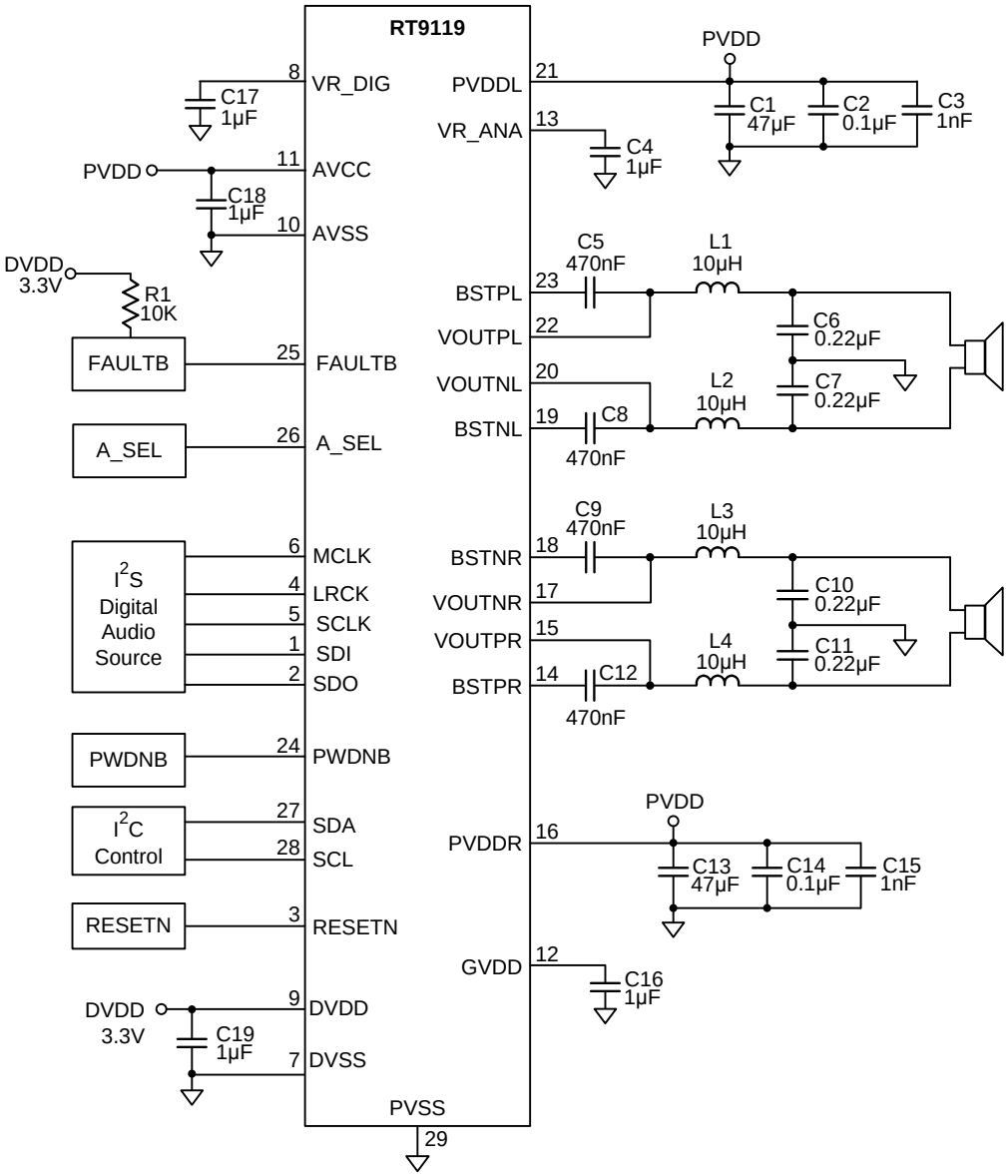
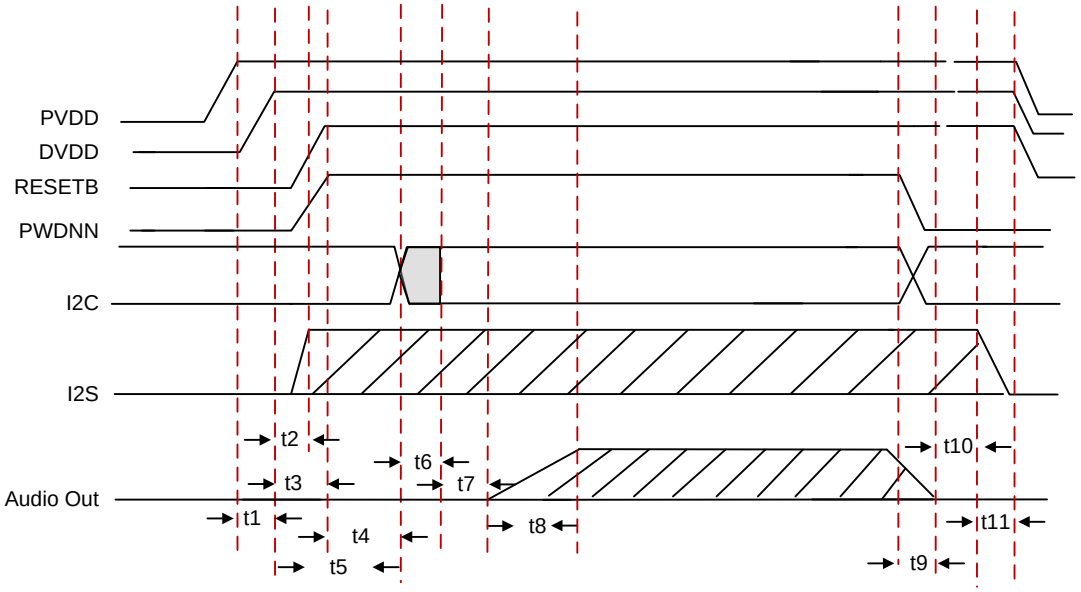


Figure 2. Timing Diagram of Slave Mode I^2S Interface

Typical Application Circuit



Timing Diagram



t1 (PVDD, DVDD) : ≥ 0ms, or, <0ms
t2 (I^2S) : >0ms, or, <0ms, after PVDD, DVDD release, no limitation before or after RESETB release, but recommended release before RESETB
t3 (DVDD to RESETB, PWDNN) : ≥0ms, should after DVDD release
t4 (RESETB, PWDNN to I^2C) : ≥1ms
t5 (DVDD to I^2C) : ≥10ms
Note : I^2C timing should meet both t4 and t5 requirement.
t6 : Depends on initial sequence finished time
t7 : Start Up Time including the SST time
t8 : Ramp up time of gain steps is from mute state to target gain.
t9 : Ramp down time of gain steps is from target gain to mute state.
t10 : >0ms, I^2S off, after t9
t11 : ≥0ms, after t10
A_SEL: Depends on the A_SEL high or low, as for the different address, no restriction, before initial setting.

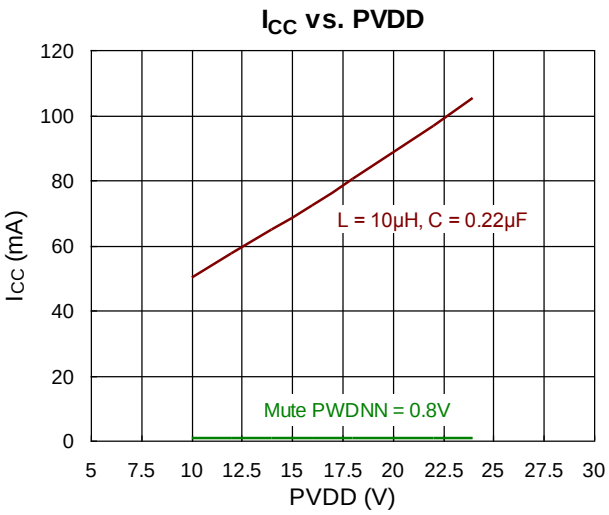
Figure 3. Power On/Off Sequence

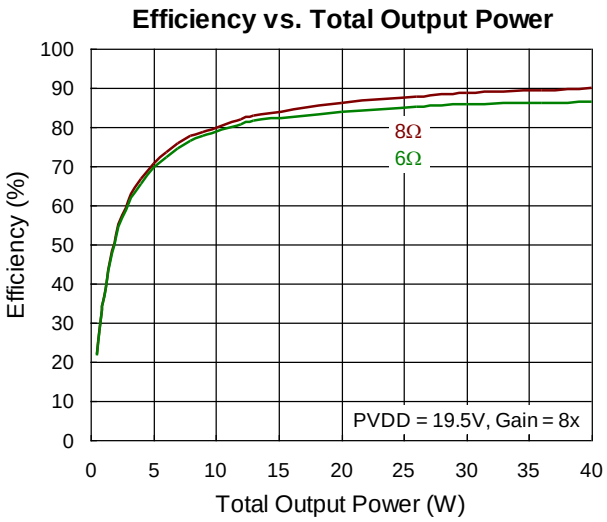
Initial Sequence

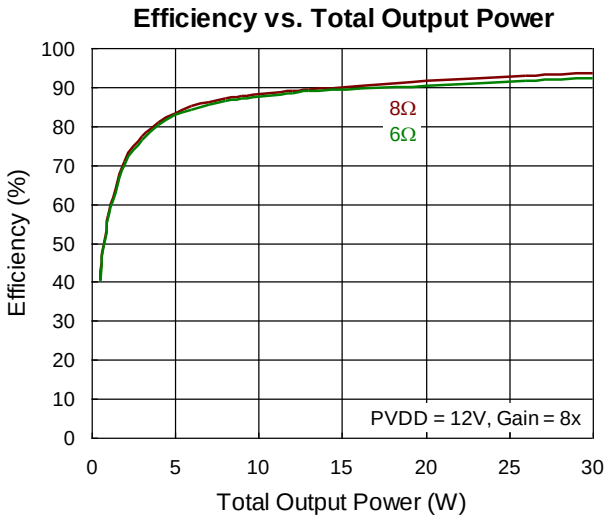
Sequence	Reg_Addr	Reg_Size	Reg_value	Description	
1	0x80	1	0x80	SW Reset, can be removed if hardware reset is already applied	Initial Setting
1mS Delay					
2	0x02	1	0x06	I^2S Bit Resolution setting(Optional)	
3	0x0E	1	0x07	Class D gain setting (Optional)	
4	0xD8	1	0x01	Disable DEPOP Function	
5	0x10	1	0x21	Enable DC Protection(Threshold and timing setting is optional)	
6	0x06	1	0x08	Set OCP to latch mode	
7	0xE0	1	0x31	SST Time = 40mS	
8	0x07	2	0x01, 0x80	Turn the volume on	
9	0x05	1	0x01	Amp turn on (For PWM 400kHz)	Amp Turn On
9	0x05	1	0x11	Amp turn on (For PWM 800kHz)	Amp Turn On

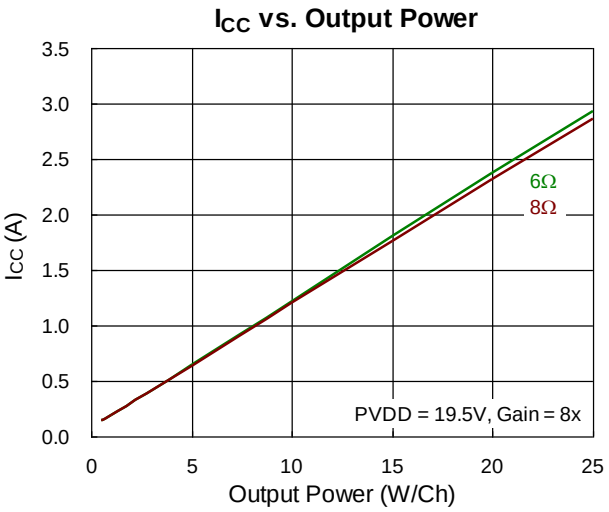
Typical Operating Characteristics

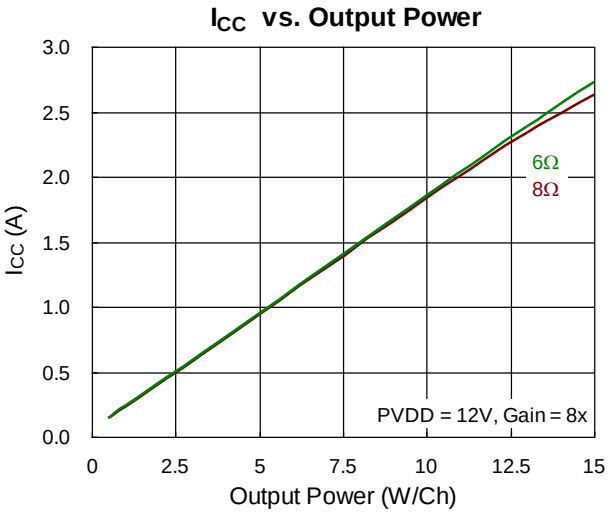
PWM = 400k

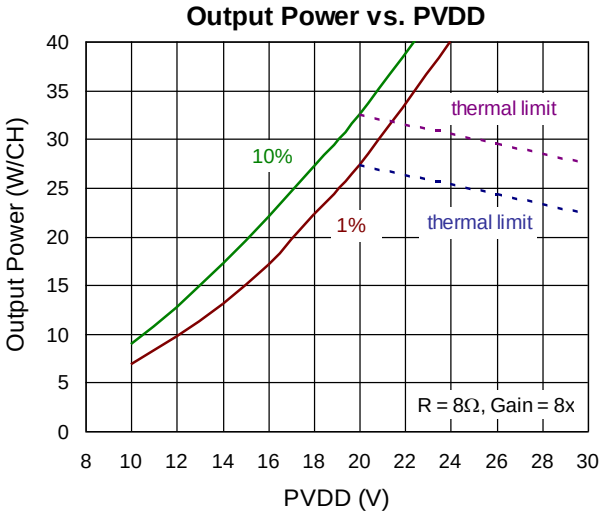




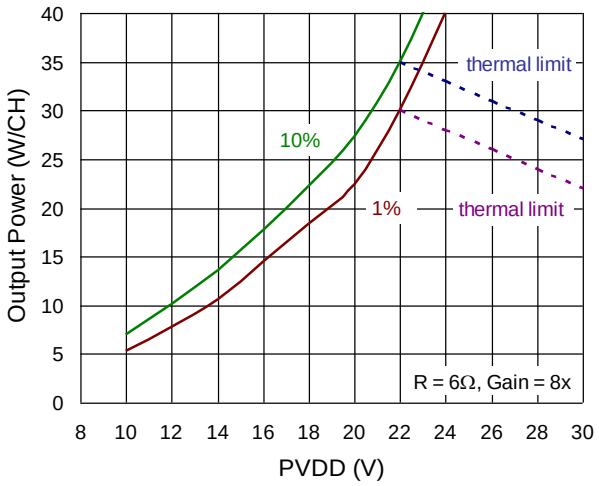




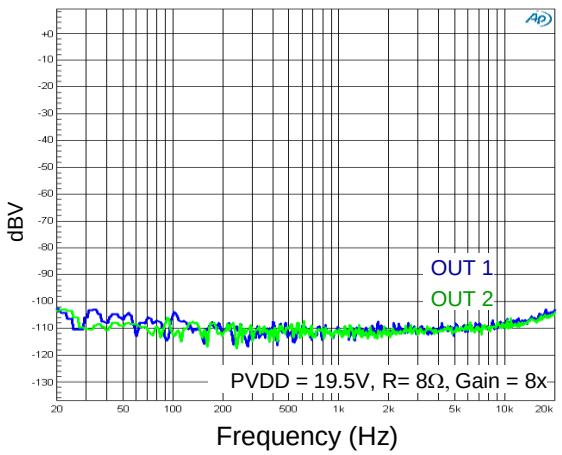




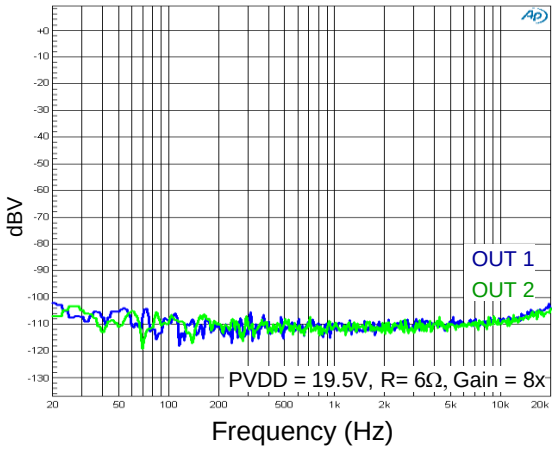
Output Power vs. PVDD



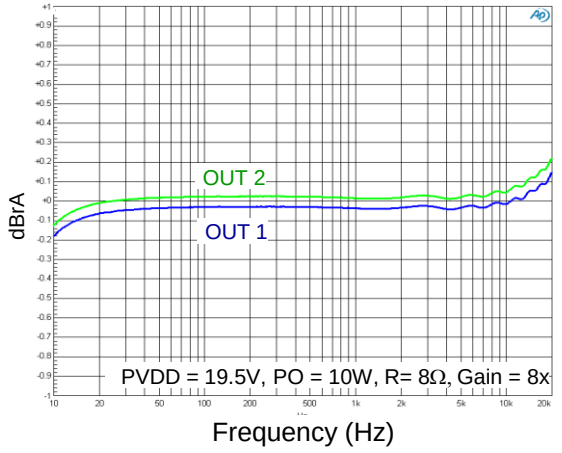
FFT of Output Noise



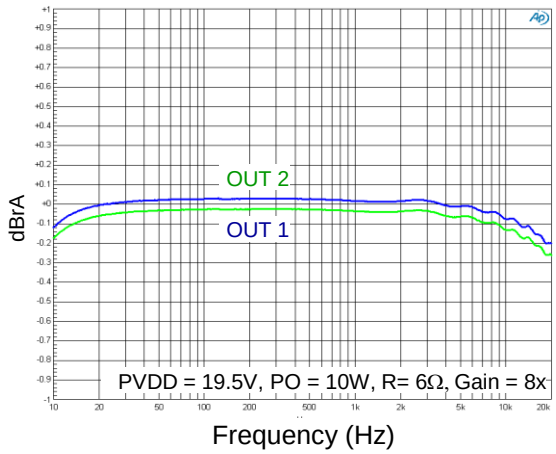
FFT of Output Noise



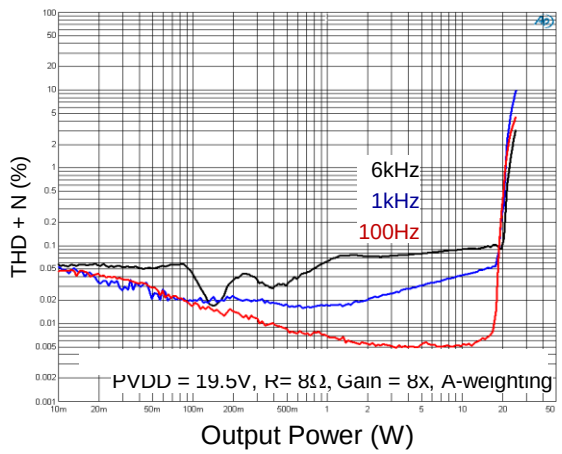
Output Level vs. Frequency



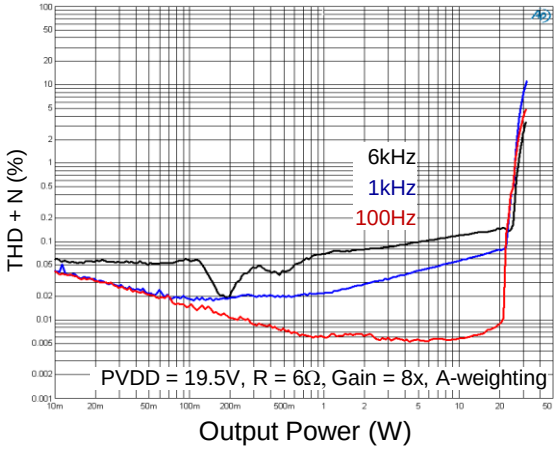
Output Level vs. Frequency



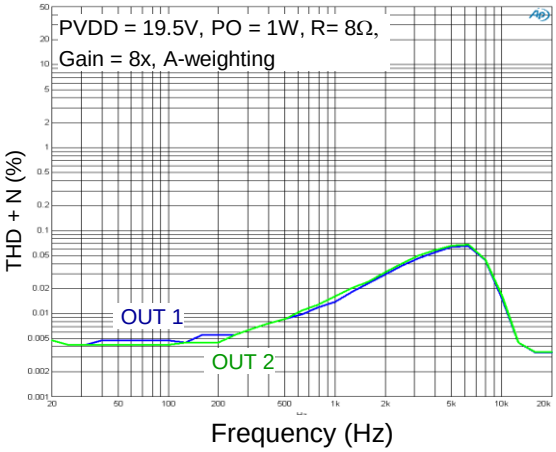
THD + N vs. Output Power



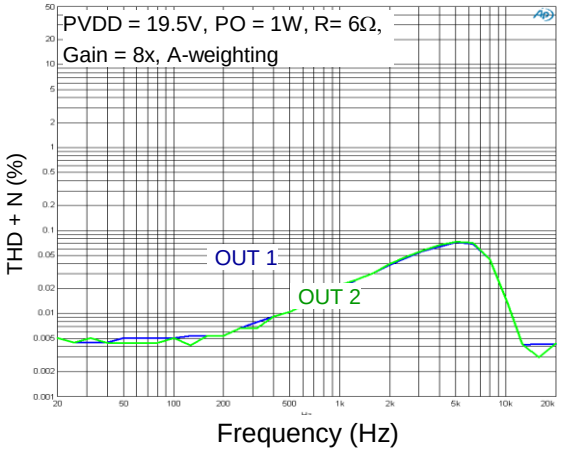
THD + N vs. Output Power



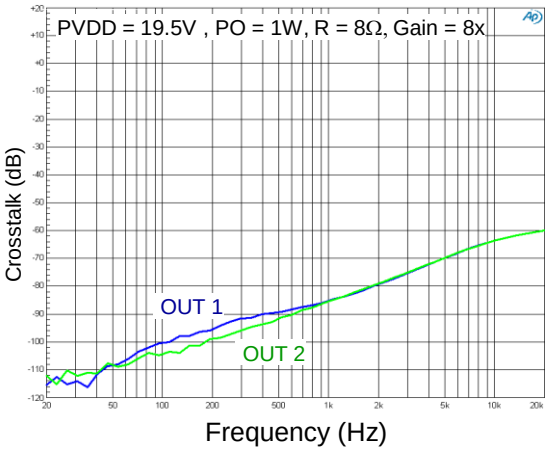
THD + N vs. Frequency



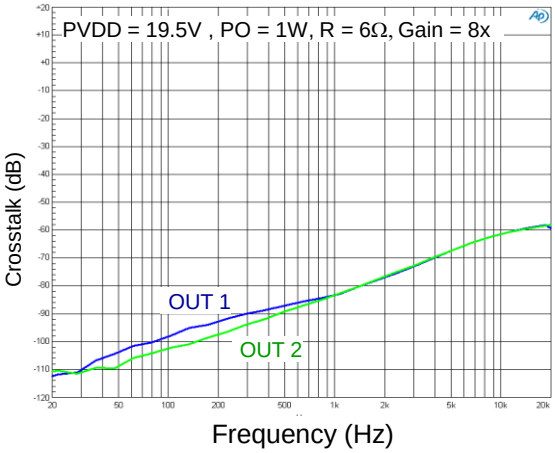
THD + N vs. Frequency



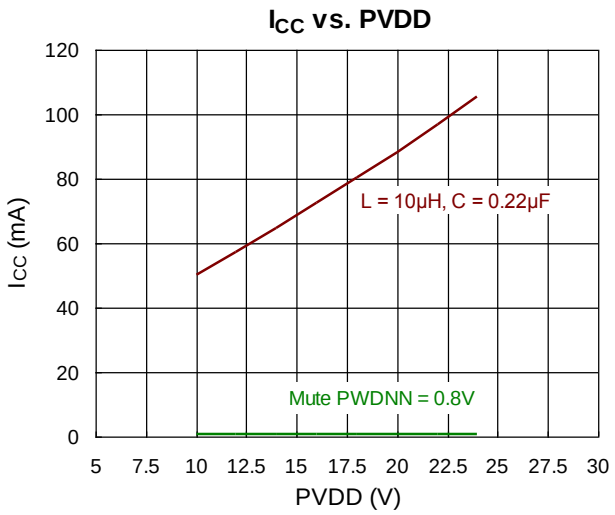
Crosstalk vs. Frequency

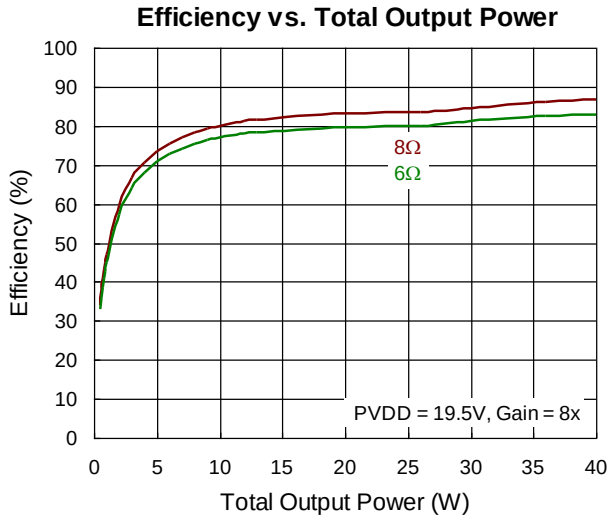


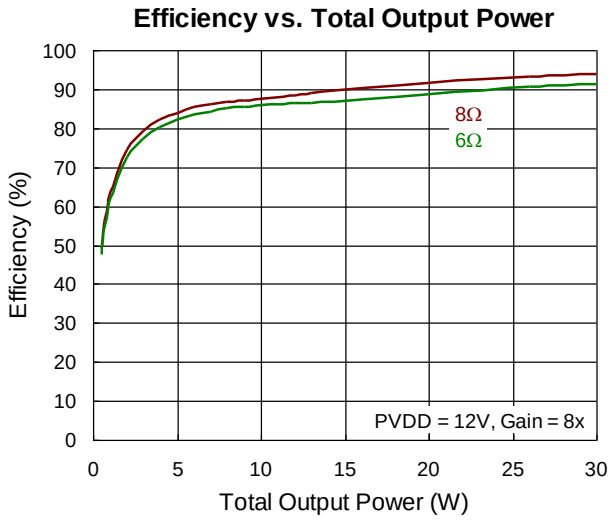
Crosstalk vs. Frequency

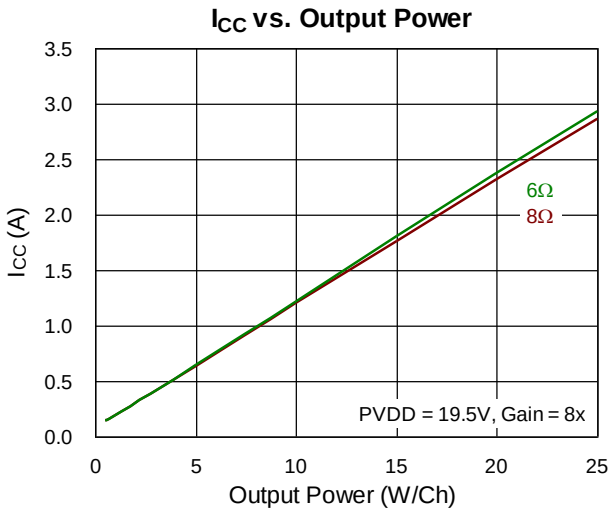


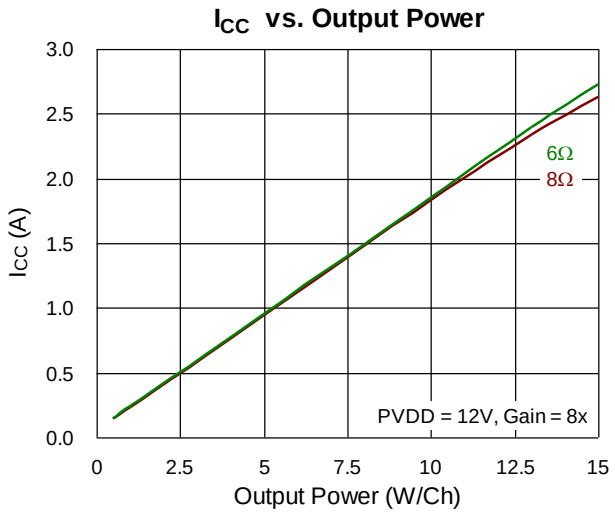
PWM = 800k

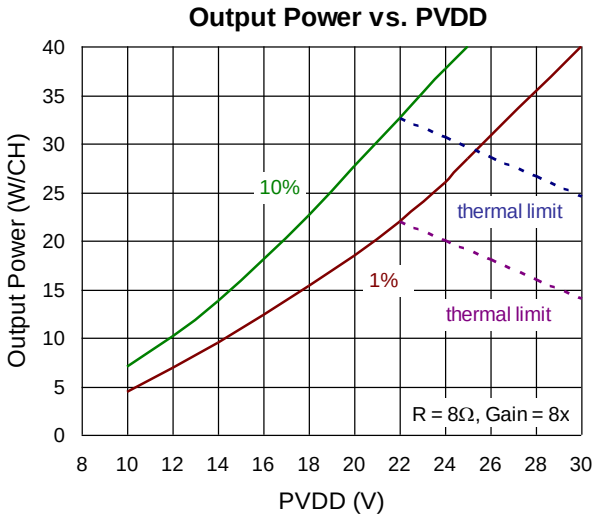




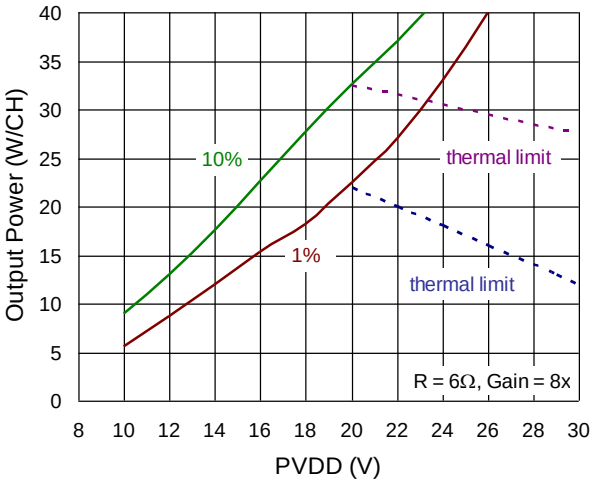




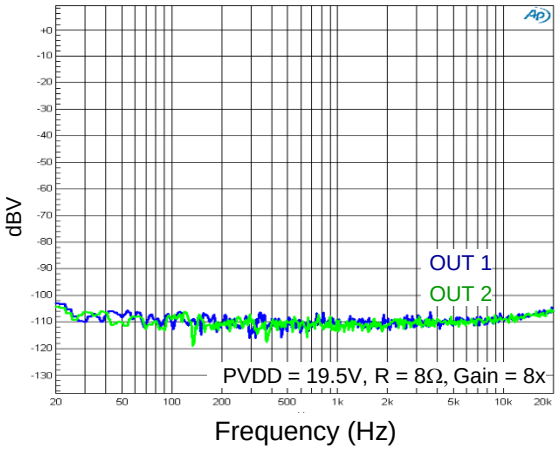




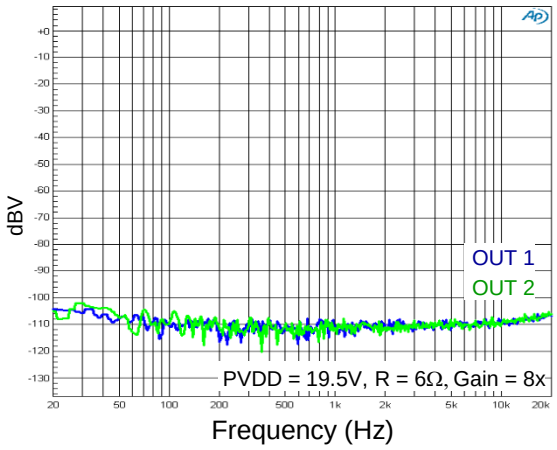
Output Power vs. PVDD



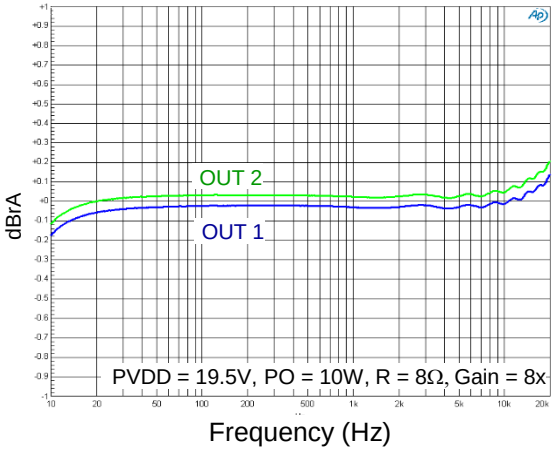
FFT of Output Noise



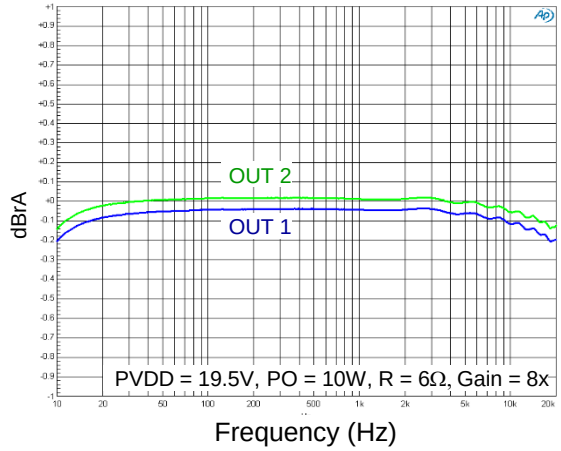
FFT of Output Noise



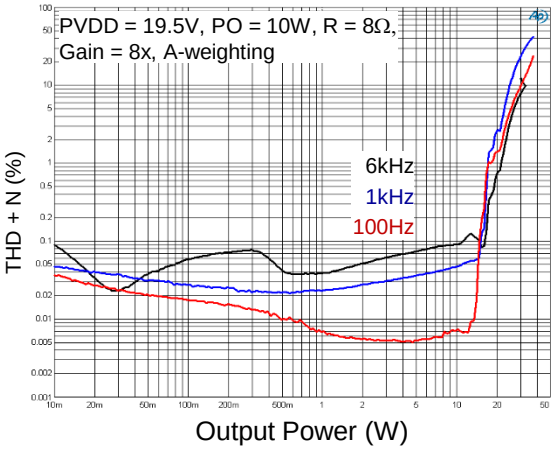
Output Level vs. Frequency



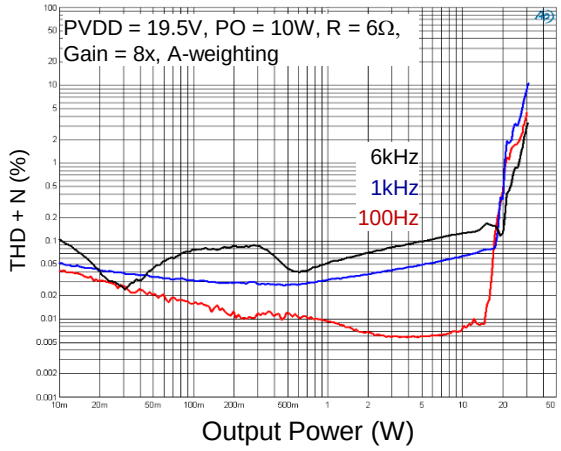
Output Level vs. Frequency



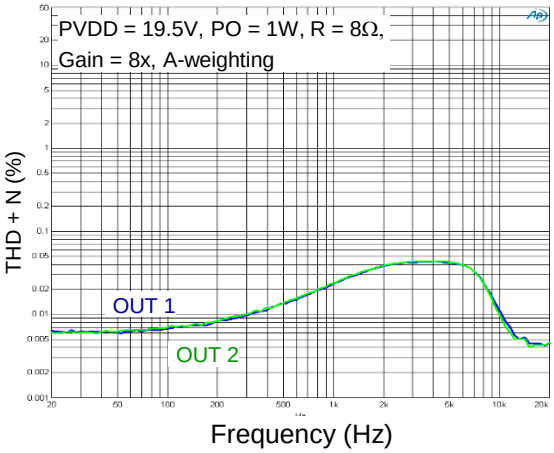
THD + N vs. Output Power



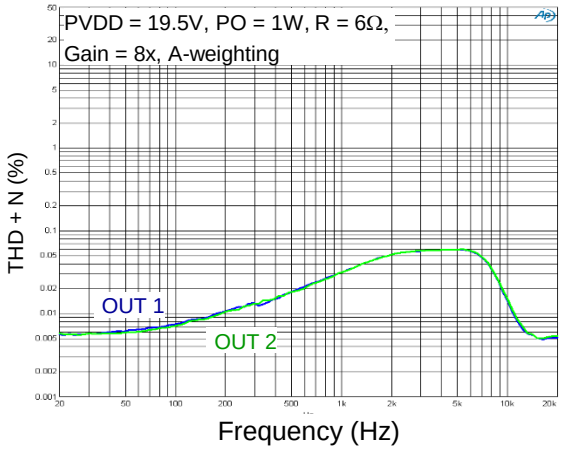
THD + N vs. Output Power



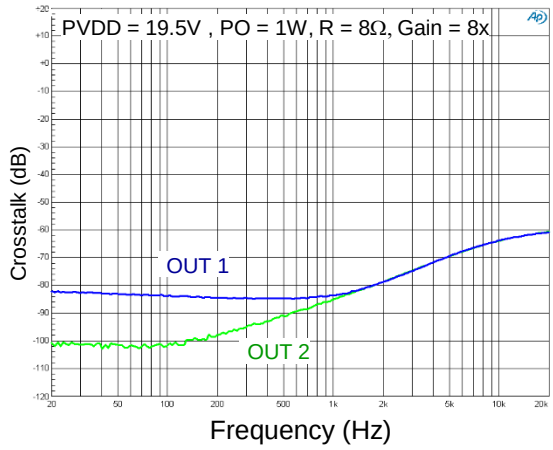
THD + N vs. Frequency



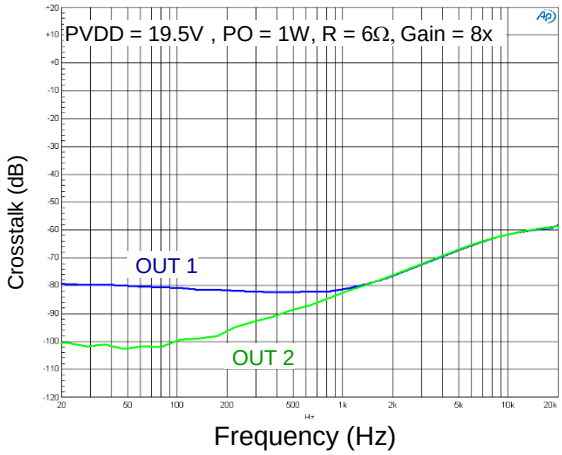
THD + N vs. Frequency



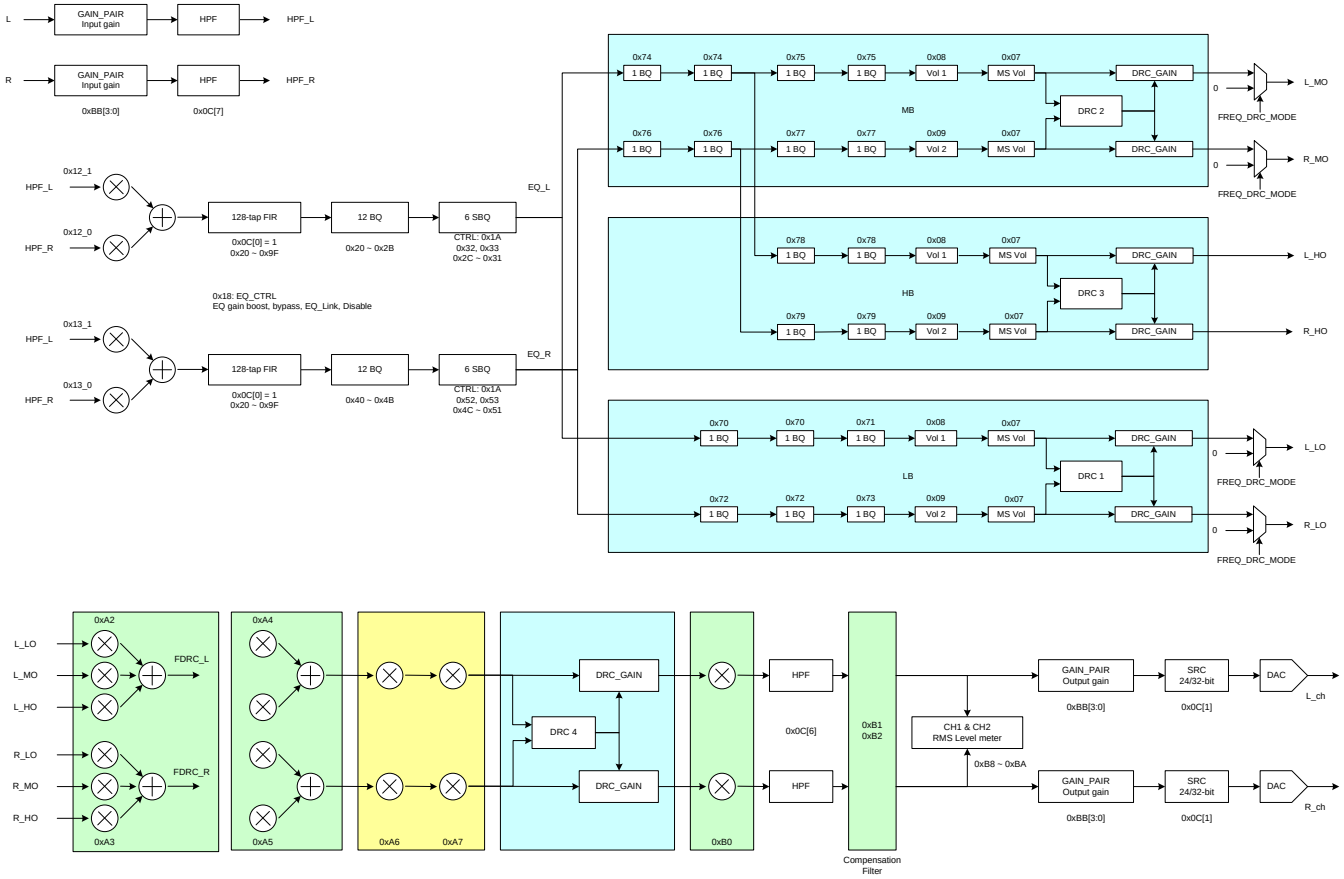
Crosstalk vs. Frequency



Crosstalk vs. Frequency

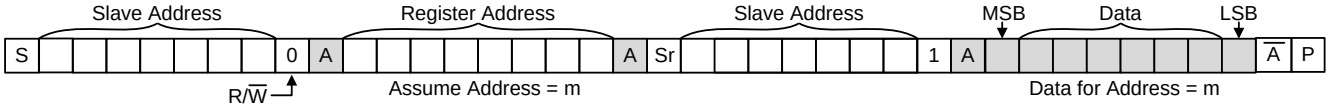


Signal Path

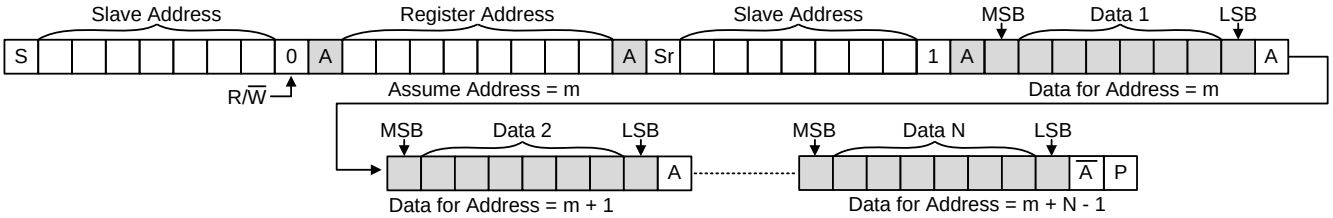


Read and Write Function

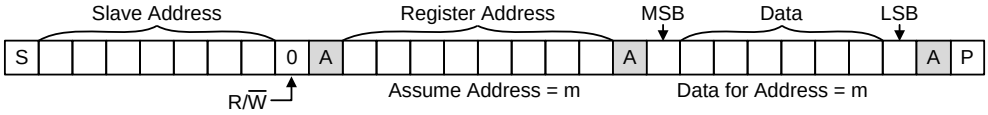
Read single byte of data from Register



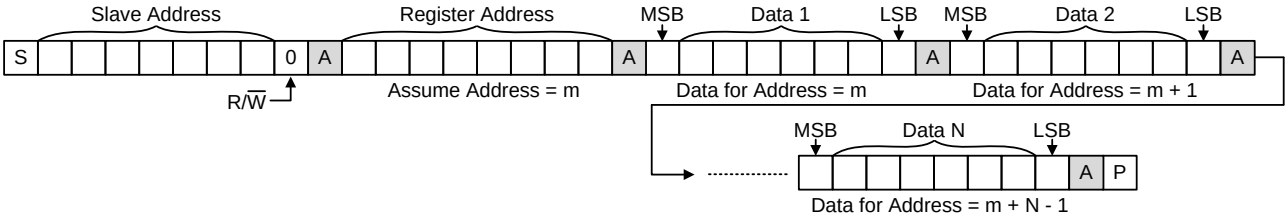
Read N bytes of data from Registers



Write single byte of data to Register



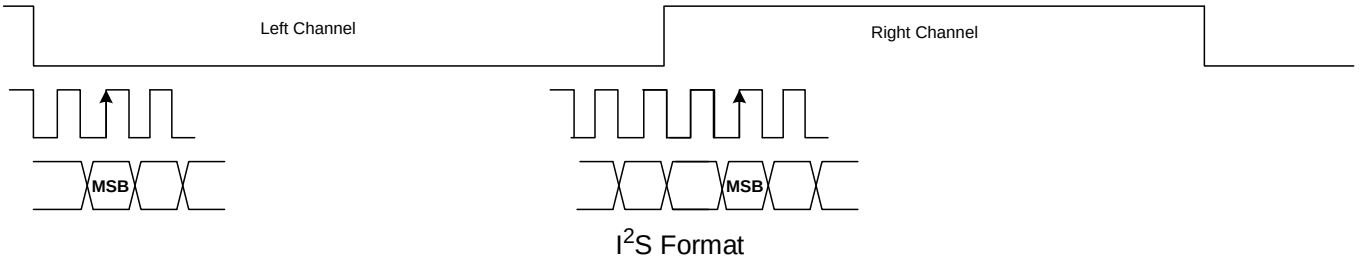
Write N bytes of data to Registers



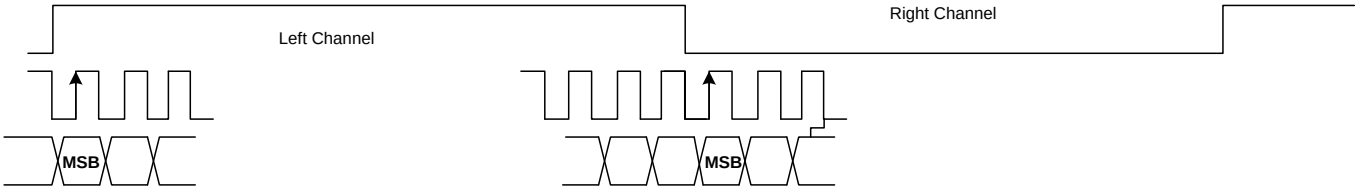
Driven by Master, Driven by Slave, P Stop, S Start, Sr Repeat Start

Audio Interface

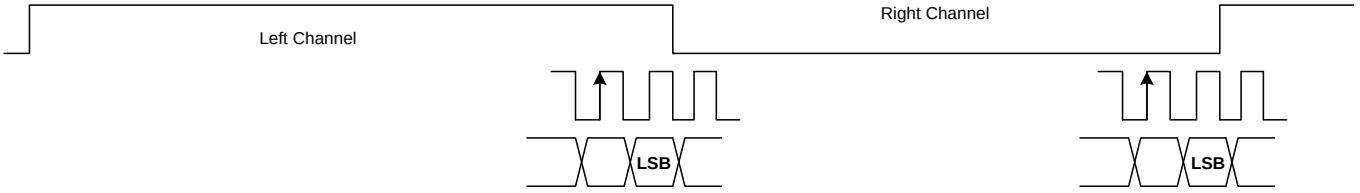
The RT9119 supports three kinds of audio interface, I^2S, Left justify and Right justify. Each kind of interface support 32 bit, 24 bit, 20bits and 16 bits format. The timing diagram is shown below.



I^2S Format



Left Justify



Right Justify

Address	BITS	Name	Description
0x02	3:0	AUD_MODE	0000 : 16bits right justify 0001 : 20bits right justify 0010 : 24bits right justify 0011 : 32bits right justify 0100 : 16bits I^2S 0101 : 20bits I^2S 0110 : 24bits I^2S 0111 : 32bits I^2S 1000 : 16bits left justify 1001 : 20bits left justify 1010 : 24bits left justify 1011 : 32bits left justify others : No define

PBTL Function

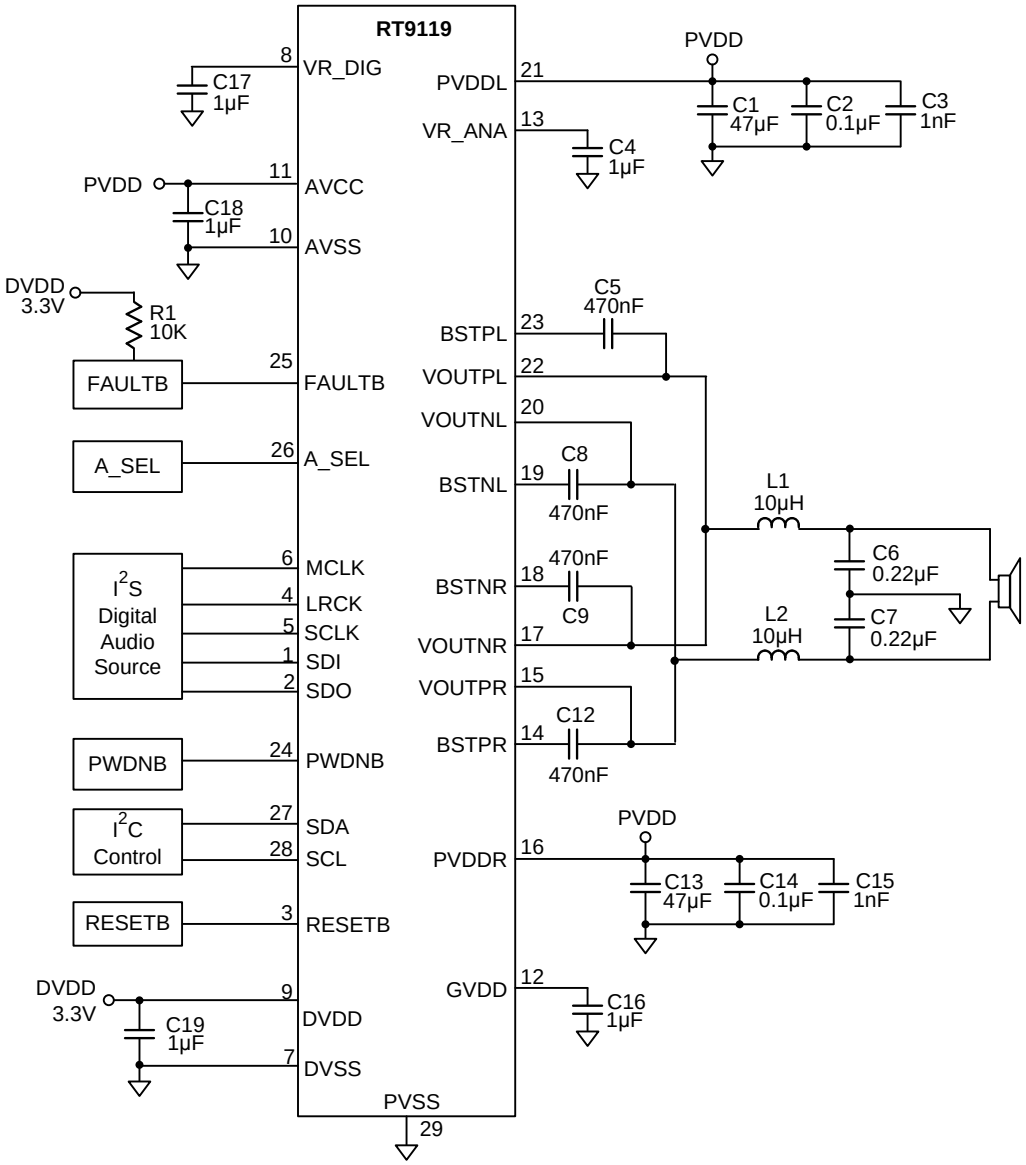
It can be configure by the hardware, also need to change the software setting.

The Input signal, can be configured by the input mixer, from register 0x12 to configure the input signal.

Address	BITS	Name	Description
0x05	5	D_PBTL	0 : BTL, 1 : PBTL

Address	BITS	Name	Description
0x12	63:32	CH1_IN_MIX_1	u[31:26],mix_1[25:0] u : Unused
	31:0	CH1_IN_MIX_0	u[31:26],mix_0[25:0] u : Unused

Mono PBTL Application Circuit



Protection Behavior

If the protection behavior happened, the IC will automated detect, there are some behavior as below list

Protection	Auto recovery	Shutdown Amp	Fault pin pull low
DC Protection	No	Yes	Yes
MCLK ERROR	Depends on 0x06 bit[6]	Yes	Yes, depends on 0x04 bit[6]
SCLK ERROR	Depends on 0x06 bit[5]	Yes	Yes, depends on 0x04 bit[5]
LRCK ERROR	Depends on 0x06 bit[4]	Yes	Yes, depends on 0x04 bit[4]
OC ERROR	Depends on 0x06 bit[3]	Yes	Yes, depends on 0x04 bit[3]
OV ERROR	Depends on 0x06 bit[2]	Yes	Yes, depends on 0x04 bit[2]
OT ERROR	Depends on 0x06 bit[1]	Yes	Yes, depends on 0x04 bit[1]
UV ERROR	Depends on 0x06 bit[0]	Yes	Yes, depends on 0x04 bit[0]

Address	Bits	Name	Description
0x04	6	MCLK_ERROR_mask	Fault mask for 0x03 MCLK error
	5	SCLK_ERROR_mask	Fault mask for 0x03 SCLK error
	4	LRCK_ERROR_mask	Fault mask for 0x03 LRCK error
	3	OC_ERROR_mask	Fault mask for 0x03 OC error
	2	OV_ERROR_mask	Fault mask for 0x03 OV error
	1	OT_ERROR_mask	Fault mask for 0x03 OT error
	0	UV_ERROR_mask	Fault mask for 0x03 UV error

Fault Behavior Type Select

If the protection behavior happened, the IC will automate detect, there are some error type can be configured as below list

Address	BITS	Name	Description
0x06	6	MCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	5	SCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	4	LRCK_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	3	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch Noted : Select 1
	2	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch

Address	BITS	Name	Description
	1	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch
	0	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0 : Auto recovery 1 : Latch

Reference Clock Selection

Due to the coefficient of PLL can be automated selected, so the RT9119 can choose the MCLK/SCLK as the reference clock from register setting.

Address	Reference Clock	Example
0x05	MCLK	To choose the reference clock Bit[0] to 0 : Reference clock is MCLK
	SCLK	To choose the reference clock Bit[0] to 1 : Reference clock is SCLK

Master Volume Gain

Address	BITS	Name	Equation
0x07	10:0	MS_VOL[10:0]	Equation : 24dB - (Dec * 0.0625) Range: 24dB (0X000) to mute (0x7ff) Ex : 10dB, Hex = 0xE0 Dec = 224 Gain = 24dB - (224 * 0.0625) = 10dB

Gain	Dec	Hex
24dB	0	0x00
10dB	224	0XE0
. . .	. . .	. . .
0dB	384	0x180
. . .	. . .	. . .

Volume Ramp

000 : 1 step in every sample

001 : mute -> –40dB, every sample with 1 step. –40dB -> 24dB, 2 sample with 1 step.

010 : mute -> –40dB, 2 sample with 1 step. –40dB -> 24dB, 4 sample with 1 step.

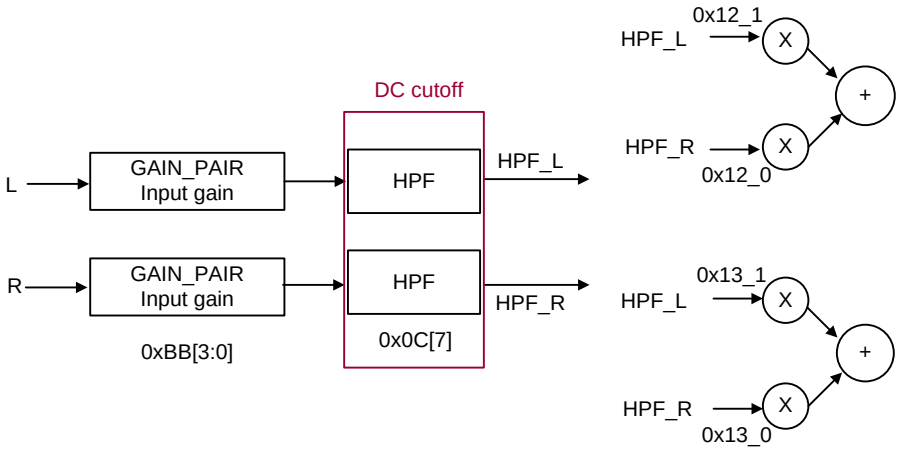
Others : mute -> –40dB, 4 sample with 1 step. –40dB -> 24dB, 8 sample with 1 step.

Address	BITS	Name	Description
0x0A	2:0	VOL_RAMP_MODE[2:0]	Volume Slew step control 000 : 1 step in every sample 001 : mute -> –40dB, every sample with 1 step. –40dB -> 24dB, 2 sample with 1 step. 010 : mute -> –40dB, 2 sample with 1 step. –40dB -> 24dB, 4 sample with 1 step. Others : mute -> –40dB, 4 sample with 1 step. -40dB -> 24dB, 8 sample with 1 step.

Input High Pass Filter

Block Diagram & Description

→There are DC-Cut filter for each channel. The cut off frequency is 1.5Hz

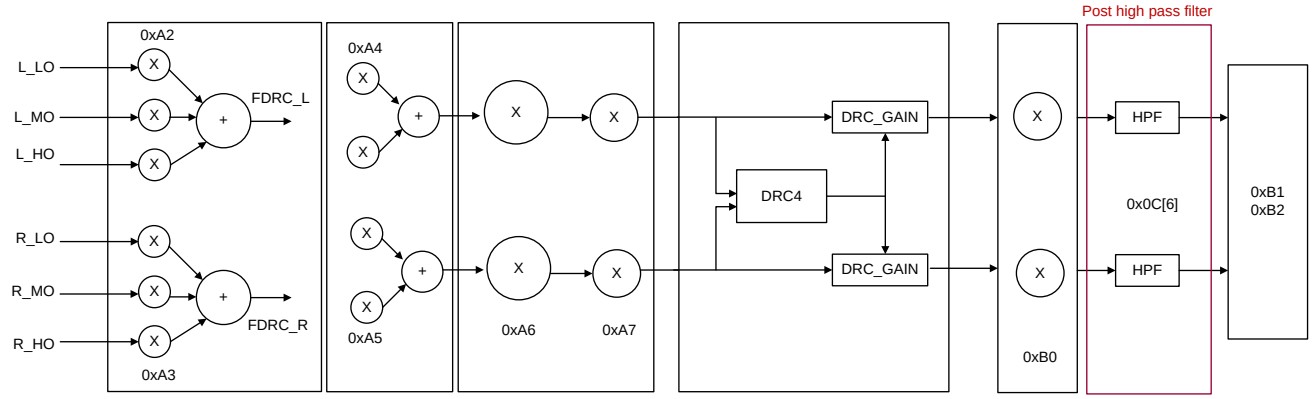


Address	BITS	Name	Description
0x0C	7	HPF_EN	1 : Input high-Pass filter enable 0 : Input high-Pass filter disable

Output High Pass Filter

Block Diagram & Description

→There are DC-Cut filter for each channel. The cut off frequency is 1.5Hz

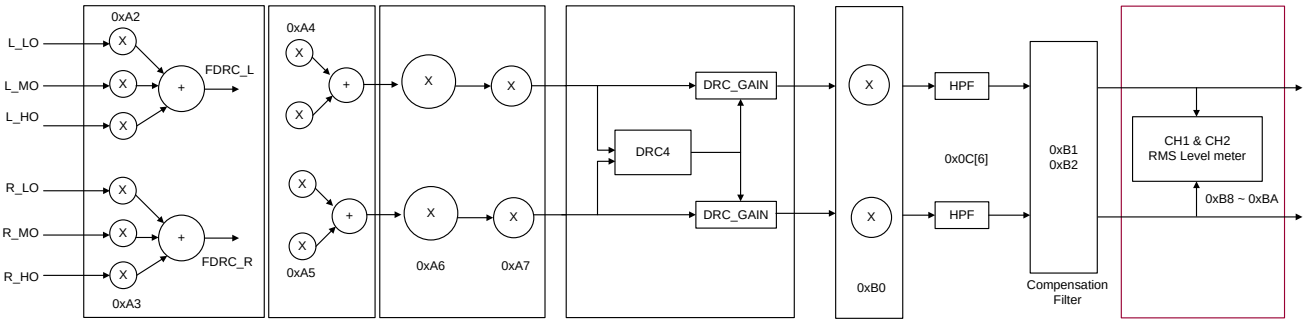


Address	BITS	Name	Description
0x0C	6	HPF_POS_EN	1 : Post high Pass filter enable 0 : Post high Pass filter disable

RMS Level Meter & Data Output

Block Diagram & Description

→The final stage of whole signal path is RMS level meter. It output the final level of each channel before digital filter.



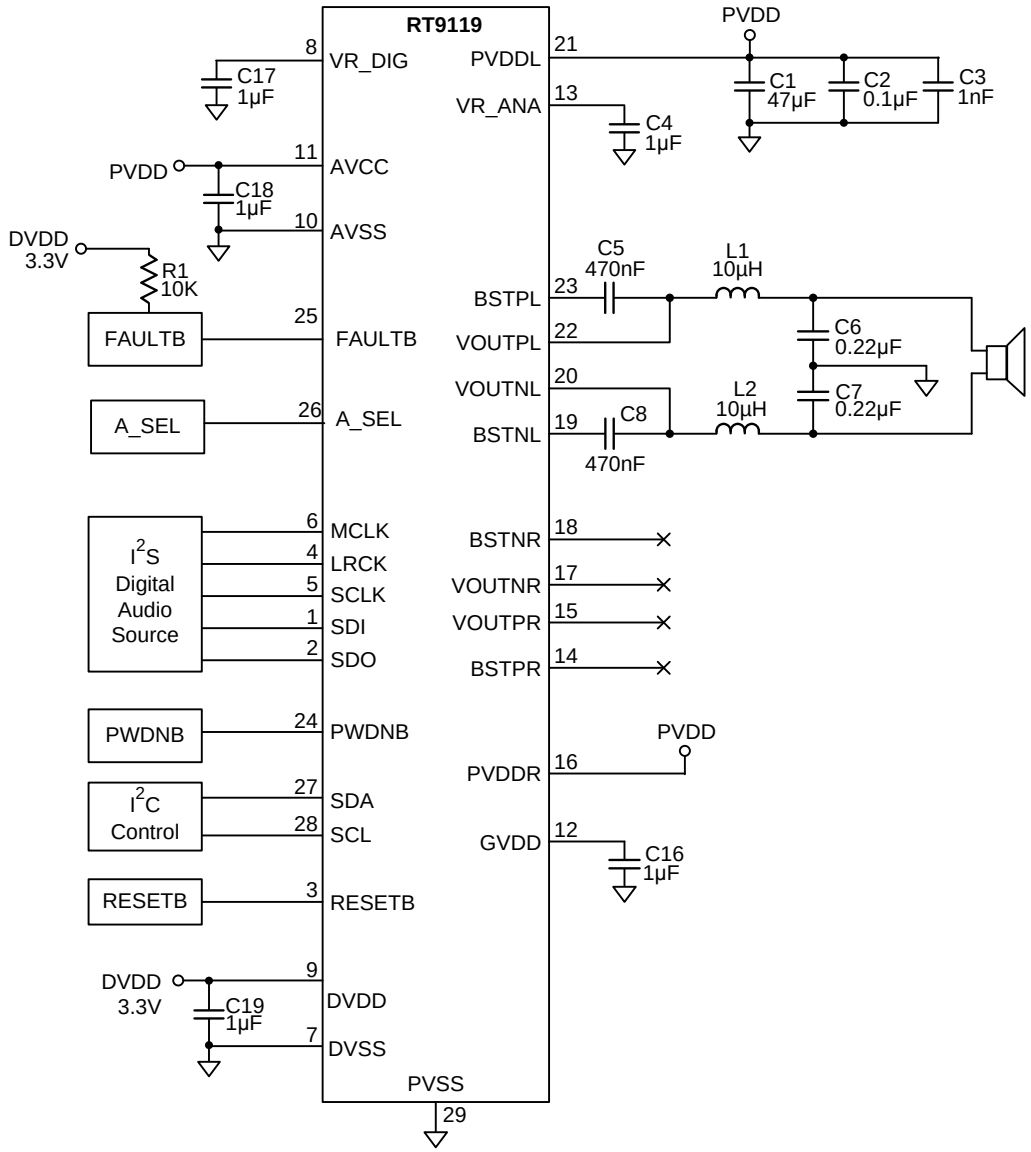
Address	BITS	Name	Description
0x0D	6:4	SDO_SEL[2:0]	000 : No output 001 : Interface output 010 : FIR output 011 : EQ output 100 : SBQ output 101 : DRC/Mixer/Gain Output 110 : Final output 111 : RMS output Other : No output

Address	BITS	Name	Description
0xB9	31:0	CH1_RMS[31:0]	To read the final RMS output
0xBA	31:0	CH2_RMS[31:0]	To read the final RMS output

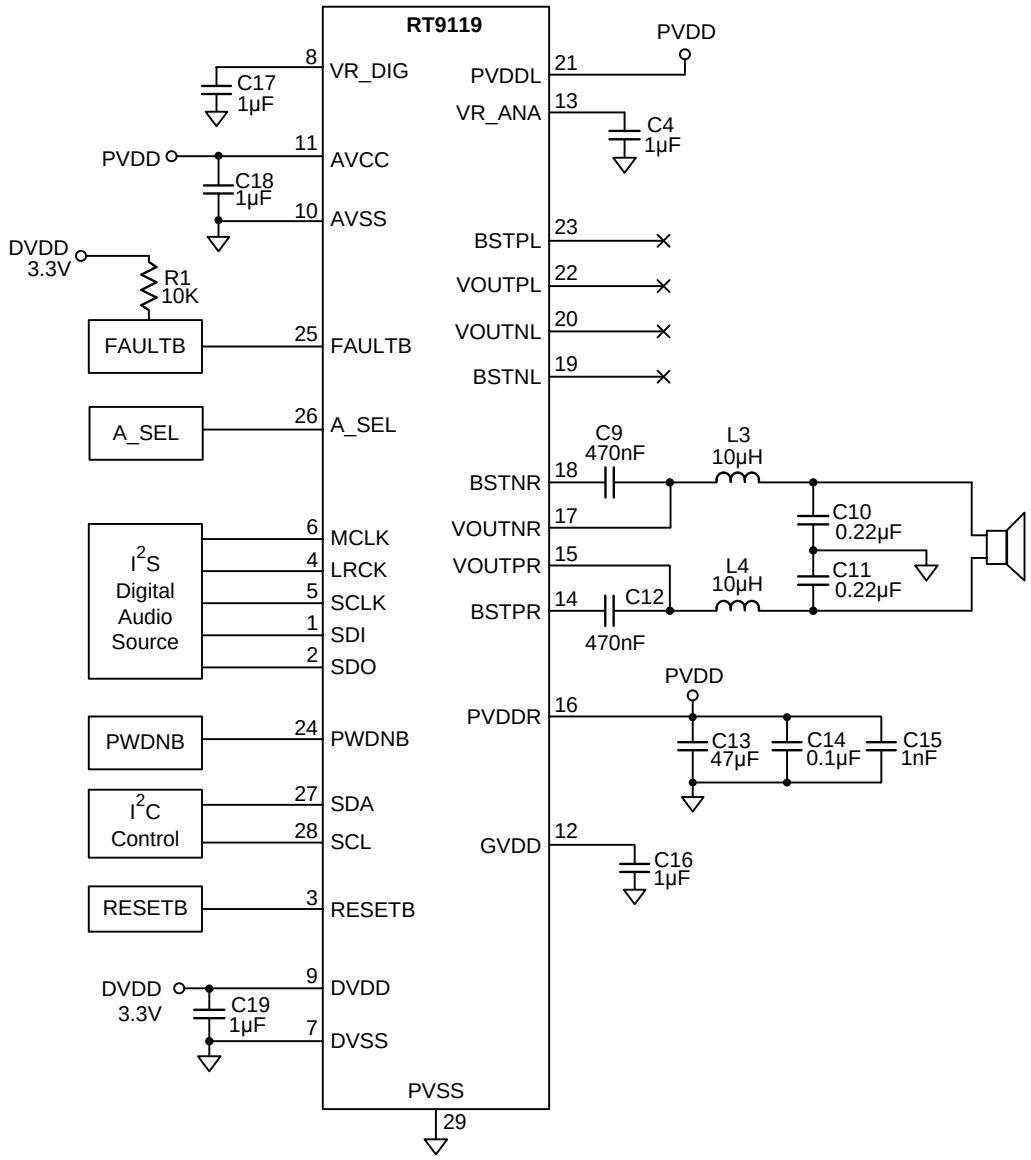
Mono Configuration

To use the mono configuration, It can be configured by register setting.

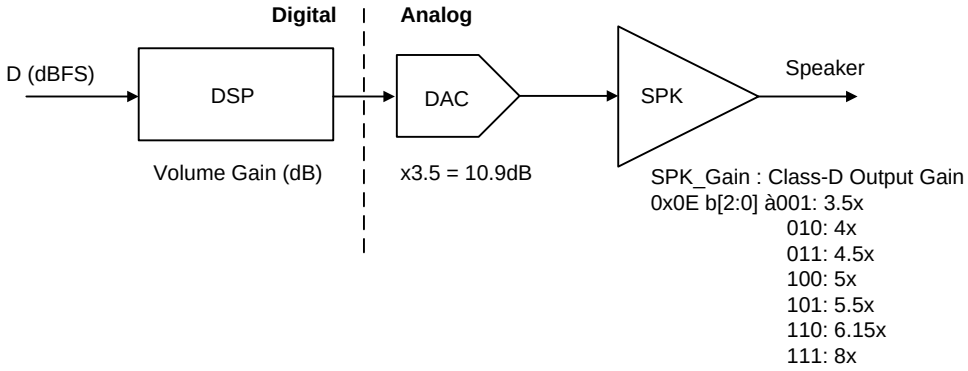
Address	BITS	Name	Description
0x0F	7	D_LPFR_EN	Enable DAC RCH LPF, 0 : Disable 1 : Enable
	6	D_LPFL_EN	Enable DAC LCH LPF, 0 : Disable 1 : Enable
	5	D_EN_RCH_PWR	RCH PWR stage enable, 0 : Disable 1 : Enable
	4	D_EN_LCH_PWR	LCH PWR stage enable, 0 : Disable 1 : Enable
	3	D_DAC_RCH_EN	Enable DAC_RCH, 0 : Disable 1 : Enable
	2	D_DAC_LCH_EN	Enable DAC LCH, 0 : Disable 1 : Enable
	1	D_SPK_RCH_EN	Enable Class D RCH SPK, 0 : Disable 1 : Enable
	0	D_SPK_LCH_EN	Enable Class D LCH SPK, 0 : Disable 1 : Enable

Mono Configuration	Example
Use Left Channel	Set the Bit[7], Bit[5], Bit[3], Bit[1] to Zero, others keep 1 

Mono Configuration	Example
Use Right Channel	Set the Bit[6], Bit[4], Bit[2], Bit[0] to Zero, others keep 1



Amplification Gain

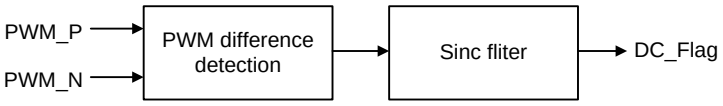


Output voltage calculation formula = $10^{(D+Vol\_Gain)/20}$ x 3.5 x Output_Gain (Vp)

Address	BITS	Name	Description
0x0E	2:0	D_SPK_GAIN[2:0]	Class D output gain, 111=8x, 110=6.15x, 101=5.5x, 100=5x, 011=4.5x, 010=4x, 001=3.5x Noted : Output Voltage will x1.14, When the AVDD(0xD5) adjust to 5.7V

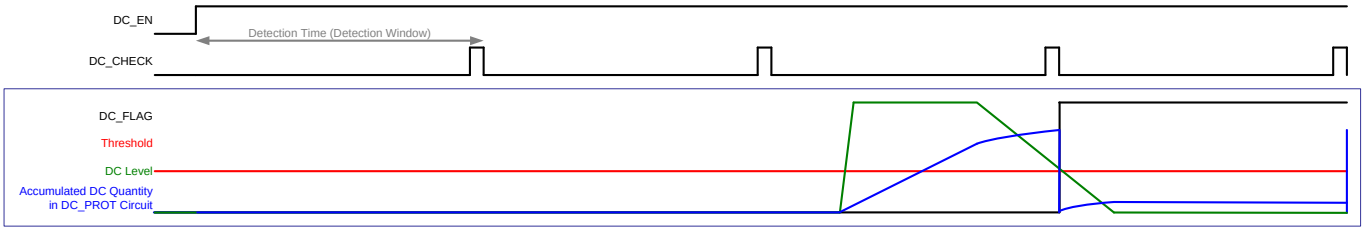
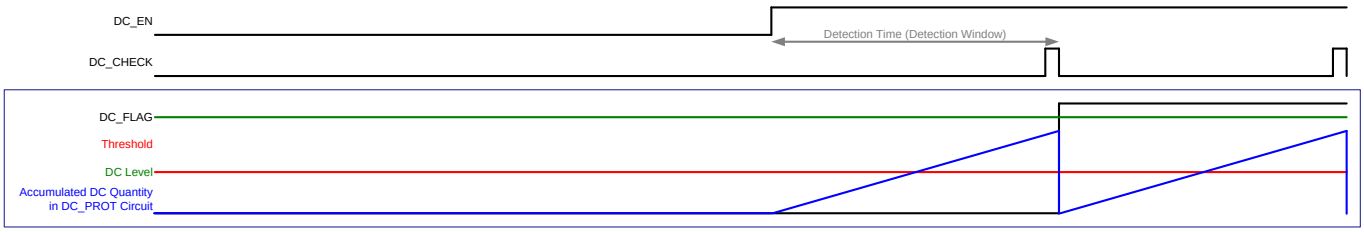
DC Protection Function

It is to use to protect the loudspeaker, when there are some DC exists at the output. The method is to detect DC at final stage (PWM), calculate the difference of the PWM and a sinc filter to decide the DC level. The IC will shut down when detect the DC.



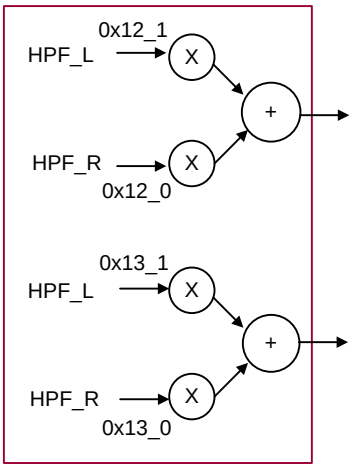
Address	BITS	Name	Description
0x10	5:4	DC_TH[1:0]	DC threshold for DC detection 00 : No available 01 : 12.5% 10 : 18.75% 11 : 25%
	3	DC_TEST	Short time check mode
	2	Reserved	
	1	DC_TIME_SEL	Detection time 0 : 342ms 1 : 684ms
	0	DC_EN	1 : DC Protection enable

DC Detection Timing

Description
Detection Scheme Detection window, for judge DC level within the detection time Accumulated DC Quantity in DC_PROT Circuit Calculate DC quantity for judgment Clear accumulate value at check state If Accumulated Quantity greater than DC Threshold at check state DC_FLAG go high Example 1 If (DC_EN = 1 then HPF_EN = 0) DC level increase to DC_FLAG smaller than DC Detection Time Large DC cause Accumulate value increasing too fast to exceed threshold at check state    Example 2 (HPF_EN = 0 then DC_EN = 1) DC_EN enable to DC_FLAG equal to DC Detection Time Start calculate timing and Accumulated value when DC_EN go high and DC_FLAG go high at check state 

Input Mixer

Block Diagram & Description
→ Input mixer range is from mute to 12dB, fixed point design, bit25 is sign bit.



->MIX_0 is from HPF_R
->MIX_1 is from HPF_L

Address	BITS	Name	Description
0x12	63:32	CH1_IN_MIX_1	u[31:26],mix_1[25:0] u : Unused
	31:0	CH1_IN_MIX_0	u[31:26],mix_0[25:0] u : Unused
0x13	63:32	CH2_IN_MIX_1	u[31:26],mix_1[25:0] u : Unused
	31:0	CH2_IN_MIX_0	u[31:26],mix_0[25:0] u : Unused

Input Mixer Gain Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x12, 0x13</td><td>25:0</td><td>mix_1[25:0] mix_0[25:0]</td><td>Equation: 20Log (Dec/8388608)
Range: 12dB (0X1ffffff) to Mute (0x00000000)
Ex : 6dB, Hex = 0x1000000
Dec = 16777216
Gain = 20Log(16777216/8388608) = 6dB

<table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>12dB</td><td>33554431</td><td>0X1FFFFFF</td></tr><tr><td>6dB</td><td>16777216</td><td>0X1000000</td></tr><tr><td>.
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</table>

Input Mixer Inverse Phase Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0x12, 0x13</td><td>25:0</td><td>bit25 is sign bit, 3.23 format.</td><td>Equation: Hex = DEC2HEX
Ex : Gain = 6dB,
Hex = 0x1000000
Phase Inverse: Hex = DEC2HEX(-16777216) = 0xFF000000

<table><tr><th>Inverse</th><th>Dec</th><th>Hex</th></tr><tr><td>12dB</td><td>–33554431</td><td>0XFE000001</td></tr><tr><td>6dB</td><td>–16777216</td><td>0XFF000000</td></tr><tr><td>.
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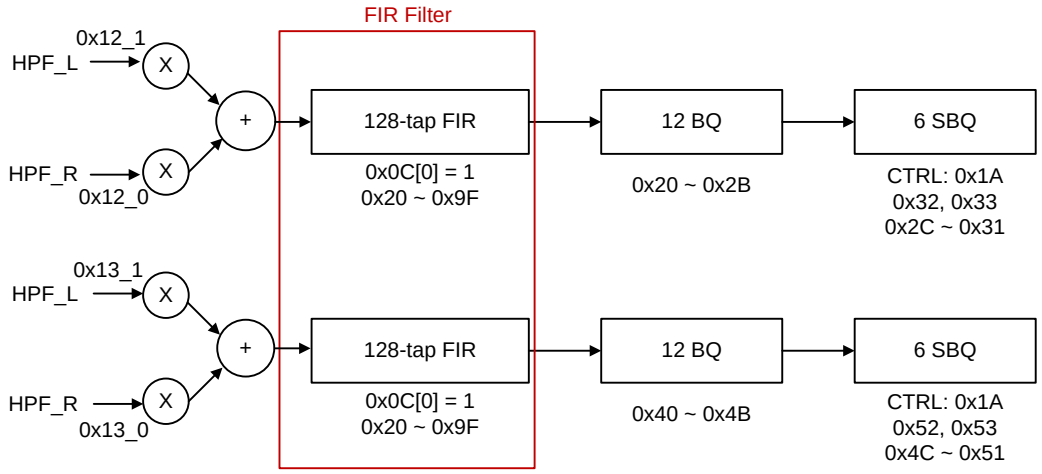
FIR Filter

Block Diagram & Description

→ There is a 128 tap FIR filter, the data is 4.28 format.



Address	BITS	Name	Description
0x0C	2	FIR_EN	FIR filter enable 0 : Disable 1 : Enable
	0	REG_PAGE_SEL	Register page select 0 : default page 1 : FIR coefficients page For FIR page, register 0x20 to 0x9F are 128 coefficients, L/R are the same. Each coefficient is 4-byte, 3.23 format

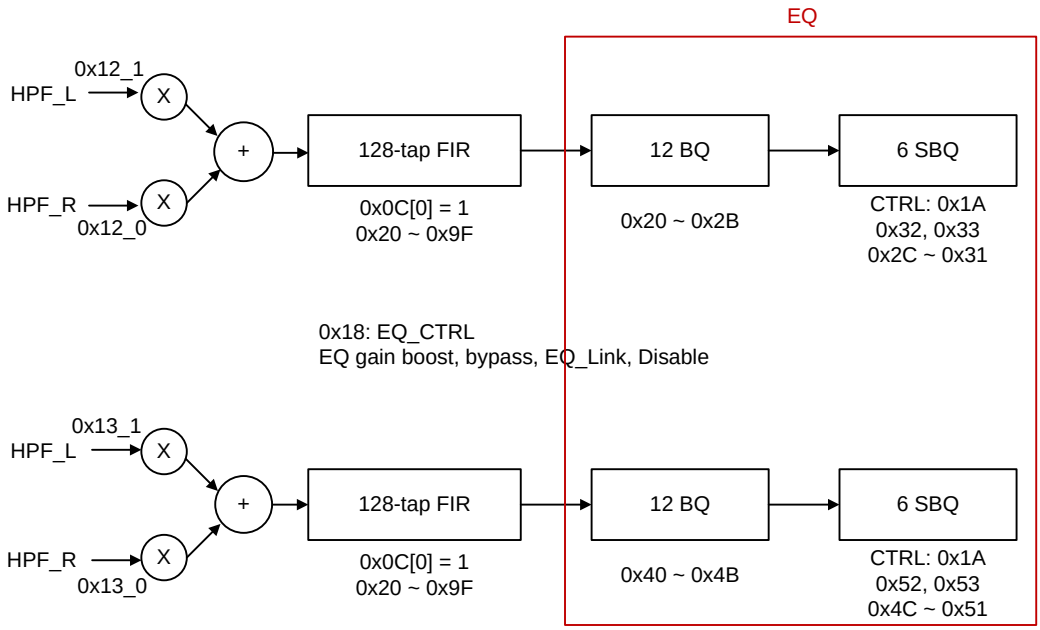
FIR Coefficient

Address	BITS	Name	Description
0x20	31:0	FIR_TAP1	When change to FIR page, register 0x20 to 0x9F are 128 coefficients, L/R are the same. Each coefficient is 4-byte, 3.23 format u[31:26], b0[25:0] u : Unused

Address	BITS	Name	Description
0x9F	31:0	FIR_TAP128	When change to FIR page, register 0x20 to 0x9F are 128 coefficients, L/R are the same. Each coefficient is 4-byte, 3.23 format u[31:26], b0[25:0] u : Unused

EQ Link & Bypass

Block Diagram & Description
→Link L/R channel EQ parameter automatically, and using the same parameter →EQ_BYPASS can bypass the EQ path in signal path. Each EQ band has disable bit. About EQ Bypass: →L channel EQ (12 BQs+6SBQs) Bypass for EQ1 to 18 is [0:17] →R channel EQ (12 BQs+6SBQs) Bypass for EQ1 to 18 is [0:17]



EQ Link/Partial Link

Address	BITS	Name	Description
0x18	3	EQ_LINK	0: L/R Can be written independently 1 : L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (CH1&CH2 BQ1~BQ12 and SBQ13~SBQ18 are linked together) ->Adjust separate channel EQ. ->When link, two channel EQ will be the same. Noted : EQ link should be enable first, then update the smooth Bi-Quad coefficient.
0x18	2:1	EQ_PART_LINK[1:0]	Partial link select, when bit 3 EQ_LINK = 1 00 : Link ALL x1 : Link CH1 & CH2 BQ7 to BQ12 1x : Link CH1 & CH2 BQ13 to BQ18 (smooth BQ)

EQ Bypass

Address	BITS	Name	Description
0x16	31:0	u[31:18], EQ_CH1_BYPASS[17:0] u : Unused	EQ Bypass Control For CH1 BQ1 to BQ18 is [0:17]
0x17	31:0	u[31:18], EQ_CH2_BYPASS[17:0] u : Unused	EQ Bypass Control For CH2 BQ1 to BQ18 is [0:17]

EQ Gain Boost

Address	BITS	Name	Description
0x14	31:0	u[31:18], EQ_CH1_GAIN_BOOST[17:0] u : Unused	Control L (CH1) channel BQ1 to BQ18 gain boost 0 : 0dB gain 1 : Bi-Quad result add 18 dB gain
0x15	31:0	u[31:18], EQ_CH2_GAIN_BOOST[17:0] u : Unused	Control R (CH2) channel BQ1 to BQ18 gain boost 0 : 0dB gain 1 : Bi-Quad result add 18 dB gain

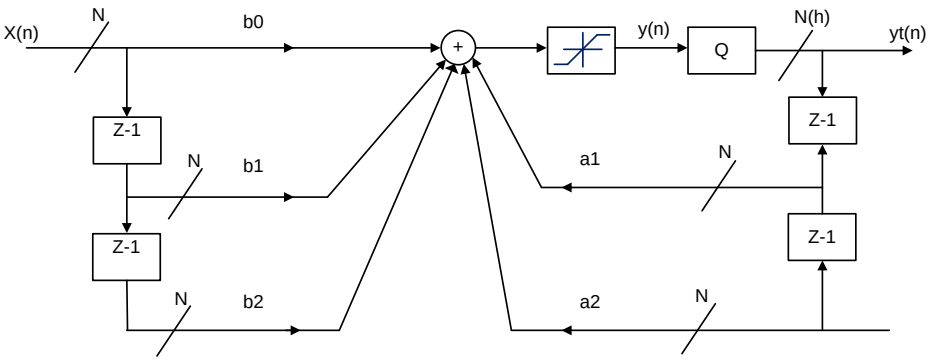
EQ

Block Diagram & Description

→ There are 12 Bands of Bi-Quad filter for each Channel. So There are 18 bands of the Bi-Quad can be used including the smooth Bi-Quad . 26 bits coefficient for each parameter. It is 4.36 format.

EQ parameter: b0/b1/b2/a1/a2

Update coefficient after writing 5 coefficients



Ch1 EQ

Address	BITS	Name	Description
0x20	159:128	CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x2B	159:128	CH1_bq_12_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_bq_12_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_bq_12_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_bq_12_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_bq_12_a2	u[31:26], a2[25:0] u : Unused

Ch2 EQ

Address	BITS	Name	Description
0x40	159:128	CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused

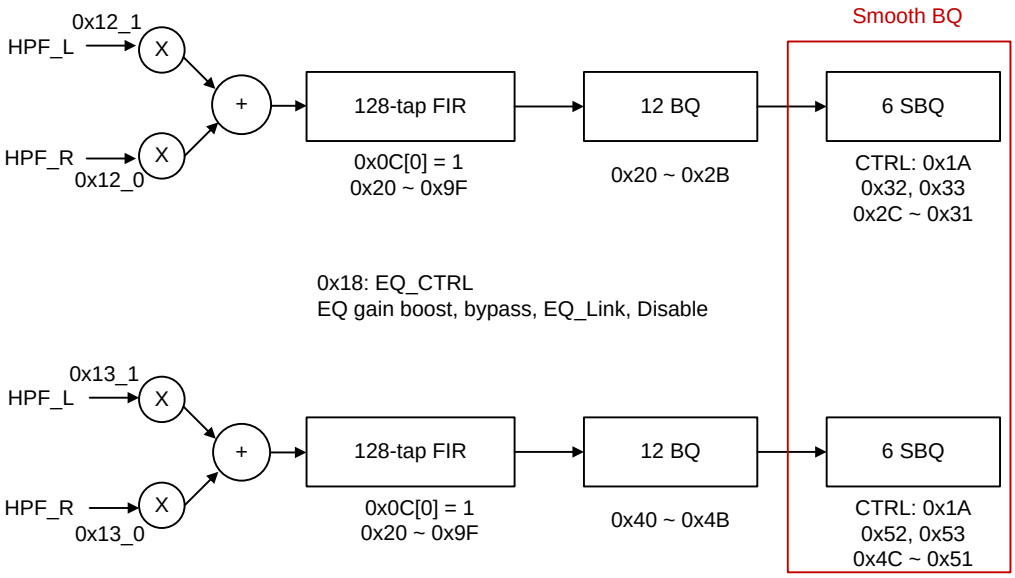
Address	BITS	Name	Description
0x4B	159:128	CH2_bq_12_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_bq_12_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_bq_12_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH2_bq_12_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_bq_12_a2	u[31:26], a2[25:0] u : Unused

Smooth Bi-Quad

Block Diagram & Description

→Smooth biquad is identical biquad filter with coefficient updated smoothly.

→New coefficient update linearly/exponentially to avoid undesirable sound during setting new coefficient for biquad.



→One smooth-BQ consists of 2 BQs to process the same audio signal in parallel. One of the BQs uses current coefficients and the other one uses updating coefficients to generate the outputs, BQ_1_output and BQ_2_output, respectively.

→For a-filter smooth, the output of smooth-BQ is the summation of BQ_1_output and BQ_2_output using the below equations.

SBQ_output[n] = a_1[n] * BQ_1_output[n]+a_2[n] * BQ_2_output[n]

a_1[n] = (1-AS) + AS * a_1[n-1], if BQ_1 is the current active BQ and a_1[0] = 1

a_2[n] = (1-AS) + AS * a_2[n-1], if BQ_2 is the updating BQ and a_2[0] = 0

If SBQ_UPDATE is triggered, a_1[n] = 0 and a_2[n] = 1 after TS samples

→For linear smooth, the equations for smooth-BQ are listed below.

a_1[n] = a_1[n-1] - 1/TS, if BQ_1 is the active BQ and a_1[0] = 1

a_2[n] = a_2[n-1] + 1/TS, if BQ_2 is the updating BQ and a_2[0] = 0

If SBQ_UPDATE is triggered, a_1[n] = 0 and a_2[n] = 1 after TS samples. When linear smooth is used, the TS shall be the power of 2 for design simplicity.

Smooth Bi-Quad Coefficient

Address	BITS	Name	Description
0x19	31:0	SMOOTH_BQ_AS	u[31:26], ae[25:0] Alpha filter coefficient for smoothing

Smooth Bi-Quad Control

Address	BITS	Name	Description
0x1A	31:16	Reserved	
	15:8	SMOOTH_BQ_TS[7:0]	After triggering coefficients update, smooth BQ delay in samples. After this delay, old coefficients are disabled. 4 to 1024 samples delay, 4 samples per step
	7:4	Reserved	
	3	SMOOTH_METHOD	Smooth method selection: 0 : By alpha filter (controlled by AS) 1 : By linear gain, controlled by TS, but only power of 2 is effective When 2N+1 > TS ≥ 2N, 2N steps is selected
	2	SMOOTH_DONE	Report status of smooth transition (after TS), 1= done
	1:0	SBQ_UPDATE[1:0]	Trigger smooth BQ coefficients update : When non-zero value is written, smooth transition is triggered. After transition is done, this register automatically goes back to 00. Before transition done, any new write to this register is invalid 00 : No update 01 : SBQ_BK1 to SBQ13, SBQ_BK2 to SBQ14 10 : SBQ_BK1 to SBQ15, SBQ_BK2 to SBQ16 11 : SBQ_BK1 to SBQ17, SBQ_BK2 to SBQ18

Ch1 SBQ

Address	BITS	Name	Description
0x2C	159:128	CH1_sbq_13_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_sbq_13_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_sbq_13_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_sbq_13_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_sbq_13_a2	u[31:26], a2[25:0] u : Unused

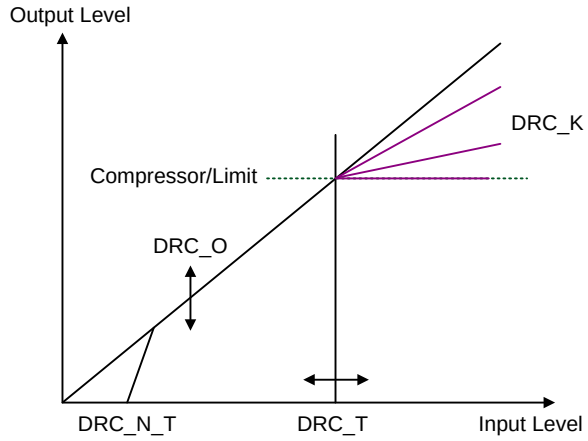
Address	BITS	Name	Description
0x33(Update address)	159:128	CH1_sbq_bk2_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH1_sbq_bk2_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH1_sbq_bk2_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH1_sbq_bk2_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH1_sbq_bk2_a2	u[31:26], a2[25:0] u : Unused

Ch2 SBQ

Address	BITS	Name	Description
0x4C	159:128	CH2_sbq_13_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_sbq_13_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_sbq_13_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH2_sbq_13_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_sbq_13_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x53(Update address)	159:128	CH2_sbq_bk2_b0	u[31:26], b0[25:0] u : Unused
	127:96	CH2_sbq_bk2_b1	u[31:26], b1[25:0] u : Unused
	95:64	CH2_sbq_bk2_b2	u[31:26], b2[25:0] u : Unused
	63:32	CH2_sbq_bk2_a1	u[31:26], a1[25:0] u : Unused
	31:0	CH2_sbq_bk2_a2	u[31:26], a2[25:0] u : Unused

Multi-Band DRC

DRC Description	Address	Description
DRC_T : Threshold	0x93, 0x99, 0x9F, 0xAA	
DRC_K : Compress ratio	0x94, 0x9A, 0xA0, 0xAB	
DRC_O : Make up gain	0x95, 0x9B, 0xA1, 0xAC	
DRC_N_T : Noise gate threshold	0xA9	
Noise Gate Enable	0x61	

Address	BITS	Name	Description
0x61	7	DRC4_N_EN	1 : DRC4 Noise gate enable 0 : DRC4 Noise gate disable
	6	DRC3_N_EN	1 : DRC3 Noise gate enable 0 : DRC3 Noise gate disable
	5	DRC2_N_EN	1 : DRC2 Noise gate enable 0 : DRC2 Noise gate disable
	4	DRC1_N_EN	1 : DRC1 Noise Gate enable 0 : DRC1 Noise gate disable

Address	BITS	Name	Description
0x93	31:0	DRC1_T[31:0]	T1[31:0], DRC1 threshold
0x94	31:0	DRC1_K[31:0]	u[31:26], K1[25:0] DRC1 compression ratio
0x95	31:0	DRC1_O[31:0]	u[31:26], O1[25:0] DRC1 make up gain
0x99	31:0	DRC2_T[31:0]	T2[31:0], DRC2 threshold
0x9A	31:0	DRC2_K[31:0]	u[31:26], K2[25:0] DRC2 compression ratio
0x9B	31:0	DRC2_O[31:0]	u[31:26], O2[25:0] DRC2 make up gain
0x9F	31:0	DRC3_T[31:0]	T3[31:0], DRC3 threshold
0xA0	31:0	DRC3_K[31:0]	u[31:26], K3[25:0] DRC3 compression ratio
0xA1	31:0	DRC3_O[31:0]	u[31:26], O3[25:0] DRC3 make up gain
0xAA	31:0	DRC4_T[31:0]	T[31:0], DRC4 threshold
0xAB	31:0	DRC4_K[25:0]	u[31:26], K4[25:0] DRC4 compression ratio
0xAC	31:0	DRC4_O[25:0]	u[31:26], O4[25:0] DRC4 make up gain
0xA9	31:0	DRC_N_T[31:0]	N_T[31:0] DRC1, 2, 3, 4 noise gate of the DRC

DRC Timing Equation

<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>AA/AE/AD Timing, which is 3.23 format</td><td>Equation : AA = (1-e-1/(ta * fs)) * 223
ta = AA/AD/AE timing,
fs = sampling rate
Ex :ta = 0.1ms, fs = 48K
AA = (1-e-1/(0.0001 * 48000)) * 223 = 1577592
DEC = 1577592
HEX = 0x181278
<table>
<tr><th>Timing</th><th>T_Dec</th><th>T_Hex</th></tr>
<tr><td>0.1ms</td><td>1577592</td><td>0x181278/0067ED88</td></tr>
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<tr><td>400ms</td><td>436</td><td>0x0001B4/007FFE4C</td></tr>
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<tr><td>1-AA/1-AE/1-AD Timing</td><td>Equation: 1-AA = (0x800000-AA timing)
Ex : If AA = 0x000001B4
1-AA = (0x800000-0x000001B4)
HEX = 0x007FFE4C
1-AA/1-AD, must be follow the equations AA + (1-AA) = 1, AD + (1-AD) = 1 for RMS and peak mode.
For peak mode, 1-AE, must be defined by users and there is no limitation.
For RMS mode, 1-AE, must be calculated and follow the equation AE + (1-AE) = 1.</td></tr>
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<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>DRC_T: Threshold</td><td>T is the threshold of the DRC
Equation : T= (Threshold-24) / 6.0206 (dB)
Ex :Threshold = –4.5dB,
(–4.5-24)/6.0206 = –4.733747
T_Dec = –4.733747*2^23 = –39709551
T_Hex = DEC2HEX (–39709551) = 0xFDA21490
<table>
<tr><th>Threshold</th><th>T_Dec</th><th>T_Hex</th></tr>
<tr><td>0dB</td><td>–33439622</td><td>0xFE01C079</td></tr>
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<tr><td>–4.5dB</td><td>–39709551</td><td>0xFDA21490</td></tr>
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<table>
<tr><th>DRC Description</th><th>Equation</th></tr>
<tr><td>DRC_K: Compress ratio</td><td>K is the compression ratio of the DRC
Equation : K = (1/Ratio-1) + 8
EX : Ratio = 8
(1/8-1)+8 = 7.125
K_Dec = 7.125*2^23 = 59768832
K_Hex = DEC2HEX (59768832) = 0x3900000

<table><tr><th>Ratio</th><th>K_Dec</th><th>K_Hex</th></tr><tr><td>Full Comp</td><td>58720256</td><td>0x3800000</td></tr><tr><td>.
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<tr><td>DRC_O: Make up gain</td><td>O is the offset of the DRC
Equation : O = 10(Offset-24)/20
EX : Offset = 0dB
10^(0-24/20) = 0.063095
O_Dec = 0.063095*2^23 = 529285
O_Hex = DEC2HEX (529285) = 0x0081385

<table><tr><th>Offset</th><th>O_Dec</th><th>O_Hex</th></tr><tr><td>0dB</td><td>529285</td><td>0x0081385</td></tr><tr><td>.
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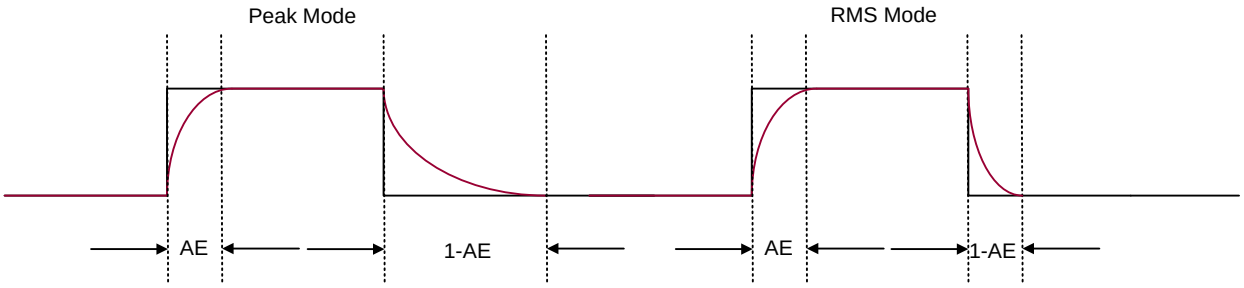
Peak Mode RMS Mode

Block Diagram & Description
→The detecting threshold using different calculated methods. Peak mode: AE and 1-AE is independent RMS mode: AE + (1-AE) = 1 

Address	BITS	Name	Description
0x60	7	DRC4_PEAK	1: Peak mode 0 : RMS mode
	6	DRC3_PEAK	1: Peak mode 0 : RMS mode
	5	DRC2_PEAK	1: Peak mode 0 : RMS mode
	4	DRC1_PEAK	1: Peak mode 0 : RMS mode

DRC Enable

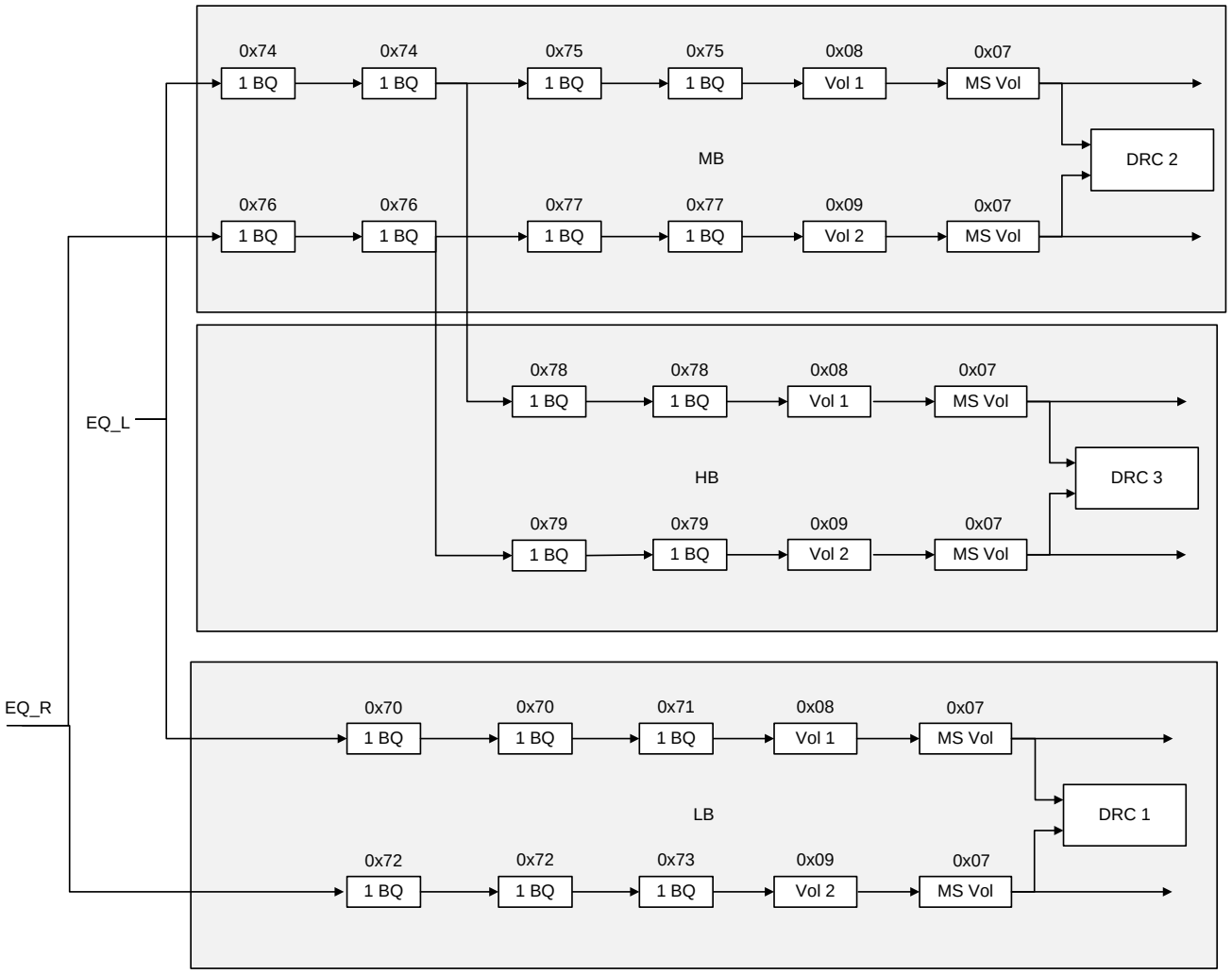
Address	BITS	Name	Description
0x60	3	DRC4_ON	DRC4 Enable (Final DRC) 1 : Enable 0 : Disable, →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC4)
	2	DRC3_ON	DRC3 Enable (H band) 1 : Enable 0 : Disable, →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC3)
	1	DRC2_ON	DRC2 Enable (M band) 1 : Enable 0 : Disable, →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC2)
	0	DRC1_ON	DRC1 Enable (L_band) 1 : Enable 0 : Disable, →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC1)

Multi Band DRC EQ

Block Diagram & Description

→To adjust the cut off frequency of the DRC1, 2, 3

→VOL 1 is 0x08 CH_1 Volume add 0x07 Master Volume, and VOL 2 is 0x09 CH_2 Volume add 0x07 Master Volume



DRC_EQ Link

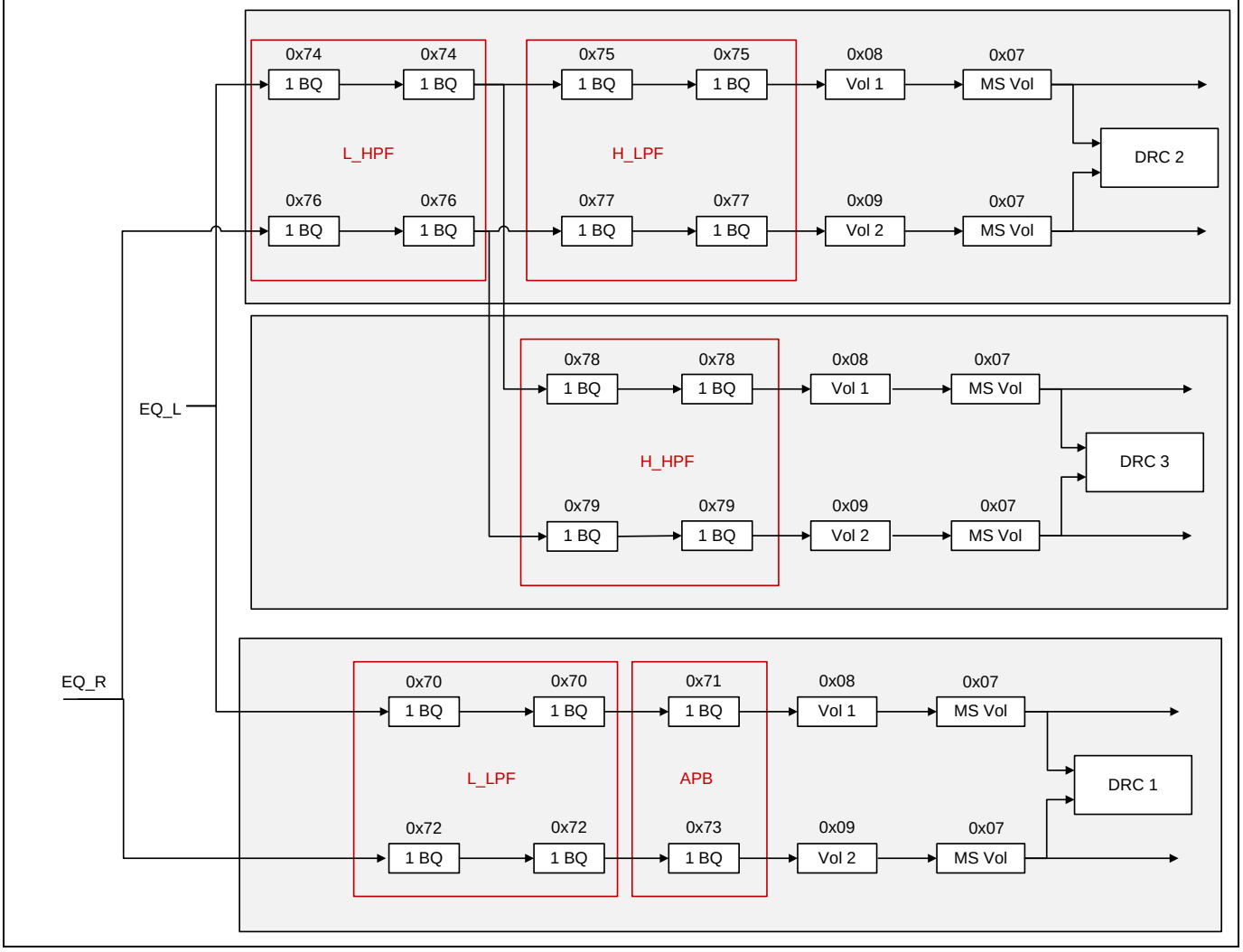
Address	BITS	Name	Description
0x18	4	DRC_EQ_LINK	0: DRC EQ L/R Can be written independently 1 : L and R are ganged for EQ Biquads; a write to left-channel BQ is also written to right-channel BQ. (0x70,0x71 is ganged to 0x72, 0x73.Also 0x74, 0x75 is ganged to 0x76, 0x77)

Address	BITS	Name	Description
0x70	159:128	LB_CH1_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	LB_CH1_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	LB_CH1_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	LB_CH1_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	LB_CH1_bq_1_a2	u[31:26], a2[25:0] u : Unused

Address	BITS	Name	Description
0x79	159:128	HB_CH2_bq_1_b0	u[31:26], b0[25:0] u : Unused
	127:96	HB_CH2_bq_1_b1	u[31:26], b1[25:0] u : Unused
	95:64	HB_CH2_bq_1_b2	u[31:26], b2[25:0] u : Unused
	63:32	HB_CH2_bq_1_a1	u[31:26], a1[25:0] u : Unused
	31:0	HB_CH2_bq_1_a2	u[31:26], a2[25:0] u : Unused

MBDRC First Order Setting

Block Diagram & Description



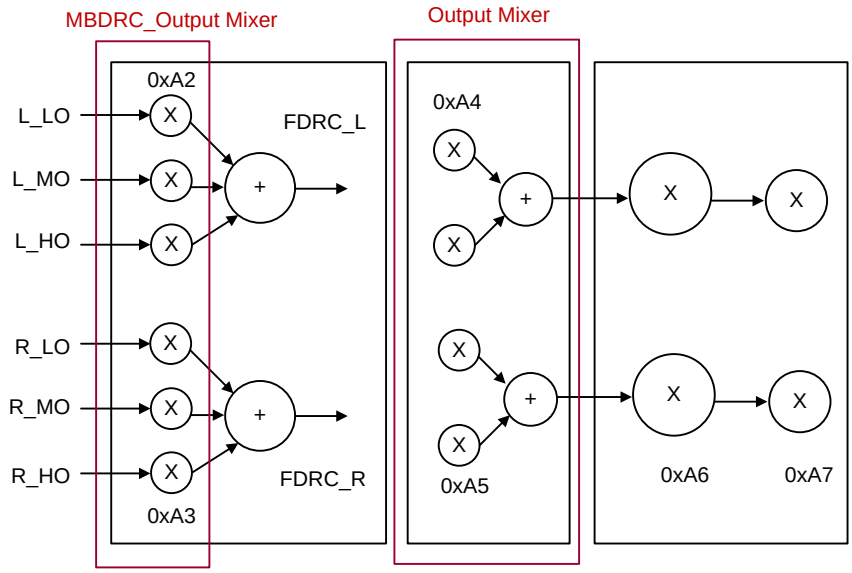
Address	BITS	Name	Description
0x62	7	SKIP_BQ1_L_MBAND	(register 0x74) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	6	SKIP_BQ2_L_MBAND	(register 0x75) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	5	SKIP_BQ1_R_MBAND	(register 0x76) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	4	SKIP_BQ2_R_MBAND	(register 0x77) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	3	SKIP_BQ1_L_HBAND	(register 0x78) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	2	SKIP_BQ1_R_HBAND	(register 0x79) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	1	SKIP_BQ1_L_LBAND	(register 0x70) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped
	0	SKIP_BQ1_R_LBAND	(register 0x72) 0 : Coefficients applied to 2 identical BQ stages 1 : Coefficients applied to 1 stage only, 1 is skipped

DRC Filter Bypass

Address	BITS	Name	Description
0x63	4	SKIP_DRC_L_HPF	L_HPF for MB and HB DRC 0 : Normal Mode 1 : SKIP
	3	SKIP_DRC_H_LPF	H_LPF for MB DRC 0 : Normal Mode 1 : SKIP
	2	SKIP_DRC_H_HPF	H_HPF for HB DRC 0 : Normal Mode 1 : SKIP
	1	SKIP_DRC_L_LPF	L_LPF for LB DRC 0 : Normal Mode 1 : SKIP
	0	SKIP_DRC_APB	APB for LB DRC 0 : Normal Mode 1 : SKIP

MBDRC/Output Mixer

Block Diagram & Description



Address	BITS	Name	Description
0xA2	95:64	CH1_OUT_MIX_L	u[31:26], mix_2[25:0] u : Unused
	63:32	CH1_OUT_MIX_M	u[31:26], mix_1[25:0] u : Unused
	31:0	CH1_OUT_MIX_H	u[31:26], mix_0[25:0] u : Unused
0xA3	95:64	CH2_OUT_MIX_L	u[31:26], mix_2[25:0] u : Unused
	63:32	CH2_OUT_MIX_M	u[31:26], mix_1[25:0] u : Unused
	31:0	CH2_OUT_MIX_H	u[31:26], mix_0[25:0] u : Unused
0xA4	63:32	CH1_OUT_MIX_1	u[31:26], mix_1[25:0] u : Unused
	31:0	CH1_OUT_MIX_0	u[31:26], mix_0[25:0] u : Unused
0xA5	63:32	CH2_OUT_MIX_1	u[31:26], mix_1[25:0] u : Unused
	31:0	CH2_OUT_MIX_0	u[31:26], mix_0[25:0] u : Unused

Output/MBDRC Mixer Gain Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0xA2, 0xA3,
0xA4, 0xA5</td><td>25:0</td><td>mix_2[25:0], mix_1[25:0]
mix_0[25:0]</td><td>Equation : 20Log(Dec/8388608)
Range : 12dB (0X1ffffff) to Mute (0x00000000)
Ex : 6dB, Hex = 0x1000000
Dec = 16777216
Gain = 20Log(16777216/8388608) = 6dB
<table><tr><th>Gain</th><th>Dec</th><th>Hex</th></tr><tr><td>12dB</td><td>33554431</td><td>0X1FFFFFF</td></tr><tr><td>6dB</td><td>16777216</td><td>0X1000000</td></tr><tr><td>.
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</table>

Mixer Inverse Phase Setting

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0xA2, 0xA3,
0xA4, 0xA5</td><td>25:0</td><td>bit25 is sign bit, 3.23 format.</td><td>Equation : Hex = DEC2HEX
Ex : Gain = 6dB,
Hex = 0x1000000
Phase Inverse : Hex = DEC2HEX(-16777216) = 0xFF000000
<table><tr><th>Inverse</th><th>Dec</th><th>Hex</th></tr><tr><td>12dB</td><td>–33554431</td><td>0XFE000001</td></tr><tr><td>6dB</td><td>–16777216</td><td>0XFF000000</td></tr><tr><td>.
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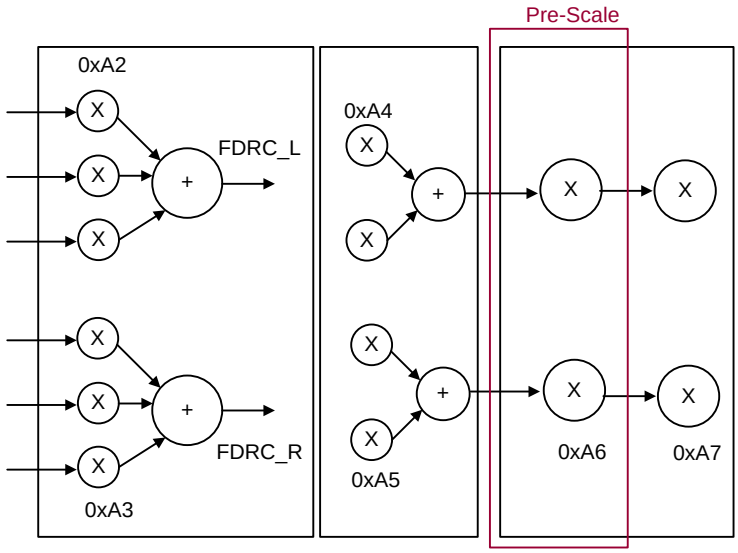
</table>

Pre-Scale

Block Diagram & Description
→The gain stage after mixer output

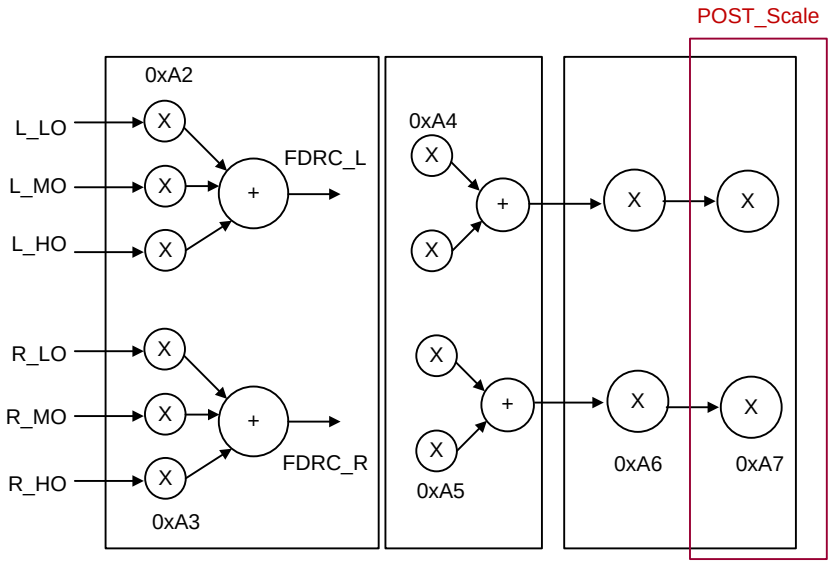


Address	BITS	Name	Equation
0xA6	31:0	PRE_SCALE, u[31:26], pre[25:0], 9.17 format Bit 25 is sign bit.	Equation : 20Log(Dec/131072) Range : 48dB (0X01ffffff) to Mute (0x00000000) Ex : 48dB, Hex = 0x01ffffff Dec = 33554431 Gain = 20Log(33554431/131072) = 48dB

Gain	Dec	Hex
48dB	33554431	0x01ffffff
20dB	1310720	0X140000
. . .	. . .	. . .
10dB	414187	0x651EB
. . .	. . .	. . .

Post-Scale

Block Diagram & Description
→The gain stage after pre-scale output



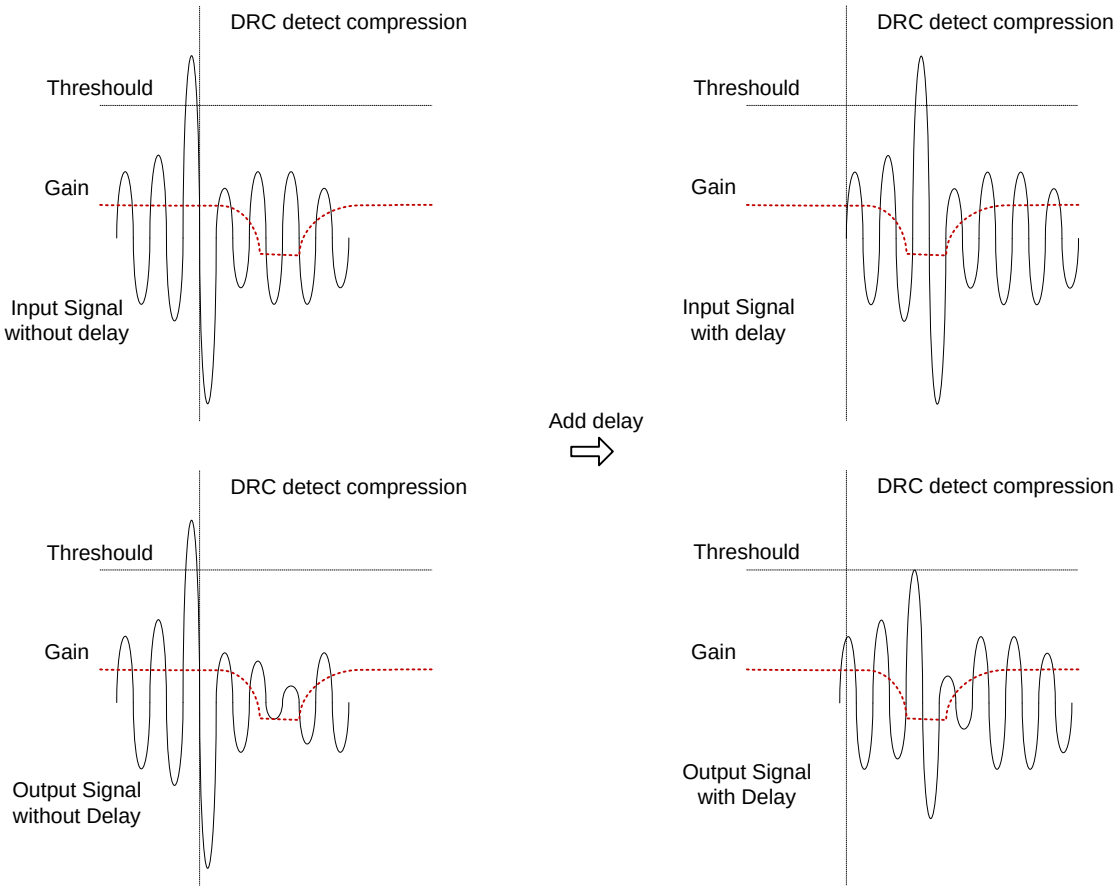
Address	BITS	Name	Equation
0xA7	31:0	POST_SCALE, 3.23 format, u[31:26], post[25:0] Bit 25 is sign bit.	Equation : 20Log(Dec/8388608) Range : 12dB (0X01ffffff) to Mute (0x00000000) Ex : 9.5dB, Hex = 0x01800000 Dec = 25165824 Gain = 20Log(25165824/8388608) = 9.5dB

Gain	Dec	Hex
12dB	33554431	0x01ffffff
. . .	. . .	. . .
6dB	16777216	0x01000000
. . .	. . .	. . .

DRC4 is final stage of DRC. It can be configure as the final DRC to limit the output power.

Block Diagram & Description

→ Make the audio output signal lately. Maximum value is 0x8F

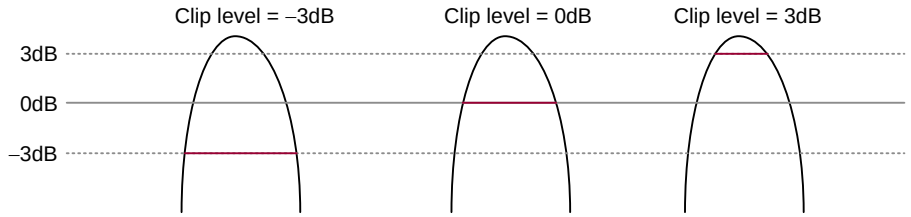


Delay = (DRC4_Delay)*1/Sample rate

Address	BITS	Name	Description
0xA8	7:0	DRC4_DELAY[7:0]	DRC4_DELAY ->The delay make the audio signal output delay ->Delay = (DRC4_DELAY)*1/sample rate ->This maximum value is 0x8F, if the setting is larger than 0x8F, it will limit at 0x8F

Hard Clip Function

To clip the signal with different threshold, operate in time domain.

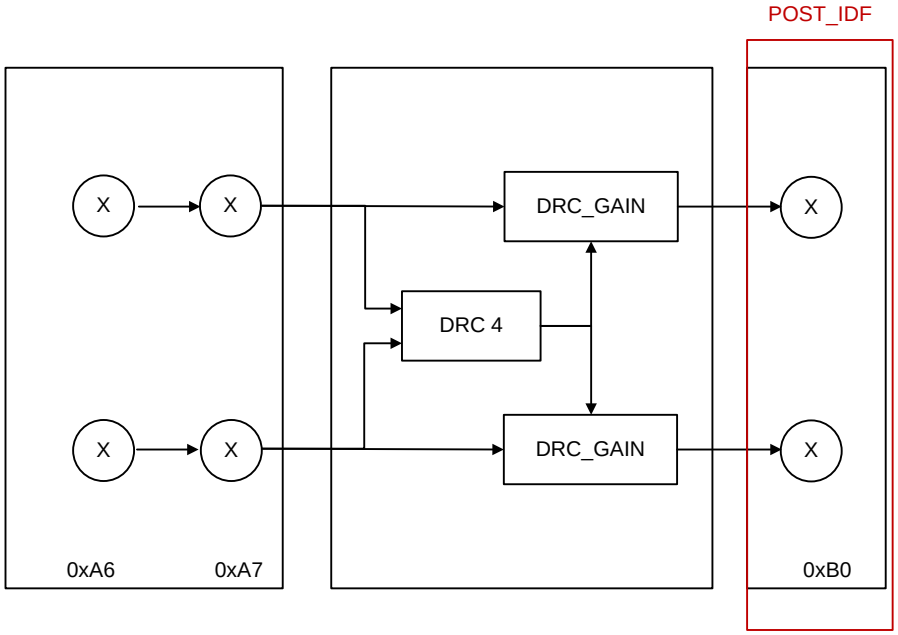


Address	BITS	Name	Description
0xB0	31	HARD_CLIP_EN	1 : Enable hard clip 0 : Disable hard clip
	30	DF_CLIP_EN	1 : Enable digital filter clip 0 : Disable digital filter clip
	18:8	HARD_CLIP_TH[10:0]	Hard Clip Threshold for Hard clip & Final Hard Clip 11'h000 : 24dB 11'h180 : 0dB 0.0625db per step

POST_IDF

Block Diagram & Description

→The gain stage after DRC 4



POST_IDF Gain

<table>
<tr><th>Address</th><th>BITS</th><th>Name</th><th>Equation</th></tr>
<tr><td>0xB0</td><td>7:0</td><td>POST_IDF[7:0]</td><td>Equation: 20Log(Dec/128)
Range : 6dB (0xFF) to Mute (0x00)
Ex : 6dB, Hex = 0xFF
Dec = 255
Gain = 20Log(255/128) = 6dB
<table>
<tr><th>Gain</th><th>Dec</th><th>Hex</th></tr>
<tr><td>6dB</td><td>255</td><td>0xFF</td></tr>
<tr><td>5dB</td><td>226</td><td>0XE2</td></tr>
<tr><td>.
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<tr><td>0dB</td><td>128</td><td>0x80</td></tr>
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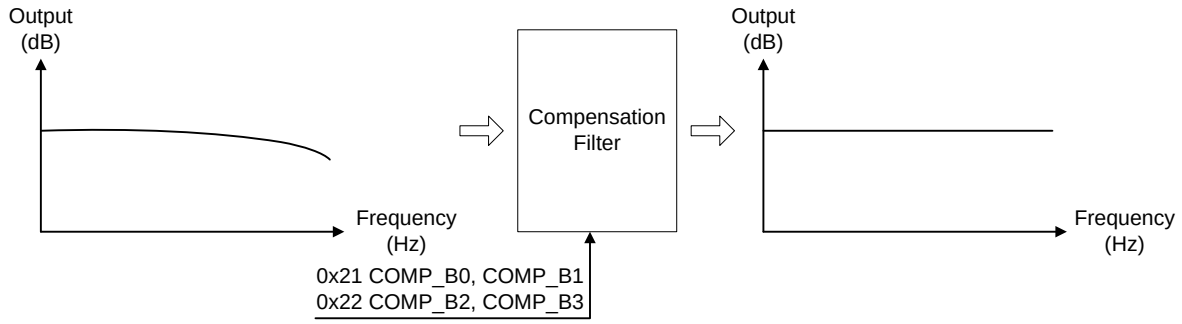
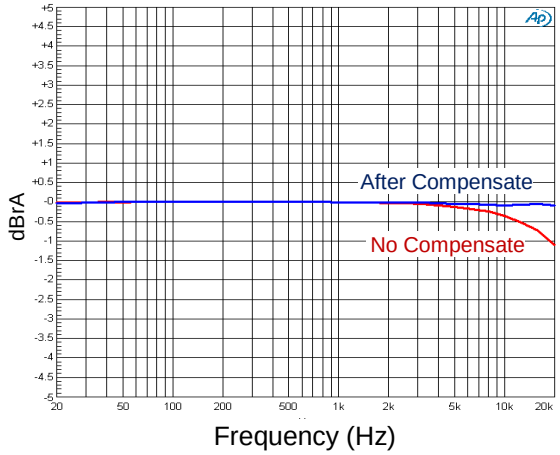
Compensate Filter

Compensation filter is purpose to compensate internal gain from DAC, this filter can also compensate the frequency response affected by LC filter, recommended setting will based on different application circuit to fit the curve



Compensate Description	Equation
Compensate	y[n]=B3*x[n-6]+B2*x[n-5]+B1*x[n-4]+B0*x[n-3]+B1*x[n-2]+B2*x[n-1]+B3*x[n] B0, B1, B2, B3: Compensate coefficient N: Input Signal when applied

Address	BITS	Name	Description
0x0C	4	COMP_EN	1 : Compensation filter enable 0 : Compensation filter disable
0xB1	31:16	COMP_B0[15:0]	Compensate B0, B1 coefficient
	15:11	Reserved	
	10:0	COMP_B1[10:0]	
0xB2	31:8	Reserved	Compensate B2, B3 coefficient
	26:16	COMP_B2[10:0]	
	15:9	Reserved	
	8:0	COMP_B3[8:0]	



Application Information

I²C Bus Specification

The RT9119 supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9119 is always a slave device in all of its communications. It can operate at up to 400kb/s. The RT9119 I²C interface is a slave only interface.

Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9119 and the bus master. During the data input, the RT9119 samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

Device Addressing

The RT9119 Support I²C Control interface. The default device address is 0011011 when A_SEL = High or 0011010 when A_SEL = Low. A_SEL will latch from the power on or software reset, then define the address depends on the low, or high.

A_SEL	Device Address
High	0011011
Low	0011010

I²C Write Control

Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9119 acknowledges this and the writes for the byte of internal address. After receiving the internal byte address, the RT9119 again responds with an acknowledgement.

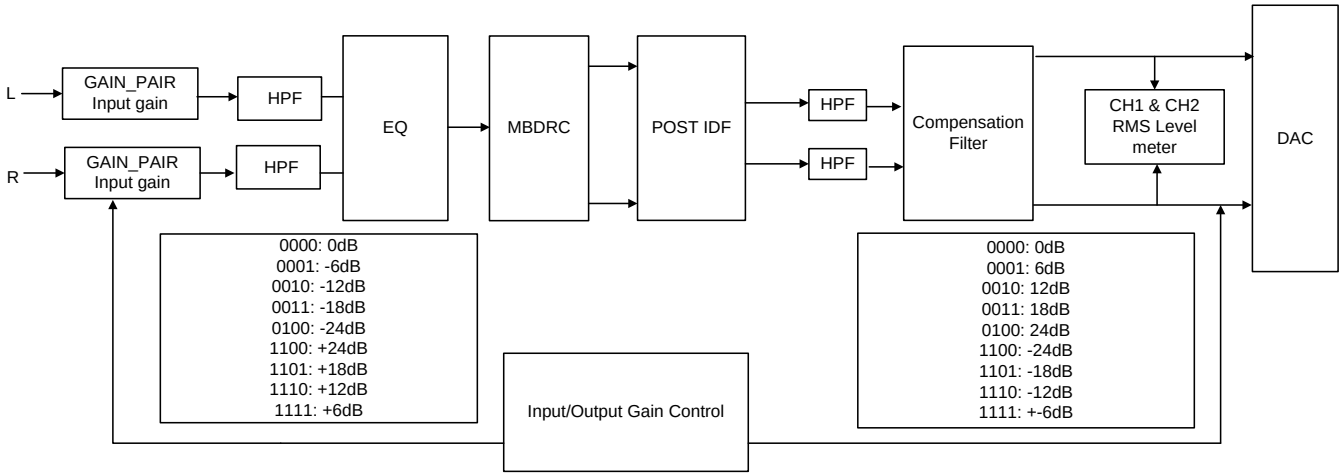
I²C Read Control

Following the START condition the master sends a device select code with the RW bit set to 1. The RT9119 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

Input / Output gain Control

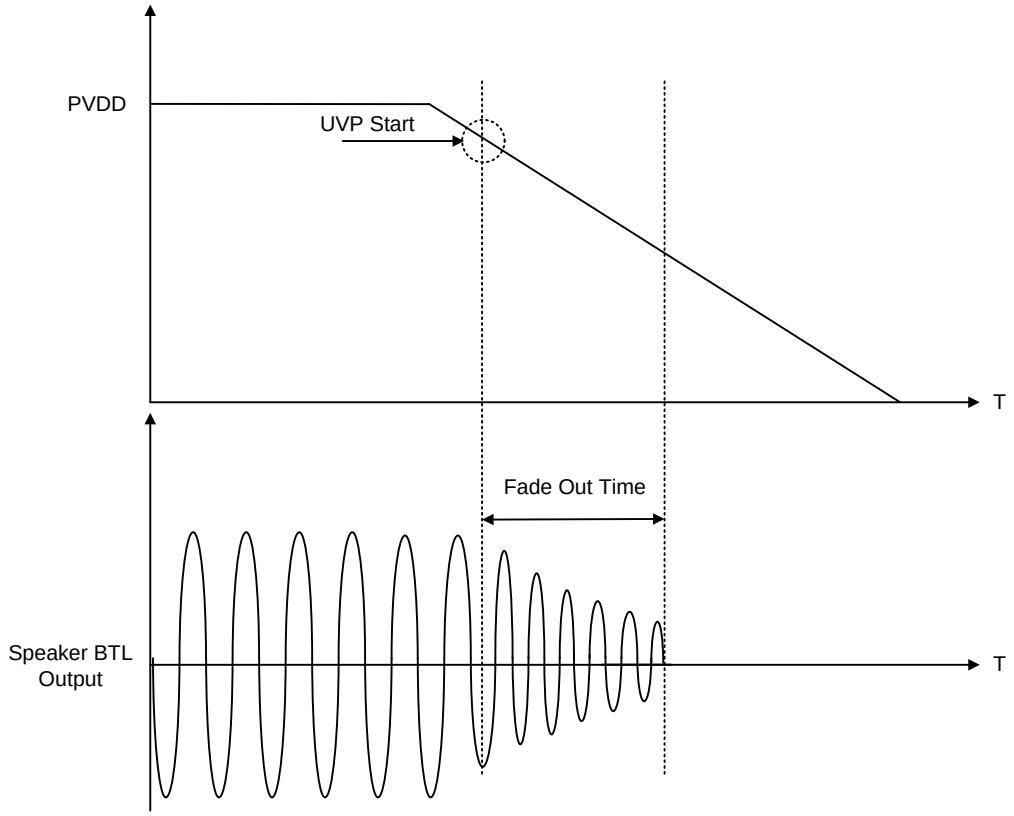
Block Diagram & Description

→ For increase Dynamic range in signal processing, gain pair control decrease gain in the initial of signal path. (0dB/-6dB/-12dB/-18dB/-24dB), and at the end of signal processing, gain pair control return the decrease gain. (0dB/6dB/12dB/18dB/24dB)



Address	BITS	Name	Description
0xBB	4	Final_Gain	Final gain after Hard clip 0 : 0dB 1 : 6dB
	3:0	GAIN_PAIR_CTRL	input decrease and output increase gain control, for increase DSP dynamic range 0000: 0dB/0dB 0001 : –6dB/6dB 0010 : –12dB/12dB 0011 : –18dB/18dB 0100 : –24dB/24dB 1100 : +24dB/–24dB 1101 : +18dB/–18dB 1110 : +12dB/–12dB 1111 : +6dB/-6dB Others : 0db/0db

UVP Speaker Fade Out Function

Block Diagram & Description
UVP voltage selection for PVDD The UVP voltage can programmable. Once PVDD voltage drops below the preset value, the RT9119 will ramp down signal to turn off the speaker    Noted : There are no relation between the VOL_RAMP and UVP RAMP.

Address	BITS	Name	Description
0xD9	7	D_UV_RAMP_DOWN	SPK UV protection behavior 0 : HZ_PROT directly 1 : Power off sequence
	6:4	D_UVP_PVDD_SEL[2:0]	Select UVP level for PVDD power domain 3'b011 : 9.5V, 3'b100 : 10.9V, 3'b101 : 12.7V, 3'b110 : 15.4V, 3'b111 : 19.8V
	3	UV_RAMP_DOWN_SEL	0: Ramp down time related with sampling rate and master volume. 2 sample with 9 volume step. (1 sample with 4 step and 1 sample with 5 steps. From 0x180 to mute (0x7FF) with 48k sampling rate is ((0x7FF-0x180)/9) * (2/48k) = 7.7ms 1 : Ramp down time related with POST_IDF only. Ramp down 1 POST_IDF step every 10.4μs. From 0x80 to mute (0x00) is (0x80 - 0x00) * 10.4μs = 1.33ms. Recommend use UV_RAMP_DOWN_SEL = 1 to provide faster ramp down time to reduce pop sound when PVDD drop too fast

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-28L 4x5 package, the thermal resistance, θ_{JA}, is 27.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (150°C - 25°C) / (27.4°C/W) = 4.56W for a VQFN-28L 4x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

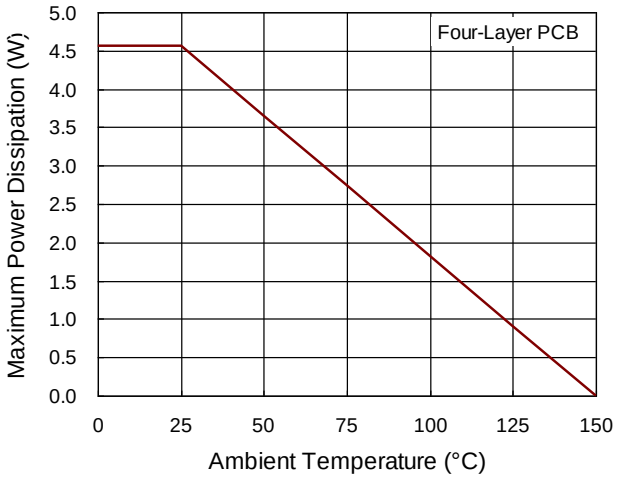
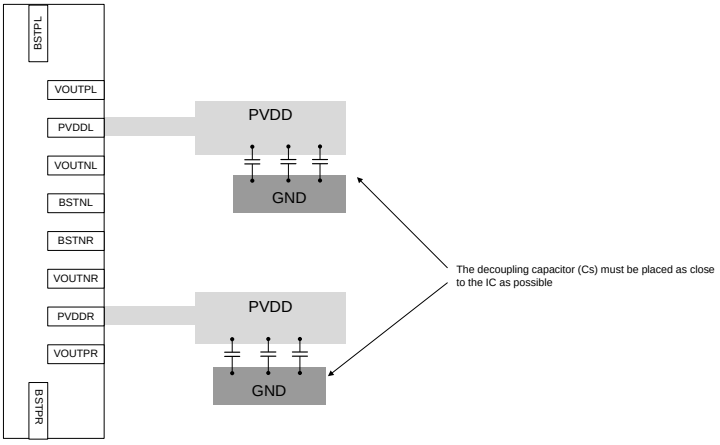


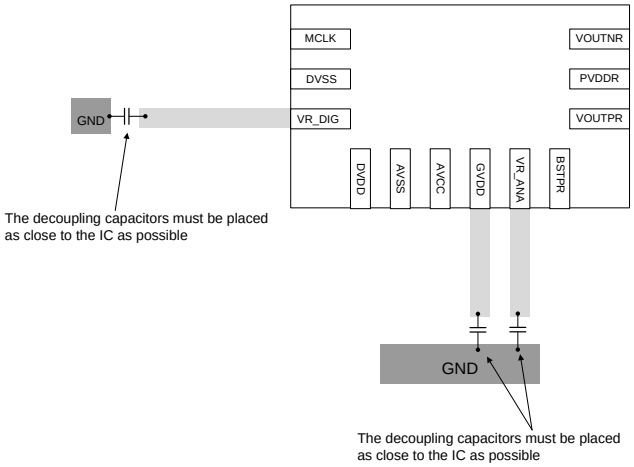
Figure 1. Derating Curve of Maximum Power Dissipation

Layout Guide

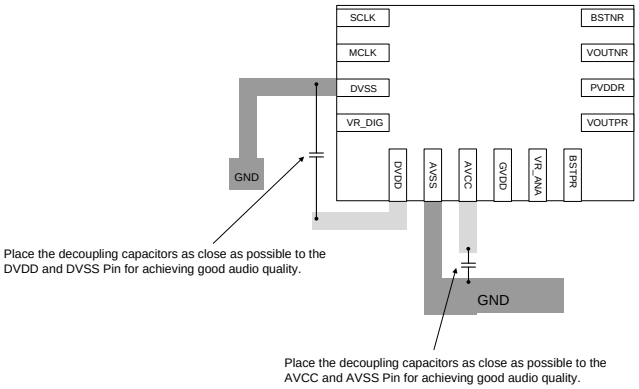
Place the decoupling capacitors as close as possible to the PVCC and GND, then use shortest trace to link these capacitors, and use more vias for GND link to GND layer to reduce parasitic inductance and resistance. The trace width is 30 mil at least.



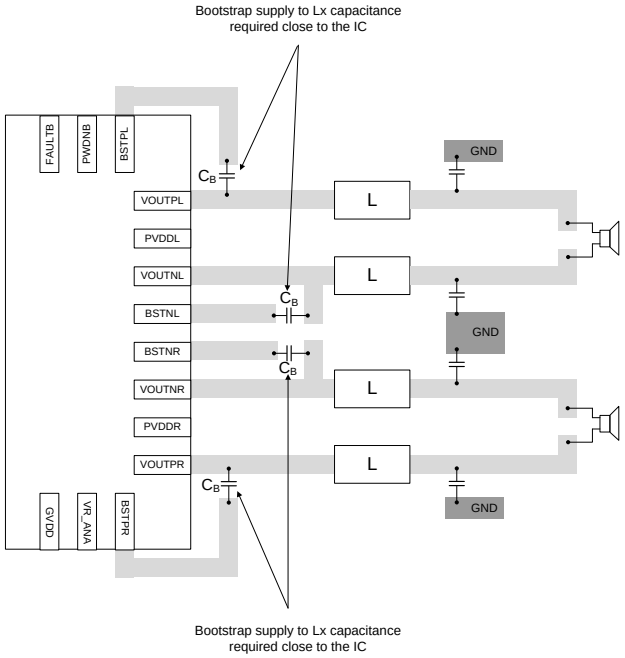
The VR_DIG VR_ANA and GVDD decoupling capacitors must be placed as close to the IC as possible.



Place the decoupling capacitors as close as possible to the DVDD and DVSS Pin, AVCC and AVSS Pin for achieving good audio quality, the trace width of DVDD is 6 mil at least and the trace width of AVCC is 30mil at least



The traces of VOUTPL VOUTNL VOUTPR and VOUTNR should be kept equal width and length respectively, and Bootstrap supply to Lx capacitance required close to the IC.



If possible, coplanar ground fill on both sides for differential pair of speaker out shielding

Register Map

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x00	1	I2S_FMT_RPT	7:5	R	SR_MODE[2:0]	Sampling Rate report 000 : 32kHz 001 : Reserved 010 : 88.2/96kHz 011 : 44.1/48kHz 100 : 16kHz 101 : 22.05/24kHz 110 : 8kHz 111 : 11.025/12kHz	3'b011
			4:2	R	CK_MODE[2:0]	Clock Mode report 000 : MCLK = 64fs 001 : MCLK = 128fs 010 : MCLK = 192fs 011 : MCLK = 256fs 100 : MCLK = 384fs 101 : MCLK = 512fs Others : Reserved	3'b011
			1:0	R	BCK_MODE[1:0]	BCK mode report 00 : BCK = 32fs 01 : BCK = 48fs 10 : BCK = 64fs Others : Reserved	2'b10
0x01	1	DEV_ID	7:0	R	DEVICE_ID[7:0]		8'h20
0x02	1	I2S_FMT	7	R/W	SR_MODE_SEL	0: Auto detection (default) 1: Manual	0
			6:4	R	Reserved	Reserved	3'b000
			3:0	R/W	AUD_MODE	0000 : 16bits right justify 0001 : 20bits right justify 0010 : 24bits right justify 0011 : 32bits right justify 0100 : 16bits I^2S 0101 : 20bits I^2S (default) 0110 : 24bits I^2S 0111 : 32bits I^2S 1000 : 16bits left justify 1001 : 20bits left justify 1010 : 24bits left justify 1011 : 32bits left justify Others : No define	4'b0101

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x03	1	ERR_RPT	7	R	DC_FLAG	DC Flag report 0: No DC error 1 : DC	0
			6	R/W	MCLK_ERR	0: No MCLK error (default) 1: MCLK error, write 0 to clear flag	0
			5	R/W	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag	0
			4	R/W	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag	0
			3	R/W	OC_ERROR	0: No OC error(default) 1: OC, write 0 to clear flag	0
			2	R/W	OV_ERROR	0: No OV error(default) 1 : OV, write 0 to clear flag	0
			1	R/W	OT_ERROR	0: No OT error(default) 1: OT, write 0 to clear flag	0
			0	R/W	UV_ERROR	0: No UV error(default) 1 : UV, write 0 to clear flag	0
0x04	1	ERR_MASK	7	R	Reserved	Reserved	0
			6	R/W	MCLK_ERROR_mask	Fault mask for 0x03 MCLK error 0 : Not mask 1 : Mask (default)	1
			5	R/W	SCLK_ERROR_mask	Fault mask for 0x03 SCLK error 0 : Not mask 1 : Mask (default)	1
			4	R/W	LRCK_ERROR_mask	Fault mask for 0x03 LRCK error 0 : Not mask 1 : Mask (default)	1
			3	R/W	OC_ERROR_mask	Fault mask for 0x03 OC error 0 : Not mask (default) 1 : Mask	0
			2	R/W	OV_ERROR_mask	Fault mask for 0x03 OV error 0 : Not mask (default) 1 : Mask	0
			1	R/W	OT_ERROR_mask	Fault mask for 0x03 OT error 0 : Not mask (default) 1 : Mask	0
			0	R/W	UV_ERROR_mask	Fault mask for 0x03 UV error 0 : Not mask (default) 1 : Mask	0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x05	1	SYS_CTL	7	R	Reserved	Reserved	0
			6	R/W	SHUDOWN	0 : Turn on 1 : Shutdown (default)	1
			5	R/W	D_PBTL	0 : BTL (default) 1 : PBTL	0
			4	R/W	D_SPK_VT_FREQ	PWM switching frequency 0: 400kHz (default) 1: 800kHz	0
			3	R/W	DIS_A_SEL_PU	Disable A_SEL pin pull up 0 : Enable (default) 1 : Disable	0
			2	R/W	dSR_DIV_SEL	0: Auto parameter for PLL (default) 1 : According to 0xC4 setting	0
			1	R/W	MS_EN	0 : Slave mode (default) 1 : Master mode	0
			0	R/W	dREF_SEL	0: MCLK 1 : SCLK (default) PS : If Master mode, PLL always reference MCLK.	1
0x06	1	ERR_TYPE	7	R	Reserved	Reserved	0
			6	R/W	MCLK_ERROR _FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (default) 1 : Latch	0
			5	R/W	SCLK_ERROR _FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (default) 1 : Latch	0
			4	R/W	LRCK_ERROR _FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (default) 1 : Latch	0
			3	R/W	OC_ERROR _FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (default) 1 : Latch Noted : Select 1	0
			2	R/W	OV_ERROR _FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (default) 1 : Latch	0
			1	R/W	OT_ERROR _FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (default) 1 : Latch	0
			0	R/W	UV_ERROR _FAULT_TYPE	Fault behavior type select. 0 : Auto recovery (default) 1 : Latch	0
0x07	2	MS_VOL	15:11	R	Reserved	Reserved	5'h0
			10:0	R/W	MS_VOL[10:0]	Master Volume control 11'h000 : 24dB 11'h180 : 0dB 11'h7FF : Mute (default) 0.0625dB per step	11'h7FF

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x08	2	CH1_VOL	15:11	R	Reserved	Reserved	5'h0
			10:0	R/W	CH1_VOL[10:0]	CH1 Volume control 11'h000 : 24dB 11'h180 : 0Db (default) 11'h7FF : Mute 0.0625dB per step	11'h180
0x09	2	CH2_VOL	15:11	R	Reserved	Reserved	5'h0
			10:0	R/W	CH2_VOL[10:0]	CH2 Volume control 11'h000 : 24dB 11'h180 : 0Db (default) 11'h7FF : Mute 0.0625dB per step	11'h180
0x0A	1	VOL_RAMP	7	R/W	CH2_MUTE	0 : CH2 un-mute (default) 1 : CH2 soft mute	0
			6	R/W	CH1_MUTE	0 : CH1 un-mute(default) 1 : CH1 soft mute	0
			5:4	R	Reserved	Reserved	2'b00
			3	R/W	SKIP_RAMP	0 : No skip volume ramp (default) 1 : Skip volume ramp	0
			2:0	R/W	VOL_RAMP_MODE[1:0]	Volume Slew step control 000 : 1 step in every sample 001 : mute -> –40dB, every sample with1 step. –40dB -> 24dB, 2 sample with 1 step. 010 : mute -> –40dB, 2 sample with 1 step. –40dB -> 24dB, 4 sample with 1 step. (default) Others : Mute -> –40dB, 4 sample with 1 step. –40dB -> 24dB, 8 sample with 1 step.	3'b001
0x0B	1	AUTO_RCVRY	7:4	R	Reserved	Reserved	4'b0000
			3:0	R/W	BKD_TIME[3:0]	Power Stage auto recovery time 0000 : 107ms 0001 : 179ms 0010 : 299ms (default) 0011 : 449ms 0100 : 598ms 0101 : 748ms 0110 : 898ms 0111 : 1047ms 1000 : 1197ms 1001 : 1346ms Others : 1496ms	4'b0010

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x0C	1	FLTR_MISC	7	R/W	HPF_EN	0 : High-Pass filter disable 1 : High-Pass filter enable (default)	1
			6	R/W	HPF_POS_EN	0: Post high Pass filter disable (default) 1 : Post high Pass filter enable	0
			5	R/W	Reserved	Reserved	0
			4	R/W	COMP_EN	0 : Compensation filter disable (default) 1 : Compensation filter enable	0
			3	R/W	Reserved	Reserved	0
			2	R/W	FIR_EN	FIR filter enable 0 : Disable (default) 1 : Enable	0
			1	R/W	SRC_RES_SEL	Resolution select for SRC part 0 : 24-bit 1 : 32-bit (default)	1
			0	R/W	REG_PAGE_SEL	Register page select 0 : Default page (default) 1 : FIR coefficients page For FIR page, register 0x20 to 0x9F are 128 coefficients, L/R are the same. Each coefficient is 4-byte, 3.23 format	0
0x0D	1	SDIO_SEL	7	R	Reserved	Reserved	0
			6:4	R/W	SDO_SEL[2:0]	**000 : No output (default)** 001 : Interface output 010 : FIR output 011 : EQ output 100 : SBQ output 101 : DRC/Mixer/Gain output 110 : Final output 111 : RMS output	3'b000
			3:2	R/W	CH1_SI[1:0]	00 : SDIN-L to CH1 (default) 01 : SDIN-R to CH1 1X : 0 to CH1	2'b00
			1:0	R/W	CH2_SI[1:0]	00 : SDIN-L to CH2 01 : SDIN-R to CH2 (default) 1X : 0 to CH2	2'b01
0x0E	1	SPK_GAIN	7:3	R	Reserved	Reserved	5'b00000
			2:0	R/W	D_SPK_GAIN[2:0]	Class D output gain 001 : 3.5x 010 : 4x 011 : 4.5x (default) 100 : 5x 101 : 5.5x 110 : 6.15x 111 : 8x	3'b011

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x0F	1	INTER_PWR_CTRL	7	R/W	D_LPFR_EN	Enable DAC RCH LPF 0 : Disable 1 : Enable (default)	1
			6	R/W	D_LPFL_EN	Enable DAC LCH LPF 0 : Disable 1 : Enable (default)	1
			5	R/W	D_EN_RCH_PWR	RCH PWR stage enable 0 : Disable 1 : Enable (default)	1
			4	R/W	D_EN_LCH_PWR	LCH PWR stage enable 0 : Disable 1 : Enable (default)	1
			3	R/W	D_DAC_RCH_EN	Enable DAC_RCH 0 : Disable 1 : Enable (default)	1
			2	R/W	D_DAC_LCH_EN	Enable DAC LCH 0 : Disable 1 : Enable (default)	1
			1	R/W	D_SPK_RCH_EN	Enable Class D RCH SPK 0 : Disable 1 : Enable (default)	1
			0	R/W	D_SPK_LCH_EN	Enable Class D LCH SPK 0 : Disable 1 : Enable (default)	1
0x10	1	DC_PROT	7:6	R	Reserved	Reserved	2'b00
			5:4	R/W	DC_TH[1:0]	DC threshold for DC detection 00 : No available **01 : 12.5%** **10 : 18.75% (default)** 11 : 25%	2'b10
			3	R/W	DC_TEST	Short time check mode 0 : Normal mode (default) 1 : Short time mode	0
			2	R/W	Reserved	Reserved	0
			1	R/W	DC_TIME_SEL	Detection time 0 : 342ms (default) 1 : 684ms	0
			0	R/W	DC_EN	0 : DC protection disable (default) 1 : DC protection enable	0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x11	1	PWM_SS_OPT	7	R/W	D_FSS_EN	Spread spectrum enable 0 : Disable 1 : Enable (default)	0
			6	R/W	PWM_MODEWHITE	Noise select 0 : Pink noise (default) 1 : White noise	0
			5	R/W	PWM_SELCOEF	Pink noise coefficient 0 : 1/2 (default) 1 : 1/4 This will affect the noise amplitude for spread spectrum signal, not recommended to modify it.	0
			4	R/W	PWM_NOISE_EN	Add noise to TRI_GEN 0 : Disable 1 : Enable (default)	0
			3:2	R/W	D_NOISE_AMP[1:0]	Nosie amplitude for SSC 00 : 5kHz (default) 01 :10kHz 10 : 15kHz 11 : 20kHz	2'b00
			1:0	R/W	D_FSS_AMP[1:0]	Spread spectrum frequency variation amplitude 00 : 20kHz 01 : 40kHz (default) 10 : 40kHz 11 : 60kHz	2'b01
0x12	8	CH1_IN_MIX	63:32	R/W	CH1_IN_MIX_1	u[31:26], mix_1[25:0]	0x00800000
			31:0	R/W	CH1_IN_MIX_0	u[31:26], mix_0[25:0]	0x00000000
0x13	8	CH2_IN_MIX	63:32	R/W	CH2_IN_MIX_1	u[31:26], mix_1[25:0]	0x00000000
			31:0	R/W	CH2_IN_MIX_0	u[31:26], mix_0[25:0]	0x00800000
0x14	4	EQ_BOOST_L	31:0	R/W	EQ_CH1_GAIN_BOOST[17:0]	u[31:18], Control L(CH1) channel BQ1 to BQ18 gain boost 0 : 0dB gain 1 : Bi-Quad result add 18dB gain	32'h0
0x15	4	EQ_BOOST_R	31:0	R/W	EQ_CH2_GAIN_BOOST[17:0]	u[31:18], Control R(CH2) channel BQ1 to BQ18 gain boost 0 : 0dB gain 1 : Bi-Quad result add 18dB gain	32'h0
0x16	4	EQ_BYPASS_L	31:0	R/W	EQ_CH1_BYPASS[17:0]	u[31:18],EQ Bypass Control. For CH1 BQ1 to BQ18 is [0:17] 0 : By pass 1 : No by pass.	32'h0
0x17	4	EQ_BYPASS_R	31:0	R/W	EQ_CH2_BYPASS[17:0]	u[31:18], EQ Bypass Control. For CH2 BQ1 to BQ18 is [0:17] 0 : By pass 1 : No by pass.	32'h0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x18	1	EQ_CTRL	7:5	R	Reserved	Reserved	3'b000
			4	R/W	DRC_EQ_LINK	0: DRC EQ L/R can be written **independently**.(default) 1 : L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (0x70, 0x71 is ganged to 0x72, 0x73.Also 0x74, 0x75 is ganged to 0x76, 0x77)	0
			3	R/W	EQ_LINK	0 : L/R can be written **independently** (default) 1 : L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (CH1 & CH2 BQ1 to BQ12 and SBQ13 to SBQ18 are linked together)	0
			2:1	R/W	EQ_PART_LINK[1:0]	Partial link select, when bit 3 EQ_LINK = 1 00 : Link ALL (default) x1 : Link CH1 & CH2 BQ7 to BQ12 1x : Link CH1 & CH2 BQ13 to BQ18 (smooth BQ)	2'b00
			0	R/W	EQ_DISABLE	0 : EQ enable (default) 1 : EQ disable	0
0x19	4	SMOOTH_BQ_ALPHA	31:0	R/W	SMOOTH_BQ_AS	u[31:26], ae[25:0] Alpha filter coefficient for smoothing	32'h00800000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x1A	4	SMOOTH_BQ_CTRL	31:16	R	Reserved	Reserved	16'h0
			15:8	R/W	SMOOTH_BQ_TS[7:0]	After triggering coefficients update, smooth BQ delay in samples. After this delay, old coefficients are disabled. 4 to 1024 samples delay, 4 samples per step	8'h0
			7:4	R/W	Reserved	Reserved	4'b0000
			3	R/W	SMOOTH_METHOD	Smooth method selection: 0 : By alpha filter (controlled by AS) (default) 1 : By linear gain, controlled by TS, but only power of 2 is effective When 2N+1 > TS ≥ 2N, 2N steps is selected	0
			2	R	SMOOTH_DONE	Report status of smooth transition (after TS) 0 : Busy 1 : Done (default)	1
			1:0	R/W	SBQ_UPDATE[1:0]	Trigger smooth BQ coefficients update : When non-zero value is written, smooth transition is triggered. After transition is done, this register automatically goes back to 00. Before transition done, any new write to this register is invalid 00 : No update (default) 01 : SBQ_BK1 to SBQ13, SBQ_BK2 to SBQ14 10 : SBQ_BK1 to SBQ15, SBQ_BK2 to SBQ16 11 : SBQ_BK1 to SBQ17, SBQ_BK2 to SBQ18	2'b00
0x20	20	CH1_BQ1	159:128	R/W	CH1_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x21	20	CH1_BQ2	159:128	R/W	CH1_bq_2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_2_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x22	20	CH1_BQ3	159:128	R/W	CH1_bq_3_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_3_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_3_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_3_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_3_a2	u[31:26], a2[25:0]	32'h00000000
0x23	20	CH1_BQ4	159:128	R/W	CH1_bq_4_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_4_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_4_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_4_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_4_a2	u[31:26], a2[25:0]	32'h00000000
0x24	20	CH1_BQ5	159:128	R/W	CH1_bq_5_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_5_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_5_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_5_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_5_a2	u[31:26], a2[25:0]	32'h00000000
0x25	20	CH1_BQ6	159:128	R/W	CH1_bq_6_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_6_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_6_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_6_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_6_a2	u[31:26], a2[25:0]	32'h00000000
0x26	20	CH1_BQ7	159:128	R/W	CH1_bq_7_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_7_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_7_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_7_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_7_a2	u[31:26], a2[25:0]	32'h00000000
0x27	20	CH1_BQ8	159:128	R/W	CH1_bq_8_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_8_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_8_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_8_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_8_a2	u[31:26], a2[25:0]	32'h00000000
0x28	20	CH1_BQ9	159:128	R/W	CH1_bq_9_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_9_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_9_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_9_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_9_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x29	20	CH1_BQ10	159:128	R/W	CH1_bq_10_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_10_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_10_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_10_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_10_a2	u[31:26], a2[25:0]	32'h00000000
0x2A	20	CH1_BQ11	159:128	R/W	CH1_bq_11_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_11_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_11_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_11_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_11_a2	u[31:26], a2[25:0]	32'h00000000
0x2B	20	CH1_BQ12	159:128	R/W	CH1_bq_12_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_bq_12_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_bq_12_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_bq_12_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_bq_12_a2	u[31:26], a2[25:0]	32'h00000000
0x2C	20	CH1_SBQ13	159:128	R/W	CH1_sbq_13_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_13_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_13_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_13_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_13_a2	u[31:26], a2[25:0]	32'h00000000
0x2D	20	CH1_SBQ14	159:128	R/W	CH1_sbq_14_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_14_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_14_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_14_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_14_a2	u[31:26], a2[25:0]	32'h00000000
0x2E	20	CH1_SBQ15	159:128	R/W	CH1_sbq_15_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_15_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_15_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_15_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_15_a2	u[31:26], a2[25:0]	32'h00000000
0x2F	20	CH1_SBQ16	159:128	R/W	CH1_sbq_16_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_16_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_16_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_16_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_16_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x30	20	CH1_SBQ17	159:128	R/W	CH1_sbq_17_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_17_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_17_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_17_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_17_a2	u[31:26], a2[25:0]	32'h00000000
0x31	20	CH1_SBQ18	159:128	R/W	CH1_sbq_18_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_18_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_18_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_18_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_18_a2	u[31:26], a2[25:0]	32'h00000000
0x32	20	CH1_SBQ_BK1	159:128	R/W	CH1_sbq_bk1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_bk1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_bk1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_bk1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_bk1_a2	u[31:26], a2[25:0]	32'h00000000
0x33	20	CH1_SBQ_BK2	159:128	R/W	CH1_sbq_bk2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH1_sbq_bk2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH1_sbq_bk2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH1_sbq_bk2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH1_sbq_bk2_a2	u[31:26], a2[25:0]	32'h00000000
0x40	20	CH2_BQ1	159:128	R/W	CH2_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x41	20	CH2_BQ2	159:128	R/W	CH2_bq_2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0x42	20	CH2_BQ3	159:128	R/W	CH2_bq_3_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_3_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_3_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_3_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_3_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x43	20	CH2_BQ4	159:128	R/W	CH2_bq_4_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_4_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_4_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_4_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_4_a2	u[31:26], a2[25:0]	32'h00000000
0x44	20	CH2_BQ5	159:128	R/W	CH2_bq_5_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_5_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_5_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_5_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_5_a2	u[31:26], a2[25:0]	32'h00000000
0x45	20	CH2_BQ6	159:128	R/W	CH2_bq_6_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_6_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_6_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_6_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_6_a2	u[31:26], a2[25:0]	32'h00000000
0x46	20	CH2_BQ7	159:128	R/W	CH2_bq_7_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_7_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_7_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_7_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_7_a2	u[31:26], a2[25:0]	32'h00000000
0x47	20	CH2_BQ8	159:128	R/W	CH2_bq_8_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_8_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_8_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_8_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_8_a2	u[31:26], a2[25:0]	32'h00000000
0x48	20	CH2_BQ9	159:128	R/W	CH2_bq_9_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_9_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_9_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_9_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_9_a2	u[31:26], a2[25:0]	32'h00000000
0x49	20	CH2_BQ10	159:128	R/W	CH2_bq_10_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_10_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_10_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_10_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_10_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x4A	20	CH2_BQ11	159:128	R/W	CH2_bq_11_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_11_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_11_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_11_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_11_a2	u[31:26], a2[25:0]	32'h00000000
0x4B	20	CH2_BQ12	159:128	R/W	CH2_bq_12_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_bq_12_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_bq_12_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_bq_12_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_bq_12_a2	u[31:26], a2[25:0]	32'h00000000
0x4C	20	CH2_SBQ13	159:128	R/W	CH2_sbq_13_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_13_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_13_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_13_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_13_a2	u[31:26], a2[25:0]	32'h00000000
0x4D	20	CH2_SBQ14	159:128	R/W	CH2_sbq_14_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_14_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_14_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_14_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_14_a2	u[31:26], a2[25:0]	32'h00000000
0x4E	20	CH2_SBQ15	159:128	R/W	CH2_sbq_15_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_15_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_15_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_15_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_15_a2	u[31:26], a2[25:0]	32'h00000000
0x4F	20	CH2_SBQ16	159:128	R/W	CH2_sbq_16_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_16_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_16_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_16_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_16_a2	u[31:26], a2[25:0]	32'h00000000
0x50	20	CH2_SBQ17	159:128	R/W	CH2_sbq_17_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_17_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_17_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_17_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_17_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x51	20	CH2_SBQ18	159:128	R/W	CH2_sbq_18_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_18_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_18_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_18_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_18_a2	u[31:26], a2[25:0]	32'h00000000
0x52	20	CH2_SBQ_BK1	159:128	R/W	CH2_sbq_bk1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_bk1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_bk1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_bk1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_bk1_a2	u[31:26], a2[25:0]	32'h00000000
0x53	20	CH2_SBQ_BK2	159:128	R/W	CH2_sbq_bk2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	CH2_sbq_bk2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	CH2_sbq_bk2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	CH2_sbq_bk2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	CH2_sbq_bk2_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x60	1	DRC_CTRL1	7	R/W	DRC4_PEAK	0 : RMS mode 1 : Peak mod (default)	1
			6	R/W	DRC3_PEAK	0 : RMS mode 1 : Peak mode (default)	1
			5	R/W	DRC2_PEAK	0 : RMS mode 1 : Peak mode (default)	1
			4	R/W	DRC1_PEAK	0 : RMS mode 1 : Peak mode (default)	1
			3	R/W	DRC4_ON	DRC4 Enable (Final DRC) 0 : Disable (default) 1 : Enable ->When disable, input signal is the same as output signal. -> Final Stage DRC enable (DRC4)	0
			2	R/W	DRC3_ON	DRC3 Enable (H band) 0 : Disable (default) 1 : Enable ->When disable, input signal is the same as output signal. ->Final Stage DRC enable (DRC3)	0
			1	R/W	DRC2_ON	DRC2 Enable (M band) 0 : Disable (default) 1 : Enable ->When disable, input signal is the same as output signal. ->Final Stage DRC enable (DRC2)	0
			0	R/W	DRC1_ON	DRC1 Enable (L_band) 0 : Disable (default) 1 : Enable ->When disable, input signal is the same as output signal. ->Final Stage DRC enable (DRC1)	0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x61	1	DRC_CTRL2	7	R/W	DRC4_N_EN	0 : DRC4 noise gate disable (default) 1 : DRC4 noise gate enable	0
			6	R/W	DRC3_N_EN	0 : DRC3 noise gate disable (default) 1 : DRC3 noise gate enable	0
			5	R/W	DRC2_N_EN	0 : DRC2 noise gate disable (default) 1 : DRC2 noise gate enable	0
			4	R/W	DRC1_N_EN	0 : DRC1 noise gate disable (default) 1 : DRC1 noise gate enable	0
			3	R/W	MB_BYPASS	0 : Normal mode (default) 1 : ByPass	0
			2	R/W	LB_BYPASS	0 : Normal mode (default) 1 : ByPass	0
			1	R/W	HB_BYPASS	0 : Normal mode (default) 1 : ByPass	0
			0	R/W	FREQ_DRC_MODE	0 : Normal mode (default) 1 : Frequency DRC mode	0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x62	1	SKIP_MBDRC_BQ1	7	R/W	SKIP_BQ1_L_MBAND	(register 0x74) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0
			6	R/W	SKIP_BQ2_L_MBAND	(register 0x75) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0
			5	R/W	SKIP_BQ1_R_MBAND	(register 0x76) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0
			4	R/W	SKIP_BQ2_R_MBAND	(register 0x77) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0
			3	R/W	SKIP_BQ1_L_HBAND	(register 0x78) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0
			2	R/W	SKIP_BQ1_R_HBAND	(register 0x79) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0
			1	R/W	SKIP_BQ1_L_LBAND	(register 0x70) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0
			0	R/W	SKIP_BQ1_R_LBAND	(register 0x72) 0 : Coefficients applied to 2 identical BQ stages (default) 1 : Coefficients applied to 1 stage only, 1 is skipped	0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x63	1	SKIP_MBDRC_BQ2	7:5	R	Reserved	Reserved	3'b000
			4	R/W	SKIP_DRC_L_HPF	L_HPF for MB and HB DRC 0 : Normal mode (default) 1 : SKIP	0
			3	R/W	SKIP_DRC_H_LPF	H_LPF for MB DRC 0 : Normal mode (default) 1 : SKIP	0
			2	R/W	SKIP_DRC_H_HPF	H_HPF for HB DRC 0 : Normal mode (default) 1 : SKIP	0
			1	R/W	SKIP_DRC_L_LPF	L_LPF for LB DRC 0 : Normal mode (default) 1 : SKIP	0
			0	R/W	SKIP_DRC_APB	APB for LB DRC 0: Normal mode(default) 1 : SKIP	0
0x70	20	LB_CH1_BQ1	159:128	R/W	LB_CH1_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	LB_CH1_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	LB_CH1_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	LB_CH1_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	LB_CH1_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x71	20	LB_CH1_BQ2	159:128	R/W	LB_CH1_bq_2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	LB_CH1_bq_2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	LB_CH1_bq_2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	LB_CH1_bq_2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	LB_CH1_bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0x72	20	LB_CH2_BQ1	159:128	R/W	LB_CH2_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	LB_CH2_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	LB_CH2_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	LB_CH2_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	LB_CH2_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x73	20	LB_CH2_BQ2	159:128	R/W	LB_CH2_bq_2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	LB_CH2_bq_2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	LB_CH2_bq_2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	LB_CH2_bq_2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	LB_CH2_bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0x74	20	MB_CH1_BQ1	159:128	R/W	MB_CH1_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	MB_CH1_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	MB_CH1_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	MB_CH1_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	MB_CH1_bq_1_a2	u[31:26], a2[25:0]	32'h00000000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x75	20	MB_CH1_BQ2	159:128	R/W	MB_CH1_bq_2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	MB_CH1_bq_2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	MB_CH1_bq_2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	MB_CH1_bq_2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	MB_CH1_bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0x76	20	MB_CH2_BQ1	159:128	R/W	MB_CH2_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	MB_CH2_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	MB_CH2_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	MB_CH2_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	MB_CH2_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x77	20	MB_CH2_BQ2	159:128	R/W	MB_CH2_bq_2_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	MB_CH2_bq_2_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	MB_CH2_bq_2_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	MB_CH2_bq_2_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	MB_CH2_bq_2_a2	u[31:26], a2[25:0]	32'h00000000
0x78	20	HB_CH1_BQ1	159:128	R/W	HB_CH1_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	HB_CH1_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	HB_CH1_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	HB_CH1_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	HB_CH1_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x79	20	HB_CH2_BQ1	159:128	R/W	HB_CH2_bq_1_b0	u[31:26], b0[25:0]	32'h00800000
			127:96	R/W	HB_CH2_bq_1_b1	u[31:26], b1[25:0]	32'h00000000
			95:64	R/W	HB_CH2_bq_1_b2	u[31:26], b2[25:0]	32'h00000000
			63:32	R/W	HB_CH2_bq_1_a1	u[31:26], a1[25:0]	32'h00000000
			31:0	R/W	HB_CH2_bq_1_a2	u[31:26], a2[25:0]	32'h00000000
0x80	1	SW_RESET	7	W	SF_RESET	0 : No action 1 : Write 1 to trigger Software reset. Need to wait 10ms for reset completion.	0
			6:0	R	Reserved	Reserved	7'b0000000
0x90	8	DRC1_RMS_AE	63:32	R/W	DRC1 RMS AE	u[31:26], ae[25:0]	32'h00800000
			31:0	R/W	DRC1 RMS 1-AE	u[31:26], (1-ae)[25:0]	32'h00000000
0x91	8	DRC1_GAIN_AA	63:32	R/W	DRC1 GAIN AA	u[31:26], aa[25:0]	32'h00800000
			31:0	R/W	DRC1 GAIN 1-AA	u[31:26], (1-aa)[25:0]	32'h00000000
0x92	8	DRC1_GAIN_AD	63:32	R/W	DRC1 GAIN AD	u[31:26], ad[25:0]	32'h00800000
			31:0	R/W	DRC1 GAIN 1-AD	u[31:26], (1-ad)[25:0]	32'h00000000
0x93	4	DRC1_TH	31:0	R/W	DRC1_T[31:0]	T1[31:0]	32'hFDA21490
0x94	4	DRC1_RATIO	31:0	R/W	DRC1_K[31:0]	u[31:26], K1[25:0]	32'h03842109

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x95	4	DRC1_OFFSET	31:0	R/W	DRC1_O[31:0]	u[31:26], O1[25:0]	32'h00084210
0x96	8	DRC2_RMS_AE	63:32	R/W	DRC2 RMS AE	u[31:26], ae[25:0]	32'h00800000
			31:0	R/W	DRC2 RMS 1-AE	u[31:26], (1-ae)[25:0]	32'h00000000
0x97	8	DRC2_GAIN_AA	63:32	R/W	DRC2 GAIN AA	u[31:26], aa[25:0]	32'h00800000
			31:0	R/W	DRC2 GAIN 1-AA	u[31:26], (1-aa)[25:0]	32'h00000000
0x98	8	DRC2_GAIN_AD	63:32	R/W	DRC2 GAIN AD	u[31:26], ad[25:0]	32'h00800000
			31:0	R/W	DRC2 GAIN 1-AD	u[31:26], (1-ad)[25:0]	32'h00000000
0x99	4	DRC2_TH	31:0	R/W	DRC2_T[31:0]	T2[31:0]	32'hFDA21490
0x9A	4	DRC2_RATIO	31:0	R/W	DRC2_K[31:0]	u[31:26], K2[25:0]	32'h03842109
0x9B	4	DRC2_OFFSET	31:0	R/W	DRC2_O[31:0]	u[31:26], O2[25:0]	32'h00084210
0x9C	8	DRC3_RMS_AE	63:32	R/W	DRC3 RMS AE	u[31:26], ae[25:0]	32'h00800000
			31:0	R/W	DRC3 RMS 1-AE	u[31:26], (1-ae)[25:0]	32'h00000000
0x9D	8	DRC3_GAIN_AA	63:32	R/W	DRC3 GAIN AA	u[31:26], aa[25:0]	32'h00800000
			31:0	R/W	DRC3 GAIN 1-AA	u[31:26], (1-aa)[25:0]	32'h00000000
0x9E	8	DRC3_GAIN_AD	63:32	R/W	DRC3 GAIN AD	u[31:26], ad[25:0]	32'h00800000
			31:0	R/W	DRC3 GAIN 1-AD	u[31:26], (1-ad)[25:0]	32'h00000000
0x9F	4	DRC3_TH	31:0	R/W	DRC3-T	T3[31:0]	32'hFDA21490
0xA0	4	DRC3_RATIO	31:0	R/W	DRC3-K	u[31:26], K3[25:0]	32'h03842109
0xA1	4	DRC3_OFFSET	31:0	R/W	DRC3-O	u[31:26], O3[25:0]	32'h00084210
0xA2	12	CH1_MBDRC_MIX	95:64	R/W	CH1_OUT_MIX_L	u[31:26], mix_2[25:0]	0x00800000
			63:32	R/W	CH1_OUT_MIX_M	u[31:26], mix_1[25:0]	0x00800000
			31:0	R/W	CH1_OUT_MIX_H	u[31:26], mix_0[25:0]	0x00800000
0xA3	12	CH2_MBDRC_MIX	95:64	R/W	CH2_OUT_MIX_L	u[31:26], mix_2[25:0]	0x00800000
			63:32	R/W	CH2_OUT_MIX_M	u[31:26], mix_1[25:0]	0x00800000
			31:0	R/W	CH2_OUT_MIX_H	u[31:26], mix_0[25:0]	0x00800000
0xA4	8	CH1_OUT_MIX	63:32	R/W	CH1_OUT_MIX_1	u[31:26], mix_1[25:0]	0x00800000
			31:0	R/W	CH1_OUT_MIX_0	u[31:26], mix_0[25:0]	0x00000000
0xA5	8	CH2_OUT_MIX	63:32	R/W	CH2_OUT_MIX_1	u[31:26], mix_1[25:0]	0x00000000
			31:0	R/W	CH2_OUT_MIX_0	u[31:26], mix_0[25:0]	0x00800000
0xA6	4	PRE_SCALE	31:0	R/W	PRE_SCALE	u[31:26], pre[25:0], 9.17 format	0x00020000
0xA7	4	POST_SCALE	31:0	R/W	POST_SCALE	u[31:26], post[25:0]	0x00800000
0xA8	1	DRC4_DELAY	7:0	R/W	DRC4_DELAY[7:0]	1/fs*DRC4_DELAY	8'hFF
0xA9	4	DRC_NG_TH	31:0	R/W	DRC_N_T[31:0]	N_T[31:0]	32'hF5B3B7C6
0xAA	4	DRC4_TH	31:0	R/W	DRC4_T[31:0]	T[31:0]	32'hFDA21490
0xAB	4	DRC4_RATIO	31:0	R/W	DRC4_K[25:0]	u[31:26], K4[25:0]	32'h03842109
0xAC	4	DRC4_OFFSET	31:0	R/W	DRC4_O[25:0]	u[31:26], O4[25:0]	32'h00081385

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0xAD	8	DRC4_AE	63:32	R/W	DRC4 AE[25:0]	u[31:26], ae[25:0]	32'h00800000
			31:0	R/W	DRC4 1-AE[25:0]	u[31:26], (1-ae)[25:0]	32'h00000000
0xAE	8	DRC4_AA	63: 32	R/W	DRC4 AA[25:0]	u[31:26], aa[25:0]	32'h00800000
			31:0	R/W	DRC4 1-AA[25:0]	u[31:26], (1-aa)[25:0]	32'h00000000
0xAF	8	DRC4_AD	63: 32	R/W	DRC4 AD[25:0]	u[31:26], ad[25:0]	32'h00800000
			31:0	R/W	DRC4 1-AD[25:0]	u[31:26], (1-ad)[25:0]	32'h00000000
0xB0	4	HARD_CLIP	31	R/W	HARD_CLIP_EN	0 : Disable hard clip (default) 1 : Enable hard clip	0
			30	R/W	DF_CLIP_EN	0 : Disable digital filter clip (default) 1 : Enable digital filter clip	0
			29:19	R	Reserved	Reserved	11'h0
			18:8	R/W	HARD_CLIP_TH[10:0]	Hard Clip Threshold when HARD_CLIP_EN = 1 11'h000 : 24dB 11'h180 : 0dB (default) 0.0625db per step	11'h180
			7:0	R/W	POST_IDF	u[31:8], POST_IDF[7:0]	8'h80
0xB1	4	COMP_FLTR1	31:16	R/W	COMP_B0[15:0]	Compensation filter B0 coefficient	16'h4000
			15:11	R	Reserved	Reserved	5'b0
			10:0	R/W	COMP_B1[10:0]	Compensation filter B1 coefficient	11'h0
0xB2	4	COMP_FLTR2	31:27	R	Reserved	Reserved	5'b00000
			26:16	R/W	COMP_B2[10:0]	Compensation filter B2 coefficient	11'h0
			15:9	R	Reserved	Reserved	7'b0000000
			8:0	R/W	COMP_B3[8:0]	Compensation filter B3 coefficient	9'h0
0xB8	8	OUT_LEVEL_A	63:32	R/W	PWM_LEVEL RMS Alpha[25:0]	u[31:26], rms[25:0]	32'h00800000
			31:0	R/W	PWM_LEVEL RMS 1-Alpha[25:0]	u[31:26], (1-rms)[25:0]	32'h00000000
0xB9	4	CH1_RMS_RPT	31:0	R	CH1_RMS[31:0]	Channel 1 Final RMS output	0
0xBA	4	CH2_RMS_RPT	31:0	R	CH2_RMS[31:0]	Channel 2 Final RMS output	0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0xBB	1	GAIN_OPT	7:5	R	Reserved	Reserved	3'b000
			4	R/W	Final_Gain	Final gain after Hard clip 0 : 0dB (default) 1 : 6dB	0
			3:0	R/W	GAIN_PAIR_CTRL	Input decrease and output increase gain control, for increase DSP dynamic range 0000: 0dB/0dB (default) 0001 : –6dB/6dB 0010 : –12dB/12dB 0011 : –18dB/18dB 0100 : –24dB/24dB 1100 : +24dB/–24dB 1101 : +18dB/–18dB 1110 : +12dB/–12dB 1111 : +6dB/–6dB Others : 0db/0db	4'b0000
0xC0	1	PLL_CONFIG1	7:4	R/W	N/A	Prohibited	4'b1010
			3	R/W	N/A	Prohibited	0
			2	R/W	N/A	Prohibited	1
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0
0xC1	1	PLL_CONFIG2	7:3	R/W	N/A	Prohibited	5'b00000
			2:0	R/W	N/A	Prohibited	3'b000
0xC2	1	PLL_CONFIG3	7:4	R/W	N/A	Prohibited	4'b0000
			3:2	R/W	N/A	Prohibited	2'b00
			1:0	R/W	N/A	Prohibited	2'b00
0xC3	1	PLL_CONFIG4	7:6	R	N/A	Prohibited	2'b00
			5:4	R/W	N/A	Prohibited	2'b01
			3	R/W	N/A	Prohibited	1
			2	R/W	N/A	Prohibited	1
			1:0	R/W	N/A	Prohibited	2'b00
0xC4	4	PLL_CONFIG5	31	R	N/A	Prohibited	0
			30:28	R	Lock_DET[2:0]	Prohibited	3'b000
			27	R	PLL_RDY	Prohibited	0
			26:23	R	N/A	Prohibited	4'b0000
			22:16	R/W	PLL_N_I	Prohibited	7'h02
			15:0	R/W	PLL_N_F	Prohibited	16'h0000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0xCA	1	BLK_EN	7:4	R	N/A	Prohibited	4'b0000
			3	R/W	N/A	Prohibited	0
			2	R/W	N/A	Prohibited	0
			1	R/W	N/A	Prohibited	1
			0	R/W	N/A	Prohibited	1
0xCB	1	ANA_BIAS1	7:6	R/W	N/A	Prohibited	2'b10
			5:4	R/W	N/A	Prohibited	2'b10
			3:2	R/W	N/A	Prohibited	2'b10
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0
0xCC	1	DAC_OPT	7	R/W	N/A	Prohibited	1
			6	R/W	N/A	Prohibited	0
			5:4	R/W	N/A	Prohibited	2'b10
			3:2	R/W	N/A	Prohibited	2'b10
			1:0	R/W	N/A	Prohibited	2'b11
0xCD	1	ANA_MODULTR1	7	R	N/A	Prohibited	0
			6	R/W	N/A	Prohibited	0
			5	R/W	N/A	Prohibited	1
			4	R/W	N/A	Prohibited	1
			3:2	R/W	N/A	Prohibited	2'b11
			1:0	R/W	N/A	Prohibited	2'b10
0xCE	1	ANA_MODULTR2	7:4	R	N/A	Prohibited	4'b0000
			3:2	R/W	D_SPK_VCM_SEL[1:0]	VCM voltage selection 00 : 2.2V 01 : 2.3V (default) 10 : 2.4V 11 : 2.5V	2'b01
			1:0	R/W	N/A	Prohibited	2'b00
0xCF	1	ANA_PWR1	7:6	R/W	D_PWM_DT_SEL[1:0]	Prohibited	2'b01
			5:4	R/W	D_PWM_SR_SEL[1:0]	Prohibited	2'b00
			3:2	R/W	D_BST_LOW_SEL[1:0]	BSTLOW threshold selection 00 : 3.93V 01 : 3.58V 10 : 3.29V (default) 11 : 3.03V	2'b10
			1	R	Reserved	Reserved	0
			0	R/W	N/A	Prohibited	1

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0xD0	1	ANA_PWR2	7:3	R	N/A	Prohibited	5'b00000
			2	R/W	N/A	Prohibited	0
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0
0xD1	1	OC_LEVEL_CTRL	7:6	R/W	N/A	Prohibited	2'b01
			5:4	R/W	N/A	Prohibited	2'b11
			3:2	R/W	N/A	Prohibited	2'b01
			1:0	R/W	N/A	Prohibited	2'b11
0xD2	1	TRI_GEN	7	R/W	N/A	Prohibited	0
			6:4	R/W	N/A	Prohibited	3'b010
			3:2	R/W	D_VTH_LOOP_SEL	Select TRI_GEN loop level 00 : No limit 01 : 90.1% 10 : 95.1% 11 : 100% (default)	2'b11
			1:0	R/W	N/A	Prohibited	2'b00
0xD3	1	ERR_RPT1	7	R	N/A	Prohibited	0
			6	R	N/A	Prohibited	0
			5	R	N/A	Prohibited	0
			4	R	N/A	Prohibited	0
			3:2	R	N/A	Prohibited	2'b00
			1	R	N/A	Prohibited	0
			0	R	N/A	Prohibited	0
0xD4	1	ERR_RPT2	7:4	R	N/A	Prohibited	4'b0000
			3:0	R	N/A	Prohibited	4'b0000
0xD5	1	PWR_SEL	7:6	R/W	N/A	Prohibited	2'b00
			0	R/W	D_AVDD_SEL	AVDD LDO output voltage 0 : 5V (default) 1 : 5.7V Noted : Output Voltage will x1.14, When the AVDD(0xD5) adjust to 5.7V	0
0xD6	1	ANA_TEST	7	R	N/A	Prohibited	0
			6	R/W	N/A	Prohibited	0
			5	R/W	N/A	Prohibited	0
			4	R/W	N/A	Prohibited	0
			3	R/W	N/A	Prohibited	0
			2	R/W	N/A	Prohibited	0
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0xD7	1	OCP_OPT	7	R/W	N/A	Prohibited	0
			6	R/W	N/A	Prohibited	0
			5	RW	N/A	Prohibited	0
			4	R/W	N/A	Prohibited	0
			3	R	N/A	Prohibited	0
			2	RW	N/A	Prohibited	0
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0
0xD8	1	DEPOP_DEGLITCH	7:4	R	N/A	Prohibited	4'b0000
			3	RW	D_DEPOP_EN	De-pop noise 0 : Disable de-pop noise circuit 1 : Enable de-pop noise circuit (default)	1
			2	RW	N/A	Prohibited	0
			1:0	RW	N/A	Prohibited	2'b01
0xD9	1	UVP_OPT	7	R/W	D_UV_RAMP_DOWN	SPK UV protection behavior 0 : HZ_PROT directly (default) 1 : Power off sequence	0
			6:4	RW	D_UVP_PVDD_SEL[2:0]	Select UVP level for PVDD power domain 000 to 010 : Reserved 011 : 9.5V (default) 100 : 10.9V 101 : 12.7V 110 : 15.4V 111 : 19.8V	3'b011
			3	RW	UV_RAMP_DOWN_SEL	0 : Ramp down time related with sampling rate and master volume. 2sample with 9 volume step. (1 sample with 4 step and 1 sample with 5 steps. From 0x180 to mute (0x7FF) with 48K sampling rate is ((0x7FF - 0x180)/9)*(2/48k) = 7.7ms 1 : Ramp down time related with POST_IDF only. Ramp down 1 POST_IDF step every 10.4μs. From 0x80 to mute (0x00) is (0x80 - 0x00)*10.4μs = 1.33ms. Recommend use UV_RAMP_DOWN_SEL = 1 to provide faster ramp down time to reduce pop sound when PVDD drop too fast.	0
			2	R	Reserved	Reserved	0
			1:0	R/W	N/A	Prohibited	2'b00

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0xDA	1	I2C_TO	7:4	R	Reserved	Reserved	3'b000
			3	R/W	N/A	Prohibited	0
			2	R/W	N/A	Prohibited	0
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0
0xDB	1	DF_OPT	7:6	R	Reserved	Reserved	2'b00
			5	R/W	N/A	Prohibited	0
			4	R/W	N/A	Prohibited	1
			3:2	R/W	N/A	Prohibited	2'b10
			1:0	R/W	N/A	Prohibited	2'b01
0xE0	1	SERVO_TIME_OPT	7:6	R/W	N/A	Prohibited	2'b00
			5:4	R/W	D_SPK_SST[1:0]	SPK start-up time 00 : 5ms 01 : 10ms (default) 10 : 20ms 11 : 40ms Noted : SST Time should larger than RC constant (3000 * BST Capacitor, for the worst case, which is 3600 * BST Capacitor)	2'b01
			3:1	R	Reserved	Reserved	3'b000
			0	R/W	PVDD_SET_TIME	0 : 2ms 1: 16ms (default)	1
0xE1	1	SERVO_CTRL_OPT	7	R/W	N/A	Prohibited	0
			6	R/W	N/A	Prohibited	0
			5	R/W	N/A	Prohibited	0
			4	R/W	N/A	Prohibited	0
			3	R/W	N/A	Prohibited	0
			2	R/W	N/A	Prohibited	1
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0
0xE2	1	OFFSET_CAL1_L	7:0	R/W	N/A	Prohibited	8'h40
0xE3	1	OFFSET_CAL1_R	7:0	R/W	N/A	Prohibited	8'h40
0xE4	1	OFFSET_RPT1_L	7:0	R	N/A	Prohibited	8'h40
0xE5	1	OFFSET_RPT1_R	7:0	R	N/A	Prohibited	8'h40
0xE6	1	OFFSET_RPT2_L	7:0	R	N/A	Prohibited	8'h40
0eE7	1	OFFSET_RPT2_R	7:0	R	N/A	Prohibited	8'h40

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0xF0	1	DIG_TEST1	7:0	R/W	N/A	Prohibited	0
0xF1	1	DIG_TEST2	7:0	R	N/A	Prohibited	8'h0
0xF2	1	DIG_TEST3	7:0	R/W	N/A	Prohibited	8'h0
0xF3	1	DIG_TEST4	7	R	N/A	Prohibited	0
			6:2	R	N/A	Prohibited	5'b00000
			1	W	N/A	Prohibited	0
			0	W	N/A	Prohibited	0
0xF4	1	DIG_TEST5	7:4	R/W	N/A	Prohibited	4'b0000
			3	R/W	N/A	Prohibited	0
			2:1	R/W	N/A	Prohibited	2'b00
			0	R/W	N/A	Prohibited	0
0xF5	1	DIG_TEST6	7:5	R/W	N/A	Prohibited	3'b000
			4	RW	N/A	Prohibited	**0**
			3	R/W	N/A	Prohibited	0
			2:0	R/W	N/A	Prohibited	3'b100
0xF6	1	BIST_RPT	7:0	R	N/A	Prohibited	8'h0
0xF7	1	BIST_EN	7:6	R	N/A	Prohibited	2'b00
			5:4	R	N/A	Prohibited	2'b00
			3	R	N/A	Prohibited	0
			2	R	N/A	Prohibited	0
			1	R	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	0
0xF8	1	DIG_TEST7	7:4	R/W	N/A	Prohibited	4'b0000
			3	R/W	N/A	Prohibited	0
			2	R/W	N/A	Prohibited	0
			1	R/W	N/A	Prohibited	0
			0	R/W	N/A	Prohibited	1
0xF9	1	DIG_TEST8	7:5	R/W	N/A	Prohibited	3'b000
			4	R/W	N/A	Prohibited	1
			3	R/W	N/A	Prohibited	0
			2	R/W	N/A	Prohibited	0
			1:0	R/W	N/A	Prohibited	2'b00
0xFA	1	SCAN_MODE	7:0	R/W	N/A	Prohibited	8'b0

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x20	4	FIR_TAP1	31:0	R/W	FIR_TAP1	u[31:26], b0[25:0] u : Unused	32'h00010000
0x21	4	FIR_TAP2	31:0	R/W	FIR_TAP2	u[31:26], b0[25:0] u : Unused	32'h00010000
0x22	4	FIR_TAP3	31:0	R/W	FIR_TAP3	u[31:26], b0[25:0] u : Unused	32'h00010000
0x23	4	FIR_TAP4	31:0	R/W	FIR_TAP4	u[31:26], b0[25:0] u : Unused	32'h00010000
0x24	4	FIR_TAP5	31:0	R/W	FIR_TAP5	u[31:26], b0[25:0] u : Unused	32'h00010000
0x25	4	FIR_TAP6	31:0	R/W	FIR_TAP6	u[31:26], b0[25:0] u : Unused	32'h00010000
0x26	4	FIR_TAP7	31:0	R/W	FIR_TAP7	u[31:26], b0[25:0] u : Unused	32'h00010000
0x27	4	FIR_TAP8	31:0	R/W	FIR_TAP8	u[31:26], b0[25:0] u : Unused	32'h00010000
0x28	4	FIR_TAP9	31:0	R/W	FIR_TAP9	u[31:26], b0[25:0] u : Unused	32'h00010000
0x29	4	FIR_TAP10	31:0	R/W	FIR_TAP10	u[31:26], b0[25:0] u : Unused	32'h00010000
0x2A	4	FIR_TAP11	31:0	R/W	FIR_TAP11	u[31:26], b0[25:0] u : Unused	32'h00010000
0x2B	4	FIR_TAP12	31:0	R/W	FIR_TAP12	u[31:26], b0[25:0] u : Unused	32'h00010000
0x2C	4	FIR_TAP13	31:0	R/W	FIR_TAP13	u[31:26], b0[25:0] u : Unused	32'h00010000
0x2D	4	FIR_TAP14	31:0	R/W	FIR_TAP14	u[31:26], b0[25:0] u : Unused	32'h00010000
0x2E	4	FIR_TAP15	31:0	R/W	FIR_TAP15	u[31:26], b0[25:0] u : Unused	32'h00010000
0x2F	4	FIR_TAP16	31:0	R/W	FIR_TAP16	u[31:26], b0[25:0] u : Unused	32'h00010000
0x30	4	FIR_TAP17	31:0	R/W	FIR_TAP17	u[31:26], b0[25:0] u : Unused	32'h00010000
0x31	4	FIR_TAP18	31:0	R/W	FIR_TAP18	u[31:26], b0[25:0] u : Unused	32'h00010000
0x32	4	FIR_TAP19	31:0	R/W	FIR_TAP19	u[31:26], b0[25:0] u : Unused	32'h00010000
0x33	4	FIR_TAP20	31:0	R/W	FIR_TAP20	u[31:26], b0[25:0] u : Unused	32'h00010000
0x34	4	FIR_TAP21	31:0	R/W	FIR_TAP21	u[31:26], b0[25:0] u : Unused	32'h00010000
0x35	4	FIR_TAP22	31:0	R/W	FIR_TAP22	u[31:26], b0[25:0] u : Unused	32'h00010000
0x36	4	FIR_TAP23	31:0	R/W	FIR_TAP23	u[31:26], b0[25:0] u : Unused	32'h00010000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x37	4	FIR_TAP24	31:0	R/W	FIR_TAP24	u[31:26], b0[25:0] u : Unused	32'h00010000
0x38	4	FIR_TAP25	31:0	R/W	FIR_TAP25	u[31:26], b0[25:0] u : Unused	32'h00010000
0x39	4	FIR_TAP26	31:0	R/W	FIR_TAP26	u[31:26], b0[25:0] u : Unused	32'h00010000
0x3A	4	FIR_TAP27	31:0	R/W	FIR_TAP27	u[31:26], b0[25:0] u : Unused	32'h00010000
0x3B	4	FIR_TAP28	31:0	R/W	FIR_TAP28	u[31:26], b0[25:0] u : Unused	32'h00010000
0x3C	4	FIR_TAP29	31:0	R/W	FIR_TAP29	u[31:26], b0[25:0] u : Unused	32'h00010000
0x3D	4	FIR_TAP30	31:0	R/W	FIR_TAP30	u[31:26], b0[25:0] u : Unused	32'h00010000
0x3E	4	FIR_TAP31	31:0	R/W	FIR_TAP31	u[31:26], b0[25:0] u : Unused	32'h00010000
0x3F	4	FIR_TAP32	31:0	R/W	FIR_TAP32	u[31:26], b0[25:0] u : Unused	32'h00010000
0x40	4	FIR_TAP33	31:0	R/W	FIR_TAP33	u[31:26], b0[25:0] u : Unused	32'h00010000
0x41	4	FIR_TAP34	31:0	R/W	FIR_TAP34	u[31:26], b0[25:0] u : Unused	32'h00010000
0x42	4	FIR_TAP35	31:0	R/W	FIR_TAP35	u[31:26], b0[25:0] u : Unused	32'h00010000
0x43	4	FIR_TAP36	31:0	R/W	FIR_TAP36	u[31:26], b0[25:0] u : Unused	32'h00010000
0x44	4	FIR_TAP37	31:0	R/W	FIR_TAP37	u[31:26], b0[25:0] u : Unused	32'h00010000
0x45	4	FIR_TAP38	31:0	R/W	FIR_TAP38	u[31:26], b0[25:0] u : Unused	32'h00010000
0x46	4	FIR_TAP39	31:0	R/W	FIR_TAP39	u[31:26], b0[25:0] u : Unused	32'h00010000
0x47	4	FIR_TAP40	31:0	R/W	FIR_TAP40	u[31:26], b0[25:0] u : Unused	32'h00010000
0x48	4	FIR_TAP41	31:0	R/W	FIR_TAP41	u[31:26], b0[25:0] u : Unused	32'h00010000
0x49	4	FIR_TAP42	31:0	R/W	FIR_TAP42	u[31:26], b0[25:0] u : Unused	32'h00010000
0x4A	4	FIR_TAP43	31:0	R/W	FIR_TAP43	u[31:26], b0[25:0] u : Unused	32'h00010000
0x4B	4	FIR_TAP44	31:0	R/W	FIR_TAP44	u[31:26], b0[25:0] u : Unused	32'h00010000
0x4C	4	FIR_TAP45	31:0	R/W	FIR_TAP45	u[31:26], b0[25:0] u : Unused	32'h00010000
0x4D	4	FIR_TAP46	31:0	R/W	FIR_TAP46	u[31:26], b0[25:0] u : Unused	32'h00010000

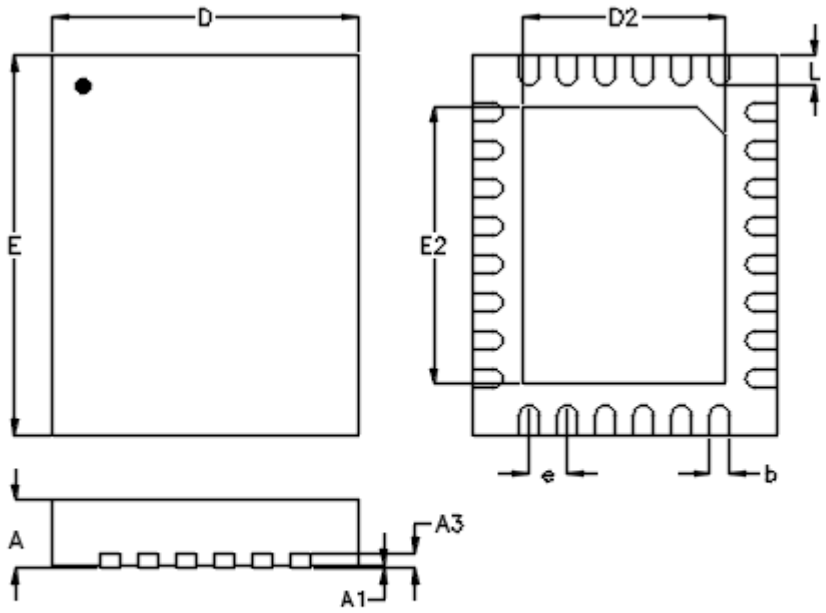
ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x4E	4	FIR_TAP47	31:0	R/W	FIR_TAP47	u[31:26], b0[25:0] u : Unused	32'h00010000
0x4F	4	FIR_TAP48	31:0	R/W	FIR_TAP48	u[31:26], b0[25:0] u : Unused	32'h00010000
0x50	4	FIR_TAP49	31:0	R/W	FIR_TAP49	u[31:26], b0[25:0] u : Unused	32'h00010000
0x51	4	FIR_TAP50	31:0	R/W	FIR_TAP50	u[31:26], b0[25:0] u : Unused	32'h00010000
0x52	4	FIR_TAP51	31:0	R/W	FIR_TAP51	u[31:26], b0[25:0] u : Unused	32'h00010000
0x53	4	FIR_TAP52	31:0	R/W	FIR_TAP52	u[31:26], b0[25:0] u : Unused	32'h00010000
0x54	4	FIR_TAP53	31:0	R/W	FIR_TAP53	u[31:26], b0[25:0] u : Unused	32'h00010000
0x55	4	FIR_TAP54	31:0	R/W	FIR_TAP54	u[31:26], b0[25:0] u : Unused	32'h00010000
0x56	4	FIR_TAP55	31:0	R/W	FIR_TAP55	u[31:26], b0[25:0] u : Unused	32'h00010000
0x57	4	FIR_TAP56	31:0	R/W	FIR_TAP56	u[31:26], b0[25:0] u : Unused	32'h00010000
0x58	4	FIR_TAP57	31:0	R/W	FIR_TAP57	u[31:26], b0[25:0] u : Unused	32'h00010000
0x59	4	FIR_TAP58	31:0	R/W	FIR_TAP58	u[31:26], b0[25:0] u : Unused	32'h00010000
0x5A	4	FIR_TAP59	31:0	R/W	FIR_TAP59	u[31:26], b0[25:0] u : Unused	32'h00010000
0x5B	4	FIR_TAP60	31:0	R/W	FIR_TAP60	u[31:26], b0[25:0] u : Unused	32'h00010000
0x5C	4	FIR_TAP61	31:0	R/W	FIR_TAP61	u[31:26], b0[25:0] u : Unused	32'h00010000
0x5D	4	FIR_TAP62	31:0	R/W	FIR_TAP62	u[31:26], b0[25:0] u : Unused	32'h00010000
0x5E	4	FIR_TAP63	31:0	R/W	FIR_TAP63	u[31:26], b0[25:0] u : Unused	32'h00010000
0x5F	4	FIR_TAP64	31:0	R/W	FIR_TAP64	u[31:26], b0[25:0] u : Unused	32'h00010000
0x60	4	FIR_TAP65	31:0	R/W	FIR_TAP65	u[31:26], b0[25:0] u : Unused	32'h00010000
0x61	4	FIR_TAP66	31:0	R/W	FIR_TAP66	u[31:26], b0[25:0] u : Unused	32'h00010000
0x62	4	FIR_TAP67	31:0	R/W	FIR_TAP67	u[31:26], b0[25:0] u : Unused	32'h00010000
0x63	4	FIR_TAP68	31:0	R/W	FIR_TAP68	u[31:26], b0[25:0] u : Unused	32'h00010000
0x64	4	FIR_TAP69	31:0	R/W	FIR_TAP69	u[31:26], b0[25:0] u : Unused	32'h00010000

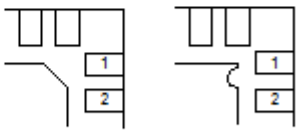
ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x65	4	FIR_TAP70	31:0	R/W	FIR_TAP70	u[31:26], b0[25:0] u : Unused	32'h00010000
0x66	4	FIR_TAP71	31:0	R/W	FIR_TAP71	u[31:26], b0[25:0] u : Unused	32'h00010000
0x67	4	FIR_TAP72	31:0	R/W	FIR_TAP72	u[31:26], b0[25:0] u : Unused	32'h00010000
0x68	4	FIR_TAP73	31:0	R/W	FIR_TAP73	u[31:26], b0[25:0] u : Unused	32'h00010000
0x69	4	FIR_TAP74	31:0	R/W	FIR_TAP74	u[31:26], b0[25:0] u : Unused	32'h00010000
0x6A	4	FIR_TAP75	31:0	R/W	FIR_TAP75	u[31:26], b0[25:0] u : Unused	32'h00010000
0x6B	4	FIR_TAP76	31:0	R/W	FIR_TAP76	u[31:26], b0[25:0] u : Unused	32'h00010000
0x6C	4	FIR_TAP77	31:0	R/W	FIR_TAP77	u[31:26], b0[25:0] u : Unused	32'h00010000
0x6D	4	FIR_TAP78	31:0	R/W	FIR_TAP78	u[31:26], b0[25:0] u : Unused	32'h00010000
0x6E	4	FIR_TAP79	31:0	R/W	FIR_TAP79	u[31:26], b0[25:0] u : Unused	32'h00010000
0x6F	4	FIR_TAP80	31:0	R/W	FIR_TAP80	u[31:26], b0[25:0] u : Unused	32'h00010000
0x70	4	FIR_TAP81	31:0	R/W	FIR_TAP81	u[31:26], b0[25:0] u : Unused	32'h00010000
0x71	4	FIR_TAP82	31:0	R/W	FIR_TAP82	u[31:26], b0[25:0] u : Unused	32'h00010000
0x72	4	FIR_TAP83	31:0	R/W	FIR_TAP83	u[31:26], b0[25:0] u : Unused	32'h00010000
0x73	4	FIR_TAP84	31:0	R/W	FIR_TAP84	u[31:26], b0[25:0] u : Unused	32'h00010000
0x74	4	FIR_TAP85	31:0	R/W	FIR_TAP85	u[31:26], b0[25:0] u : Unused	32'h00010000
0x75	4	FIR_TAP86	31:0	R/W	FIR_TAP86	u[31:26], b0[25:0] u : Unused	32'h00010000
0x76	4	FIR_TAP87	31:0	R/W	FIR_TAP87	u[31:26], b0[25:0] u : Unused	32'h00010000
0x77	4	FIR_TAP88	31:0	R/W	FIR_TAP88	u[31:26], b0[25:0] u : Unused	32'h00010000
0x78	4	FIR_TAP89	31:0	R/W	FIR_TAP89	u[31:26], b0[25:0] u : Unused	32'h00010000
0x79	4	FIR_TAP90	31:0	R/W	FIR_TAP90	u[31:26], b0[25:0] u : Unused	32'h00010000
0x7A	4	FIR_TAP91	31:0	R/W	FIR_TAP91	u[31:26], b0[25:0] u : Unused	32'h00010000
0x7B	4	FIR_TAP92	31:0	R/W	FIR_TAP92	u[31:26], b0[25:0] u : Unused	32'h00010000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x7C	4	FIR_TAP93	31:0	R/W	FIR_TAP93	u[31:26], b0[25:0] u : Unused	32'h00010000
0x7D	4	FIR_TAP94	31:0	R/W	FIR_TAP94	u[31:26], b0[25:0] u : Unused	32'h00010000
0x7E	4	FIR_TAP95	31:0	R/W	FIR_TAP95	u[31:26], b0[25:0] u : Unused	32'h00010000
0x7F	4	FIR_TAP96	31:0	R/W	FIR_TAP96	u[31:26], b0[25:0] u : Unused	32'h00010000
0x80	4	FIR_TAP97	31:0	R/W	FIR_TAP97	u[31:26], b0[25:0] u : Unused	32'h00010000
0x81	4	FIR_TAP98	31:0	R/W	FIR_TAP98	u[31:26], b0[25:0] u : Unused	32'h00010000
0x82	4	FIR_TAP99	31:0	R/W	FIR_TAP99	u[31:26], b0[25:0] u : Unused	32'h00010000
0x83	4	FIR_TAP100	31:0	R/W	FIR_TAP100	u[31:26], b0[25:0] u : Unused	32'h00010000
0x84	4	FIR_TAP101	31:0	R/W	FIR_TAP101	u[31:26], b0[25:0] u : Unused	32'h00010000
0x85	4	FIR_TAP102	31:0	R/W	FIR_TAP102	u[31:26], b0[25:0] u : Unused	32'h00010000
0x86	4	FIR_TAP103	31:0	R/W	FIR_TAP103	u[31:26], b0[25:0] u : Unused	32'h00010000
0x87	4	FIR_TAP104	31:0	R/W	FIR_TAP104	u[31:26], b0[25:0] u : Unused	32'h00010000
0x88	4	FIR_TAP105	31:0	R/W	FIR_TAP105	u[31:26], b0[25:0] u : Unused	32'h00010000
0x89	4	FIR_TAP106	31:0	R/W	FIR_TAP106	u[31:26], b0[25:0] u : Unused	32'h00010000
0x8A	4	FIR_TAP107	31:0	R/W	FIR_TAP107	u[31:26], b0[25:0] u : Unused	32'h00010000
0x8B	4	FIR_TAP108	31:0	R/W	FIR_TAP108	u[31:26], b0[25:0] u : Unused	32'h00010000
0x8C	4	FIR_TAP109	31:0	R/W	FIR_TAP109	u[31:26], b0[25:0] u : Unused	32'h00010000
0x8D	4	FIR_TAP110	31:0	R/W	FIR_TAP110	u[31:26], b0[25:0] u : Unused	32'h00010000
0x8E	4	FIR_TAP111	31:0	R/W	FIR_TAP111	u[31:26], b0[25:0] u : Unused	32'h00010000
0x8F	4	FIR_TAP112	31:0	R/W	FIR_TAP112	u[31:26], b0[25:0] u : Unused	32'h00010000
0x90	4	FIR_TAP113	31:0	R/W	FIR_TAP113	u[31:26], b0[25:0] u : Unused	32'h00010000
0x91	4	FIR_TAP114	31:0	R/W	FIR_TAP114	u[31:26], b0[25:0] u : Unused	32'h00010000
0x92	4	FIR_TAP115	31:0	R/W	FIR_TAP115	u[31:26], b0[25:0] u : Unused	32'h00010000

ADDR	Byte Number	RegName	BITS	R/W	Name	Description	Default
0x93	4	FIR_TAP116	31:0	R/W	FIR_TAP116	u[31:26], b0[25:0] u : Unused	32'h00010000
0x94	4	FIR_TAP117	31:0	R/W	FIR_TAP117	u[31:26], b0[25:0] u : Unused	32'h00010000
0x95	4	FIR_TAP118	31:0	R/W	FIR_TAP118	u[31:26], b0[25:0] u : Unused	32'h00010000
0x96	4	FIR_TAP119	31:0	R/W	FIR_TAP119	u[31:26], b0[25:0] u : Unused	32'h00010000
0x97	4	FIR_TAP120	31:0	R/W	FIR_TAP120	u[31:26], b0[25:0] u : Unused	32'h00010000
0x98	4	FIR_TAP121	31:0	R/W	FIR_TAP121	u[31:26], b0[25:0] u : Unused	32'h00010000
0x99	4	FIR_TAP122	31:0	R/W	FIR_TAP122	u[31:26], b0[25:0] u : Unused	32'h00010000
0x9A	4	FIR_TAP123	31:0	R/W	FIR_TAP123	u[31:26], b0[25:0] u : Unused	32'h00010000
0x9B	4	FIR_TAP124	31:0	R/W	FIR_TAP124	u[31:26], b0[25:0] u : Unused	32'h00010000
0x9C	4	FIR_TAP125	31:0	R/W	FIR_TAP125	u[31:26], b0[25:0] u : Unused	32'h00010000
0x9D	4	FIR_TAP126	31:0	R/W	FIR_TAP126	u[31:26], b0[25:0] u : Unused	32'h00010000
0x9E	4	FIR_TAP127	31:0	R/W	FIR_TAP127	u[31:26], b0[25:0] u : Unused	32'h00010000
0x9F	4	FIR_TAP128	31:0	R/W	FIR_TAP128	u[31:26], b0[25:0] u : Unused	32'h00010000

Outline Dimension





DETAIL A

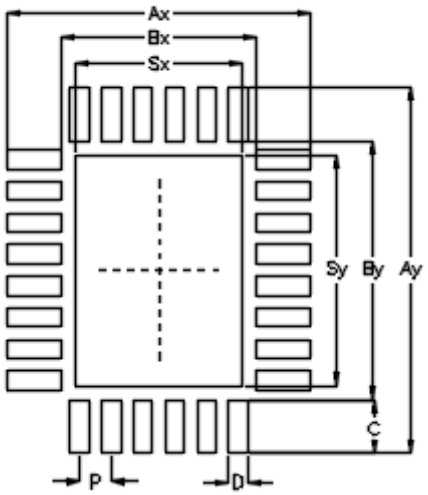
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.900	4.100	0.154	0.161
D2	2.600	2.700	0.102	0.106
E	4.900	5.100	0.193	0.201
E2	3.600	3.700	0.142	0.146
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 28L QFN 4x5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*5-28	28	0.50	4.80	5.80	3.10	4.10	0.85	0.30	2.65	3.65	±0.05

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