

SUD50P08-25L-E3-VB Datasheet

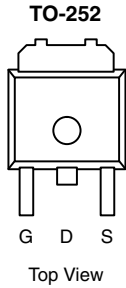
P-Channel 100-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

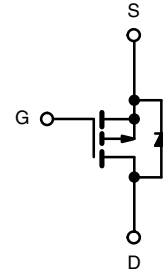
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ)
- 100	0.017 at $V_{GS} = - 10$ V	- 50	55 nC
	0.021 at $V_{GS} = - 4.5$ V	- 47	

FEATURES

- Trench Power MOSFET


RoHS
 COMPLIANT


Drain Connected to Tab



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175\text{ }^{\circ}\text{C}$)	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	- 50 ^a	A
	$T_C = 70\text{ }^{\circ}\text{C}$		- 42.5 ^a	
	$T_A = 25\text{ }^{\circ}\text{C}$		- 12.5 ^{b, c}	
	$T_A = 70\text{ }^{\circ}\text{C}$		- 10.5 ^{b, c}	
Pulsed Drain Current		I_{DM}	- 40	
Continuous Source-Drain Diode Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_S	- 50 ^a	
	$T_A = 25\text{ }^{\circ}\text{C}$		- 6.9 ^{b, c}	
Avalanche Current	L = 0.1 mH	I_{AS}	- 45	mJ
Single-Pulse Avalanche Energy		E_{AS}	101	
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	136	W
	$T_C = 70\text{ }^{\circ}\text{C}$		95	
	$T_A = 25\text{ }^{\circ}\text{C}$		8.3 ^{b, c}	
	$T_A = 70\text{ }^{\circ}\text{C}$		5.8 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 10$ sec	R_{thJA}	15	18	$^{\circ}\text{C/W}$
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.85	1.1	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 10$ sec.d. Maximum under steady state conditions is 40 $^{\circ}\text{C/W}$.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 73		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1		- 3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 100 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 100 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = - 10 V				A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = - 10 V, I _D = - 12.5 A		0.017		Ω
		V _{GS} = - 4.5 V, I _D = - 10.5 A		0.021		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 12.5 A		52		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 50 V, V _{GS} = 0 V, f = 1 MHz		4700		pF
Output Capacitance	C _{oss}			320		
Reverse Transfer Capacitance	C _{rss}			235		
Total Gate Charge	Q _g	V _{DS} = - 50 V, V _{GS} = - 10 V, I _D = - 12.5 A		105	160	nC
		V _{DS} = - 50 V, V _{GS} = - 4.5 V, I _D = - 12.5 A		55	85	
Gate-Source Charge	Q _{gs}			16		
Gate-Drain Charge	Q _{gd}			26		
Gate Resistance	R _g	f = 1 MHz		4		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 50 V, R _L = 3.8 Ω I _D ≅ - 10.5 A, V _{GEN} = - 10 V, R _g = 1 Ω		45	70	ns
Rise Time	t _r			220	330	
Turn-Off Delay Time	t _{d(off)}			95	145	
Fall Time	t _f			110	165	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 40 V, R _L = 3.8 Ω I _D ≅ - 10.5 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		15	25	ns
Rise Time	t _r			25	40	
Turn-Off Delay Time	t _{d(off)}			105	160	
Fall Time	t _f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 50	A
Pulse Diode Forward Current ^a	I _{SM}				- 40	
Body Diode Voltage	V _{SD}	I _S = - 10.5 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 10.5 A, di/dt = 100 A/μs, T _J = 25 °C		55	85	ns
Body Diode Reverse Recovery Charge	Q _{rr}			110	165	nC
Reverse Recovery Fall Time	t _a			37		ns
Reverse Recovery Rise Time	t _b			18		

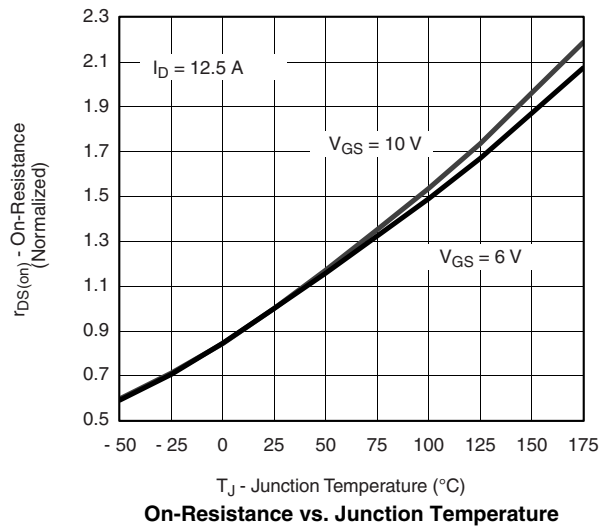
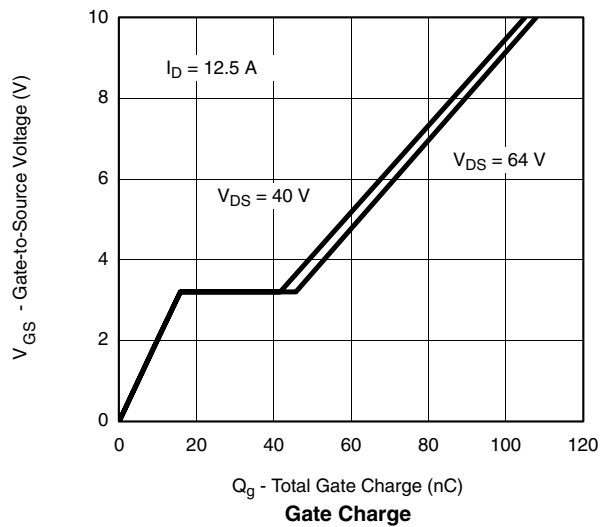
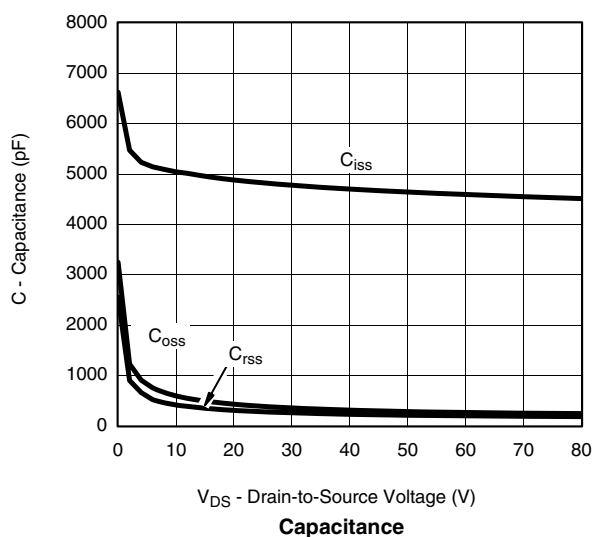
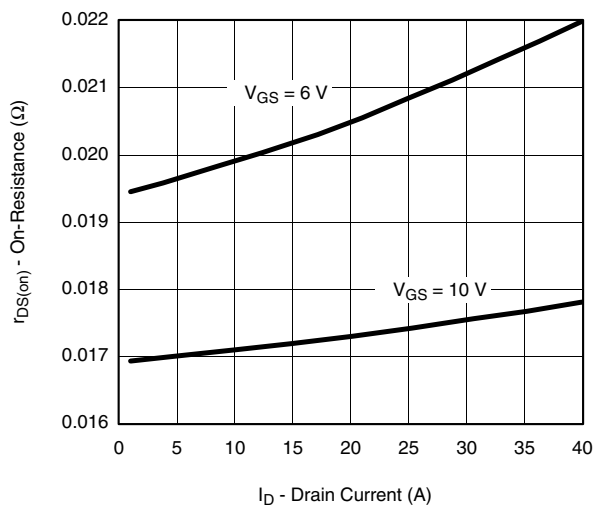
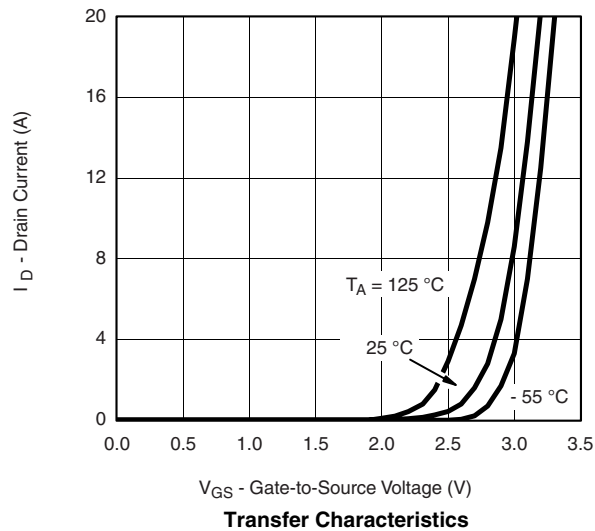
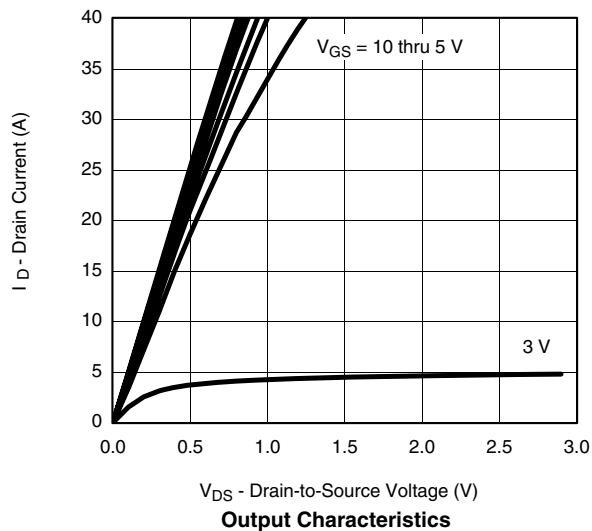
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

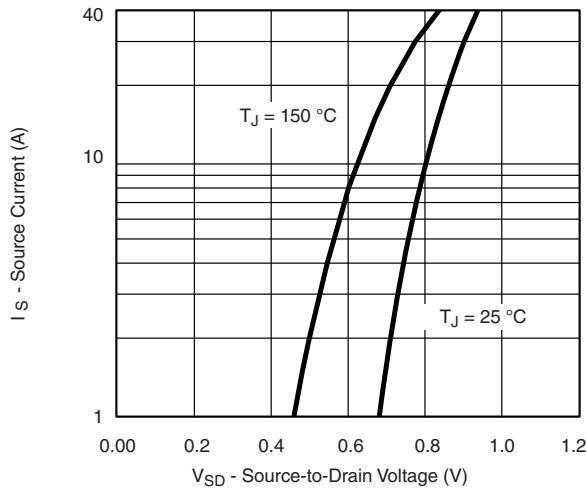
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

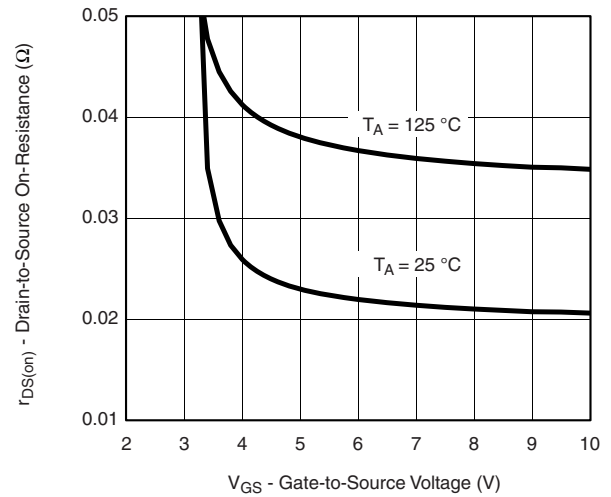
TYPICAL CHARACTERISTICS 25 °C unless noted



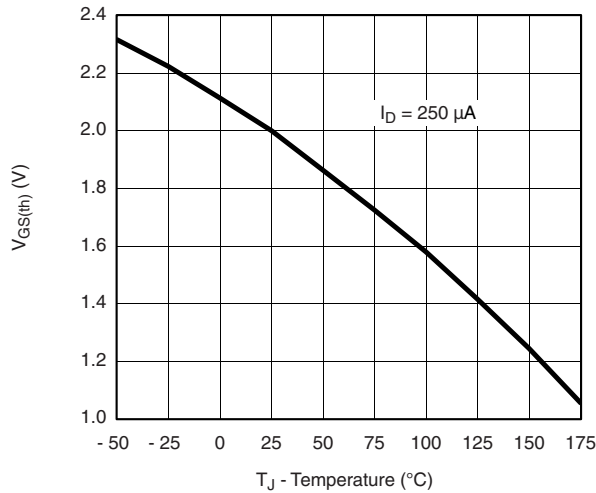
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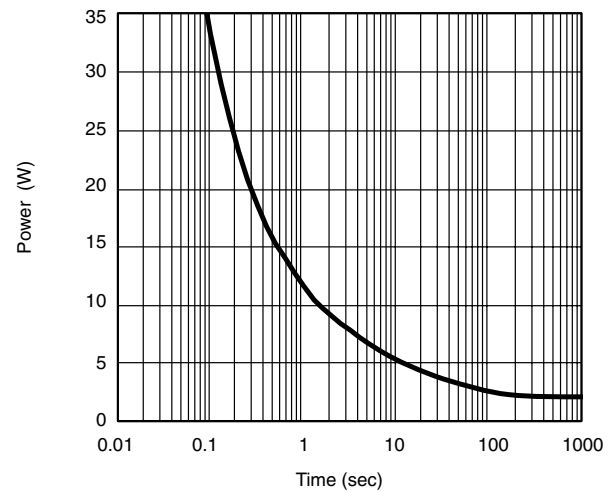
Source-Drain Diode Forward Voltage



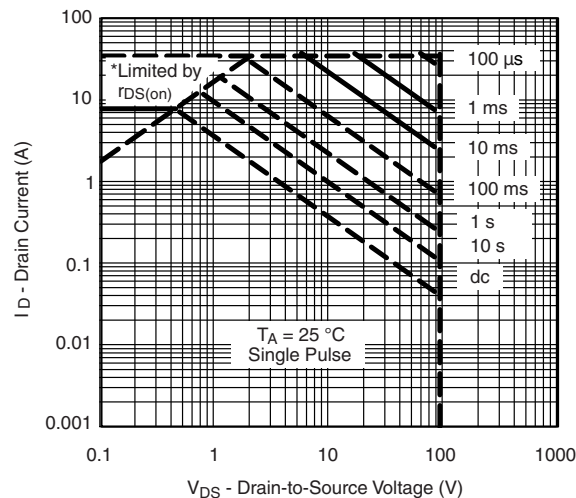
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



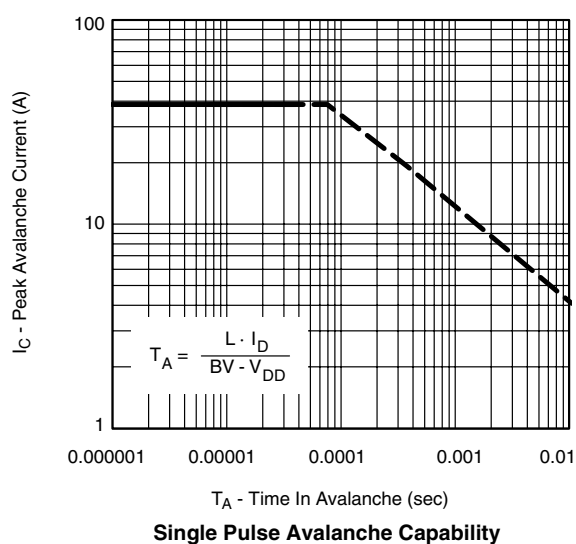
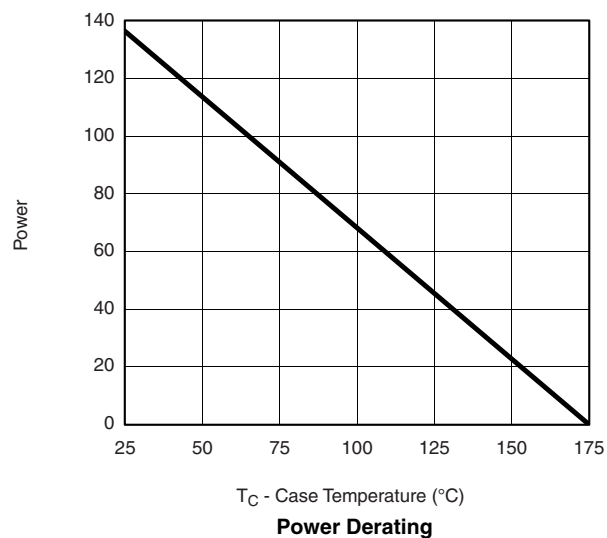
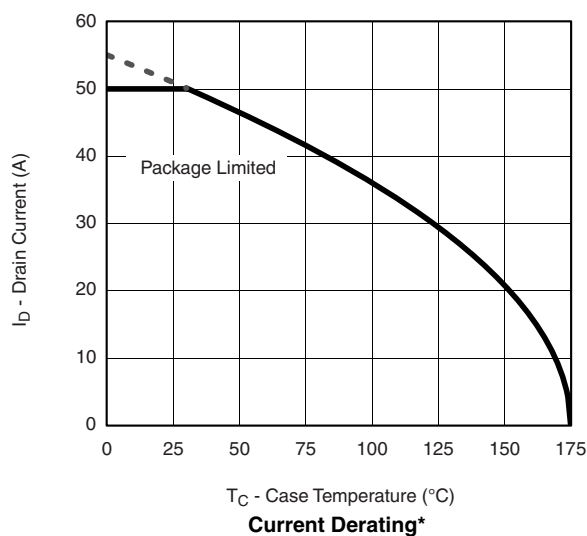
Single Pulse Power, Junction-to-Ambient



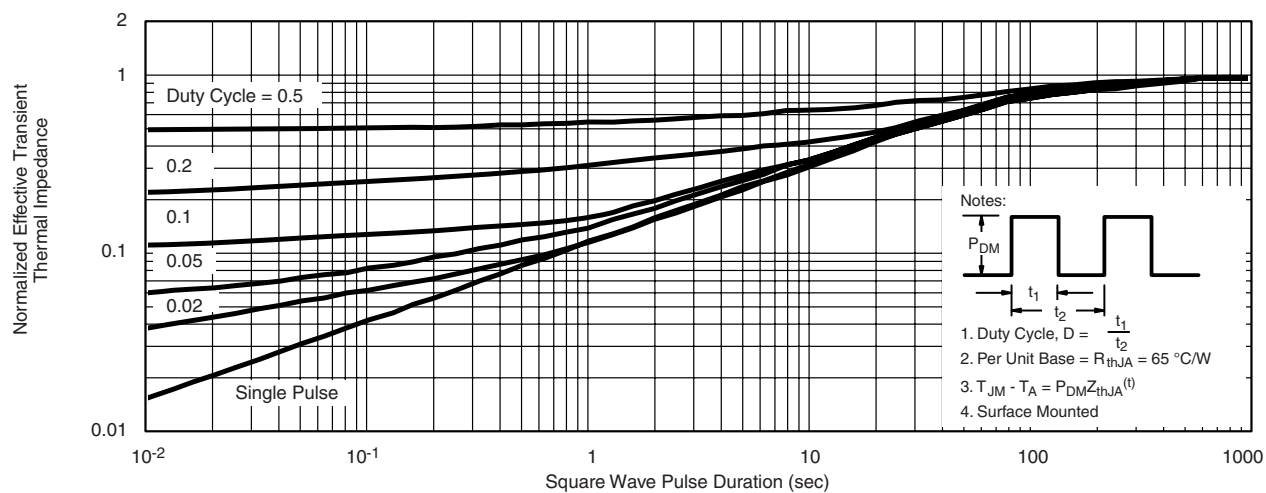
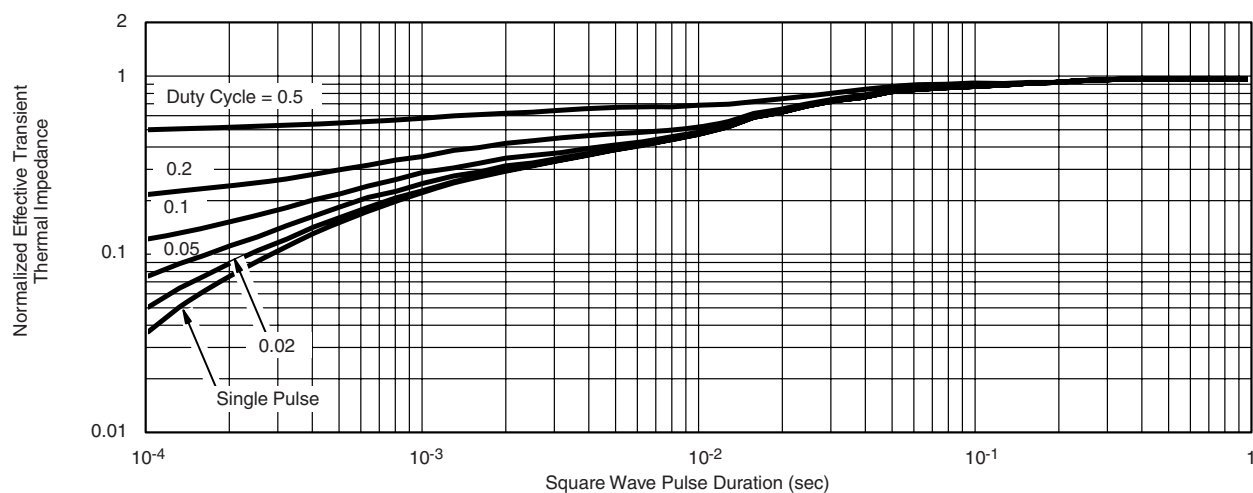
* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C unless noted



*The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C unless noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

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