

# MOSFET – N-Channel, POWERTRENCH®

**30 V, 20 A, 2.2 mΩ**

## FDMC7660

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Features

- Max  $r_{DS(on)}$  = 2.2 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 20\text{ A}$
- Max  $r_{DS(on)}$  = 3.3 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 18\text{ A}$
- High Performance Technology for Extremely Low  $r_{DS(on)}$
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- DC – DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching

### MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

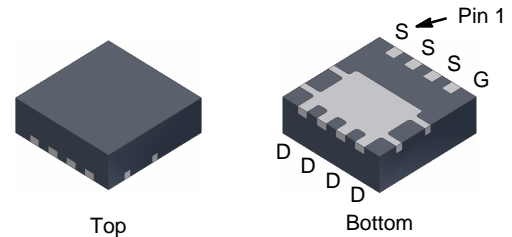
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	±20	V
$I_D$	Drain Current – Continuous (Package Limited) $T_C = 25^\circ\text{C}$ – Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$ – Continuous $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed	40 100 20 200	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	200	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	41 2.3	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

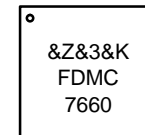
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
30 V	2.2 mΩ @ 10 V	20 A
	3.3 mΩ @ 4.5 V	



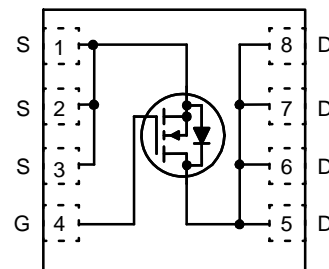
PQFN8 3.3X3.3, 0.65P  
(Power 33)  
CASE 483AK

### MARKING DIAGRAM



&Z = Assembly Plant Code  
&3 = 3-Digit Date Code  
&K = 2-Digits Lot Run Traceability Code  
FDMC7660 = Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDMC7660

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

B <sub>V</sub> DSS	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	30	–	–	V
$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	14	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	–	–	100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–6	–	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	–	1.8	2.2	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 18 A	–	2.6	3.3	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125°C	–	2.2	3.1	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 20 A	–	163	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	3630	4830	pF
C <sub>oss</sub>	Output Capacitance		–	1345	1790	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	110	165	pF
R <sub>g</sub>	Gate Resistance		–	0.9	–	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	14	25	ns
t <sub>r</sub>	Rise Time		–	6.8	14	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	36	58	ns
t <sub>f</sub>	Fall Time		–	5.7	11	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 20 A	–	54	86	nC
		V <sub>GS</sub> = 0 V to 4.5 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 20 A	–	24	38	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 20 A	–	11	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	5.6	–	nC

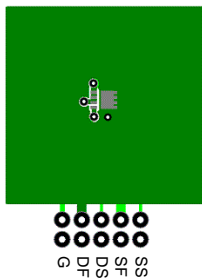
### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source-Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A (Note 2)	–	0.8	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.9 A (Note 2)	–	0.7	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 20 A, di/dt = 100 A/μs	–	45	63	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	25	35	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- Starting T<sub>J</sub> = 25°C, L = 1 mH, I<sub>AS</sub> = 20 A, V<sub>DD</sub> = 27 V, V<sub>GS</sub> = 10 V.
- As an N-channel device, the negative V<sub>gs</sub> rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

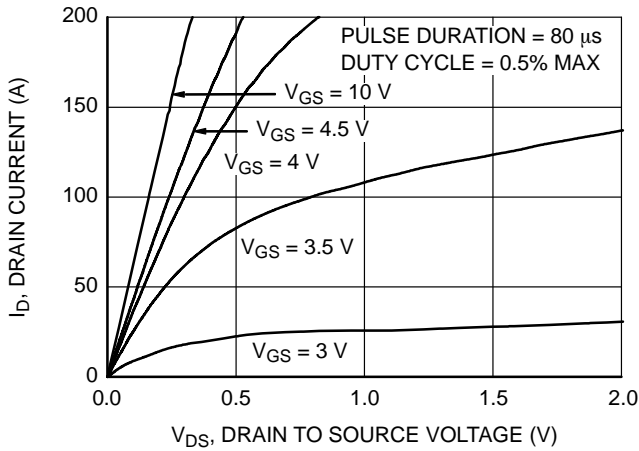


Figure 1. On Region Characteristics

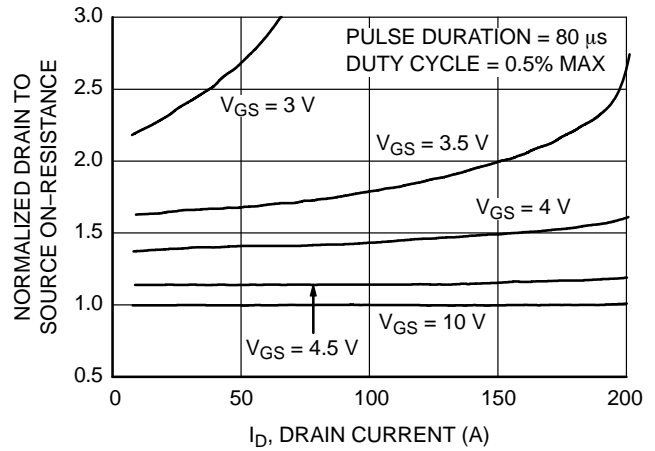


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

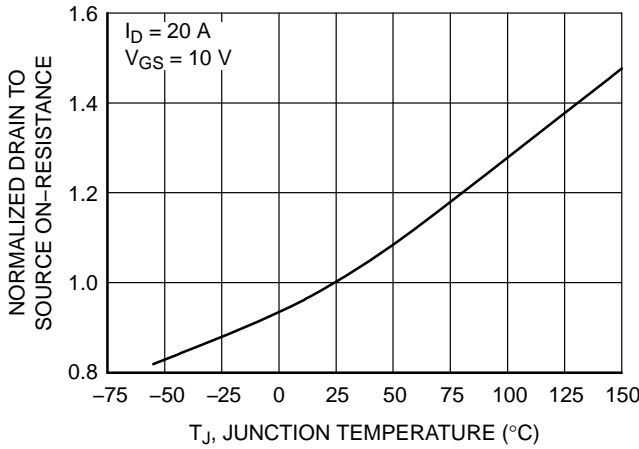


Figure 3. Normalized On Resistance vs. Junction Temperature

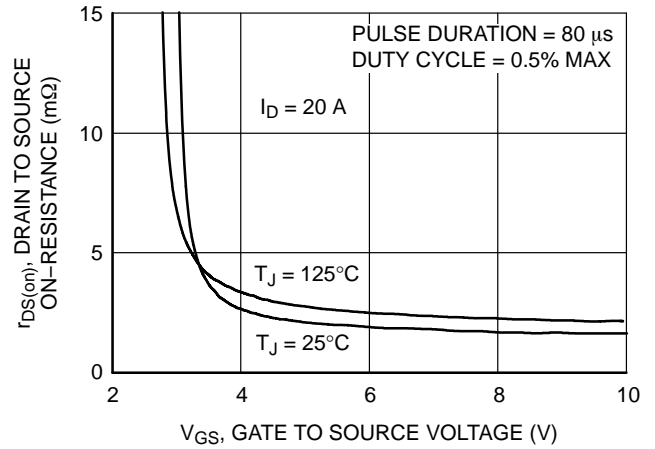


Figure 4. On-Resistance vs. Gate to Source Voltage

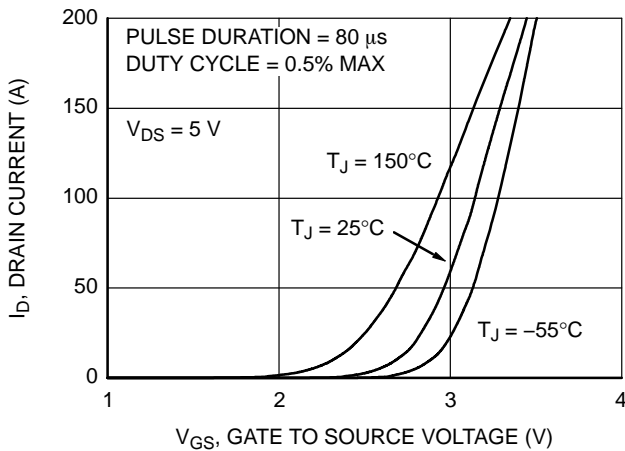


Figure 5. Transfer Characteristics

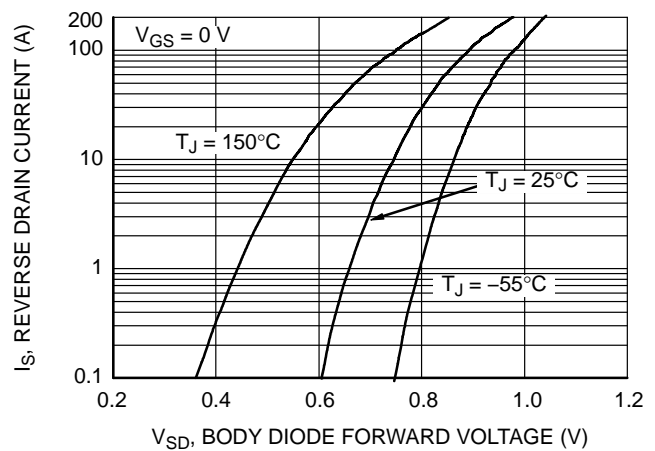


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

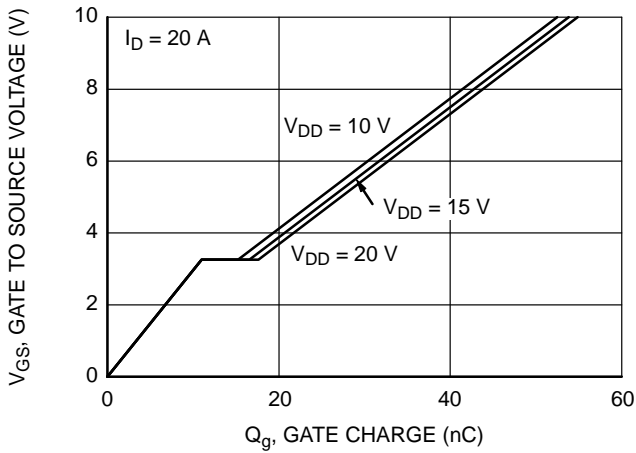


Figure 7. Gate Charge Characteristics

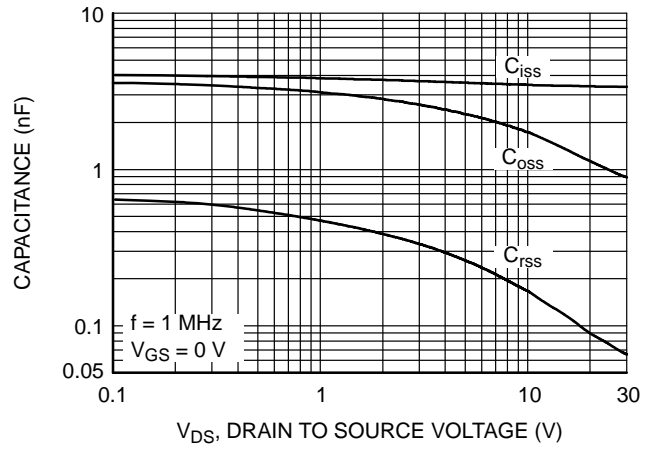


Figure 8. Capacitance vs. Drain to Source Voltage

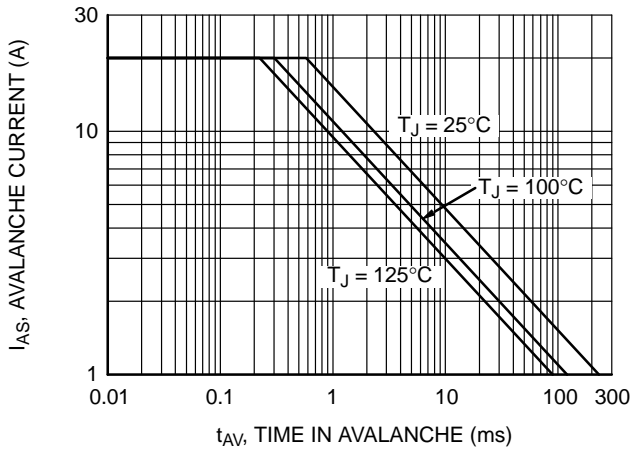


Figure 9. Unclamped Inductive Switching Capability

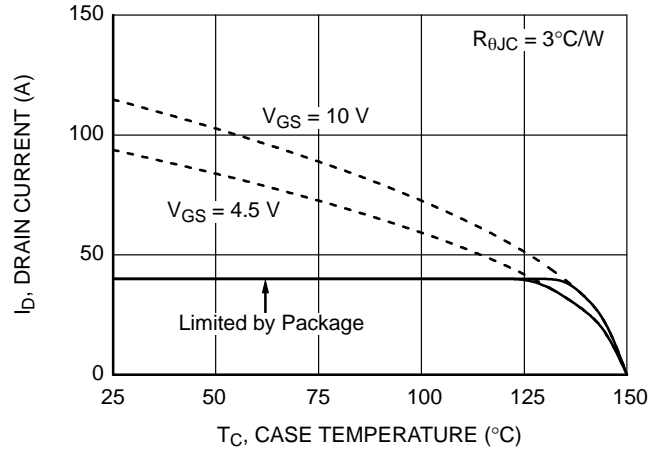


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

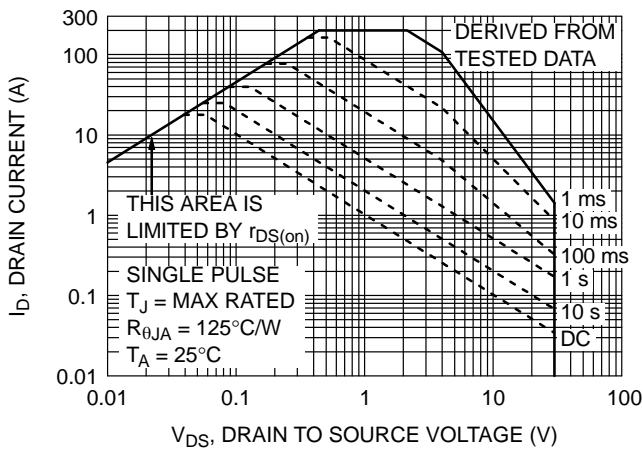


Figure 11. Forward Bias Safe Operating Area

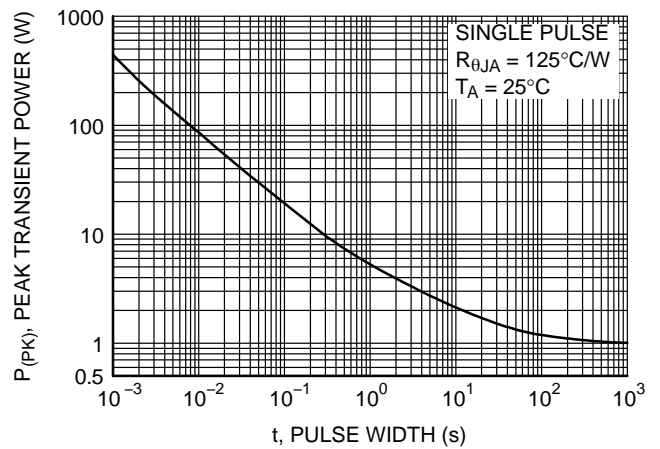


Figure 12. Single Pulse Maximum Power Dissipation

# FDMC7660

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

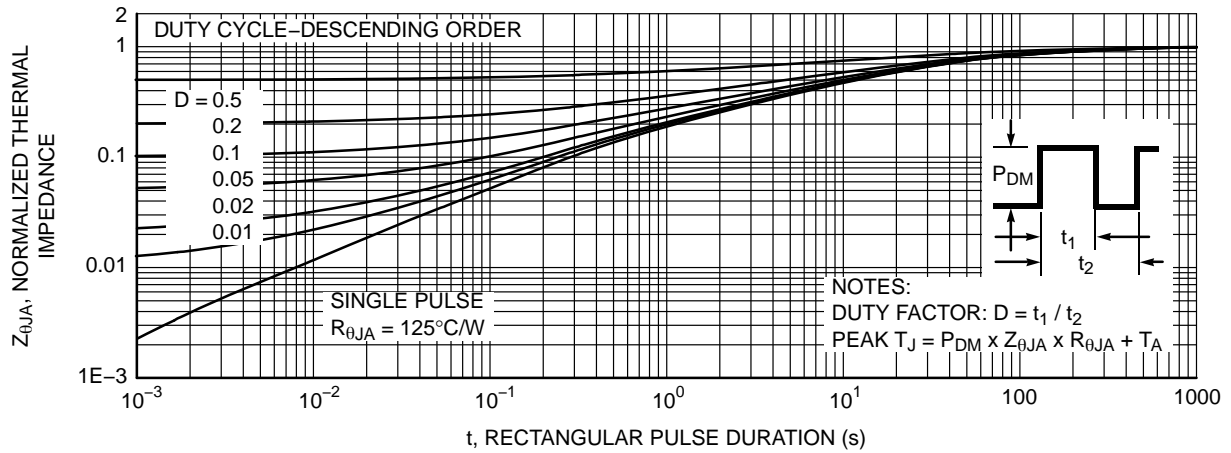


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

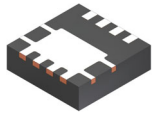
### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC7660	FDMC7660	PQFN8 3.3X3.3, 0.65P (Power 33) (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

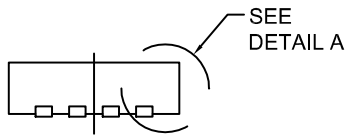


**PQFN8 3.3X3.3, 0.65P**  
**CASE 483AK**  
**ISSUE B**

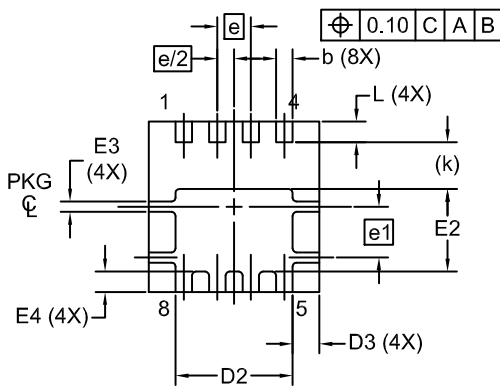
DATE 12 OCT 2021



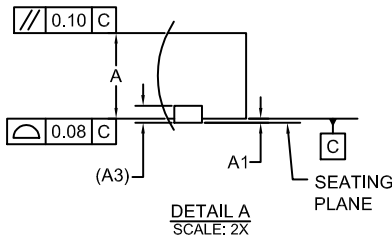
TOP VIEW



FRONT VIEW



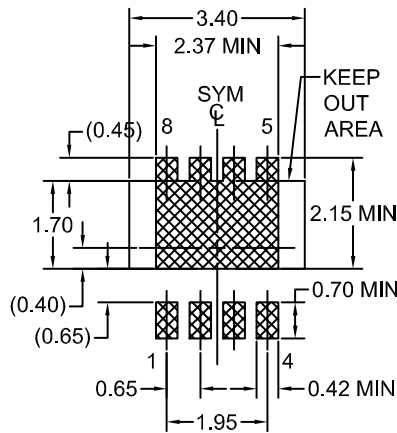
BOTTOM VIEW



DETAIL A  
SCALE: 2X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



LAND PATTERN  
RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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<b>DESCRIPTION:</b>	<b>PQFN8 3.3X3.3, 0.65P</b>	<b>PAGE 1 OF 1</b>

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