

N-channel Enhancement Mode Power MOSFET

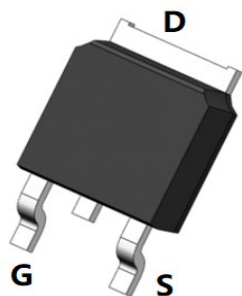
Features

- $V_{DS} = 250$, $I_D = 30$ A
 $R_{DS(ON)} < 800 \text{ m}\Omega$ @ $V_{GS} = 10\text{V}$
 $R_{DS(ON)} < 960 \text{ m}\Omega$ @ $V_{GS} = 4.5\text{V}$

General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

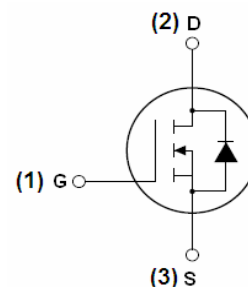
100% UIS TESTED!
100% ΔV_{ds} TESTED!



TO-252-2L Top View



Pin Assignment



Schematic Diagram

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	250	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	4.5	A
		T _C = 100 °C		3.0	
Pulsed Drain Current ^a			I _{DM}	16	W/°C
Linear Derating Factor				0.33	
Linear Derating Factor (PCB Mount) ^e				0.020	
Single Pulse Avalanche Energy ^b			E _{AS}	130	mJ
Repetitive Avalanche Current ^a			I _{AR}	4.5	A
Repetitive Avalanche Energy ^a			E _{AR}	5.2	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	45	W
Maximum Power Dissipation (PCB Mount) ^e	T _A = 25 °C			2.5	
Peak Diode Recovery dV/dt ^c			dV/dt	4.8	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s			260	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50 \text{ V}$; starting $T_J = 25^\circ\text{C}$, $L = 14 \text{ mH}$, $R_g = 25 \Omega$, $I_{AS} = 3.8 \text{ A}$ (see fig. 12).
- $I_{SD} \leq 3.8 \text{ A}$, $dI/dt \leq 90 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	50	°C/W
Maximum Junction-to-Ambient	R_{thJA}	-	110	
Maximum Junction-to-Case	R_{thJC}	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		250	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.36	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 250 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 200 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.3 A ^b	-	-	0.8	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.3 A ^b		1.5	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^c		-	260	-	pF
Output Capacitance	C _{oss}			-	77	-	
Reverse Transfer Capacitance	C _{rss}			-	15	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 4.4 A, V _{DS} = 200 V, see fig. 6 and 13 ^{b, c}	-	-	14	nC
Gate-Source Charge	Q _{gs}			-	-	2.7	
Gate-Drain Charge	Q _{gd}			-	-	7.8	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 125 V, I _D = 4.4 A, R _G = 18 Ω, R _D = 28 Ω, see fig. 10 ^{b, c}		-	7.0	-	ns
Rise Time	t _r			-	13	-	
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Fall Time	t _f			-	12	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.8	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	15	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 3.8 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4.4 A, dI/dt = 100 A/μs ^b		-	200	400	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.93	1.9	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

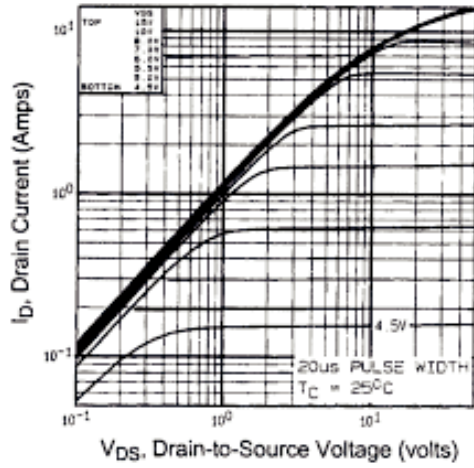


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

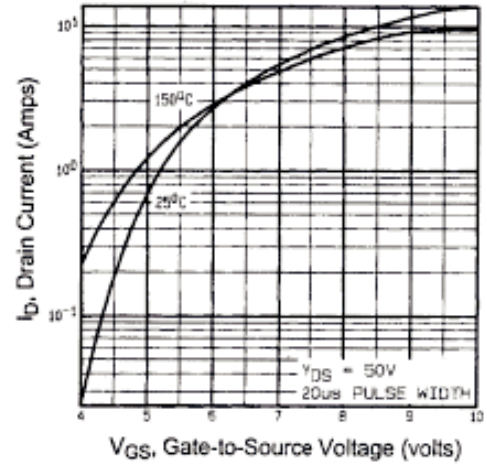


Fig. 3 - Typical Transfer Characteristics

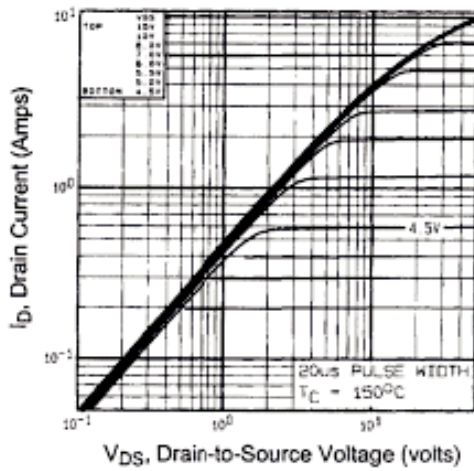


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

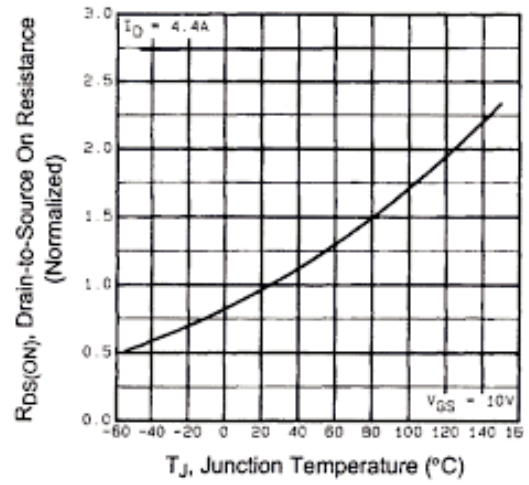


Fig. 4 - Normalized On-Resistance vs. Temperature

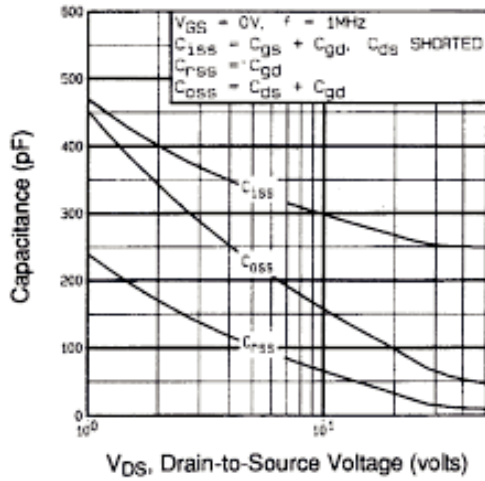


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

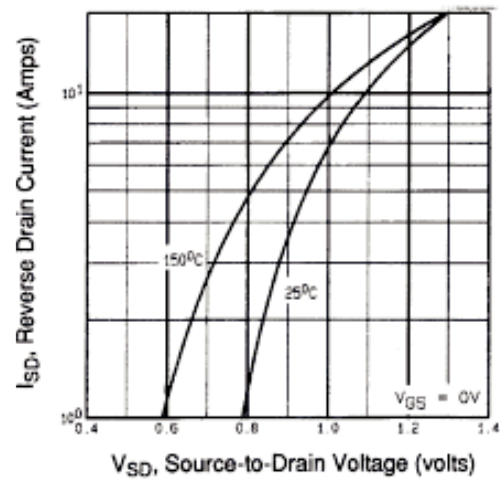


Fig. 7 - Typical Source-Drain Diode Forward Voltage

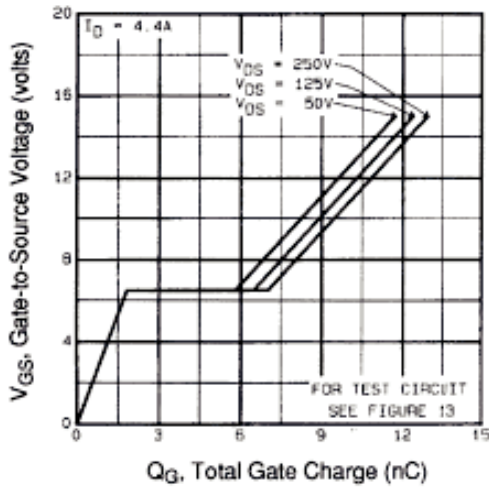


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

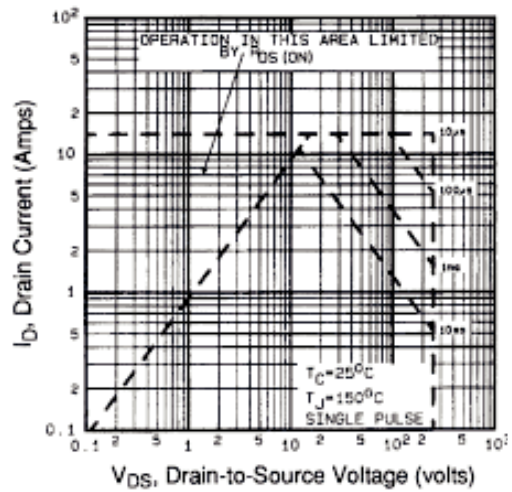


Fig. 8 - Maximum Safe Operating Area

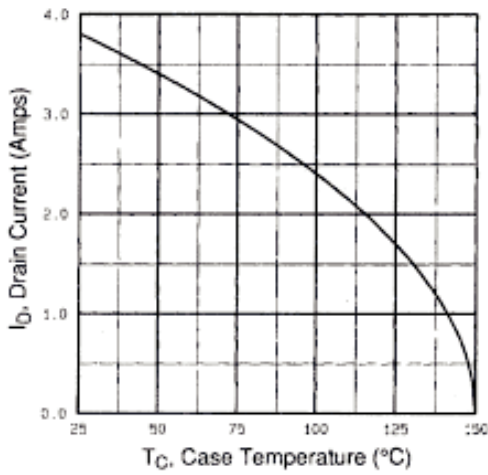


Fig. 9 - Maximum Drain Current vs. Case Temperature

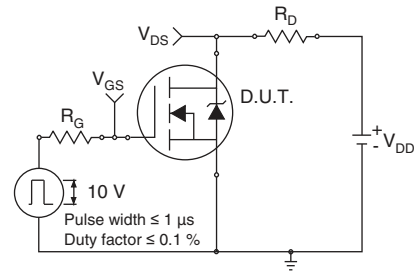


Fig. 10a - Switching Time Test Circuit

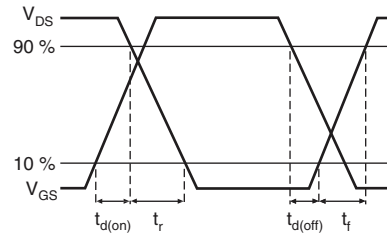


Fig. 10b - Switching Time Waveforms

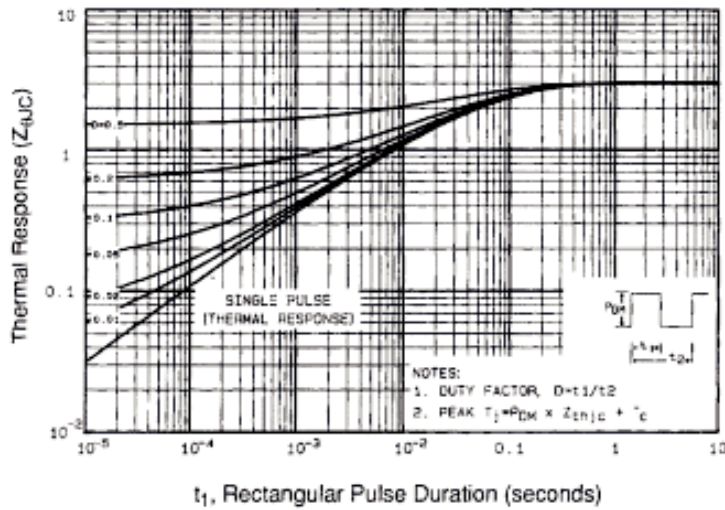


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

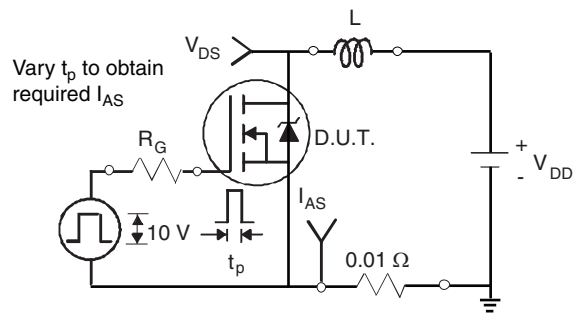


Fig. 12a - Unclamped Inductive Test Circuit

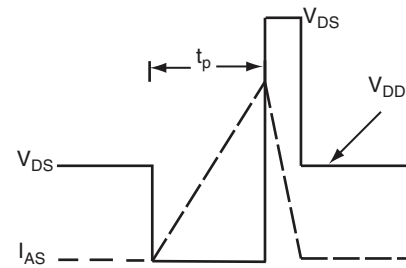


Fig. 12b - Unclamped Inductive Waveforms

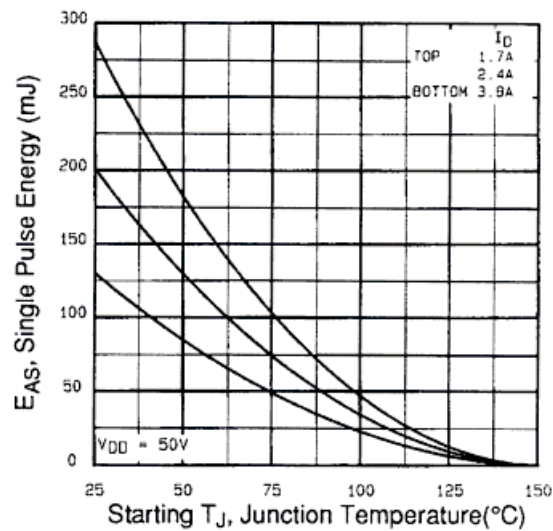


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

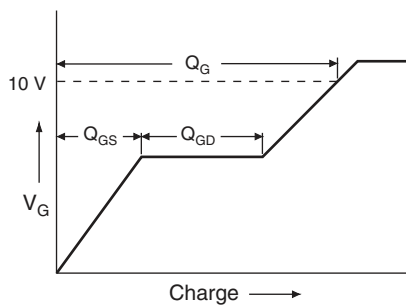


Fig. 13a - Basic Gate Charge Waveform

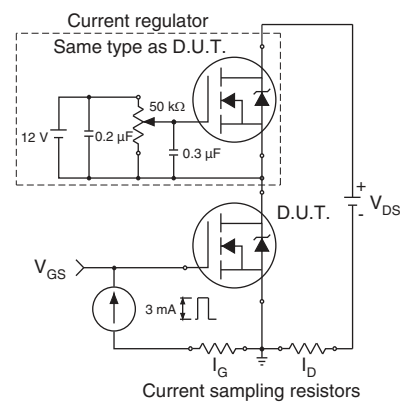
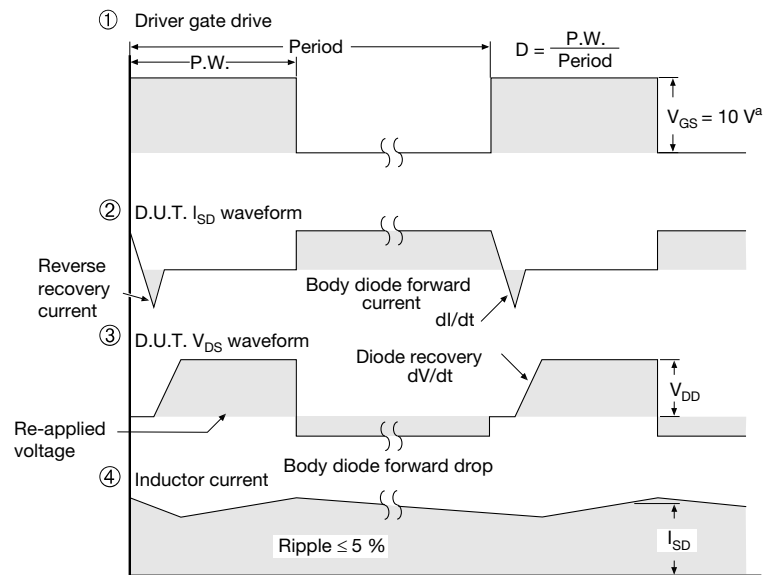
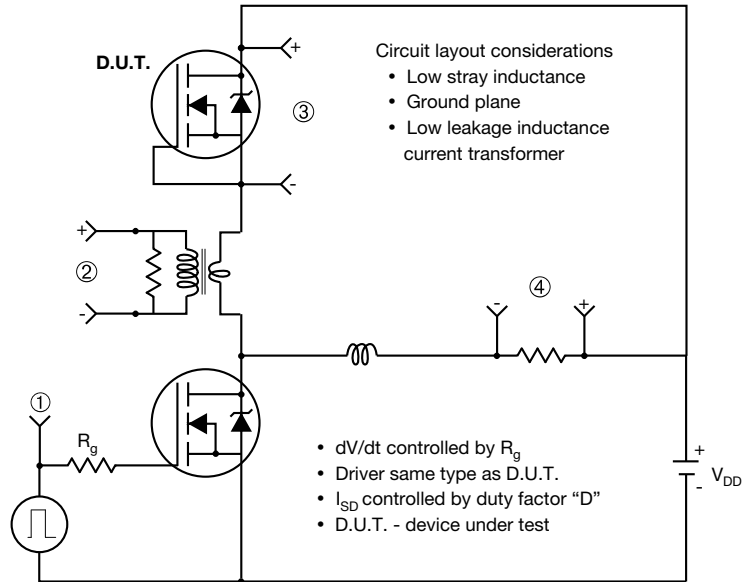


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel