24-Bit 2-/4-Channel ΔΣ ADC with Easy Drive Input Current Cancellation and I2C Interface

FEATURES

- **Up to 2 Differential or 4 Single-Ended Inputs**
- **Easy Drive™ Technology Enables Rail-to-Rail Inputs with Zero Differential Input Current**
- **Directly Digitizes High Impedance Sensors with Full Accuracy**
- **2-Wire I²C Interface with 9 Addresses Plus One Global Address for Synchronization**
- **600nV RMS Noise**
- **Integrated High Accuracy Temperature Sensor**
- **GND to V_{CC} Input/Reference Common Mode Range**
- Programmable 50Hz, 60Hz or Simultaneous 50Hz/60Hz Rejection Mode
- 2ppm INL, No Missing Codes
- 1ppm Offset and 15ppm Full-Scale Error
- 2× Speed/Reduced Power Mode (15Hz Using Internal Oscillator and 80μA at 7.5Hz Output)
- No Latency: Digital Filter Settles in a Single Cycle, Even After a New Channel Is Selected
- Single Supply 2.7V to 5.5V Operation (0.8mW)
- Internal Oscillator
- Tiny 4mm × 3mm DFN Package

APPLICATIONS

- Direct Sensor Digitizer
- Direct Temperature Measurement
- Instrumentation
- Industrial Process Control

DESCRIPTION

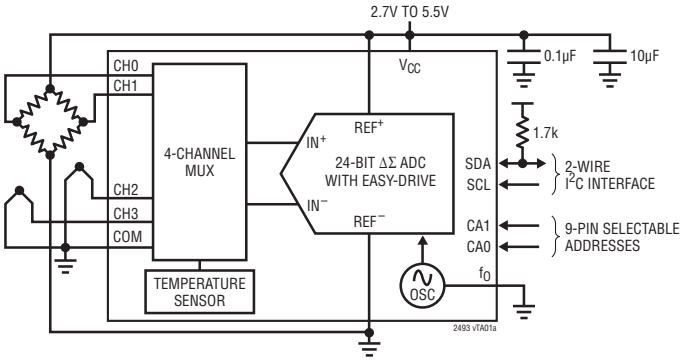
The LTC®2493 is a 4-channel (2-channel differential), 24-bit, No Latency ΔΣ™ ADC with Easy Drive technology and a 2-wire, I²C interface. The patented sampling scheme eliminates dynamic input current errors and the shortcomings of on-chip buffering through automatic cancellation of differential input current. This allows large external source impedances and rail-to-rail input signals to be directly digitized while maintaining exceptional DC accuracy.

The LTC2493 includes a high accuracy temperature sensor and an integrated oscillator. This device can be configured to measure an external signal (from combinations of 4 analog input channels operating in single-ended or differential modes) or its internal temperature sensor. The integrated temperature sensor offers 1/30th °C resolution and 2°C absolute accuracy.

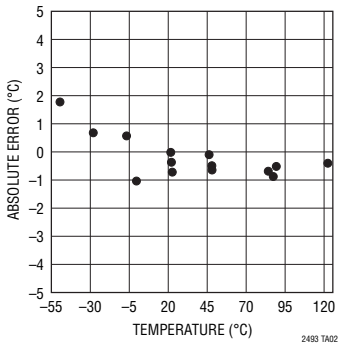
The LTC2493 allows a wide common mode input range (0V to V_{CC}), independent of the reference voltage. Any combination of single-ended or differential inputs can be selected and the first conversion, after a new channel is selected, is valid. Access to the multiplexer output enables optional external amplifiers to be shared between all analog inputs and auto-calibration continuously removes their associated offset and drift.

TYPICAL APPLICATION

Data Acquisition System with Temperature Compensation



Integrated High Performance Temperature Sensor

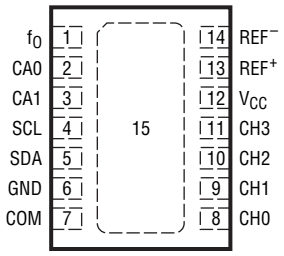


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) .....–0.3V to 6V
Analog Input Voltage
(CH0 to CH3, COM)..... –0.3V to (V_{CC} + 0.3V)
REF^+, REF^- ..... –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2493C ..... 0°C to 70°C
LTC2493I .....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2493CDE#PBF	LTC2493CDE#TRPBF	2493	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2493IDE#PBF	LTC2493IDE#TRPBF	2493	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (NORMAL SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)		24			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	● ●		2 1	10	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 13)	●		0.5	2.5	µV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}			0.1		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V 5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V			15 15 15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	2.7V < V_{CC} < 5.5V, 2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 12)			0.6		μV_{RMS}
Internal PTAT Signal	T_A = 27°C (Note 13)		27.8	28.0	28.2	mV
Internal PTAT Temperature Coefficient				93.5		µV/°C

ELECTRICAL CHARACTERISTICS (2X SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)		24			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	●		2 1	10	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 13)	●		0.2	2	mV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC}			100		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}			0.1		ppm of V_{REF}/°C
Output Noise	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, GND ≤ IN^+ = IN^- ≤ V_{CC}			0.85		μV_{RMS}

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common Mode Rejection DC	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 5)	●	140			dB
Input Common Mode Rejection 50Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 7)	●	140			dB
Input Common Mode Rejection 60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 8)	●	140			dB
Input Normal Mode Rejection 50Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 7)	●	110	120		dB
Input Normal Mode Rejection 60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 8)	●	110	120		dB
Input Normal Mode Rejection 50Hz/60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 9)	●	87			dB
Reference Common Mode Rejection DC	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 5)	●	120	140		dB
Power Supply Rejection DC	V_{REF} = 2.5V, IN^+ = IN^- = GND			120		dB
Power Supply Rejection, 50Hz ±2%, 60Hz ±2%	V_{REF} = 2.5V, IN^+ = IN^- = GND (Notes 7, 8, 9)			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage (IN^+ Corresponds to the Selected Positive Input Channel)			GND – 0.3V		V_{CC} + 0.3V	V
IN^-	Absolute/Common Mode IN^- Voltage (IN^- Corresponds to the Selected Negative Input Channel to COM)			GND – 0.3V		V_{CC} + 0.3V	V
V_{IN}	Input Voltage Range ($IN^+ – IN^-$)	Differential/Single-Ended	●	–FS		+FS	V
FS	Full-Scale of the Input ($IN^+ – IN^-$)	Differential/Single-Ended	●	$0.5V_{REF}$			V
LSB	Least Significant Bit of the Output Code		●	$FS/2^{24}$			
REF^+	Absolute/Common Mode REF^+ Voltage		●	0.1		V_{CC}	V
REF^-	Absolute/Common Mode REF^- Voltage		●	GND		$REF^+ – 0.1V$	V
V_{REF}	Reference Voltage Range ($REF^+ – REF^-$)		●	0.1		V_{CC}	V
$CS(IN^+)$	IN^+ Sampling Capacitance				11		pF
$CS(IN^-)$	IN^- Sampling Capacitance				11		pF
$CS(V_{REF})$	V_{REF} Sampling Capacitance				11		pF
$I_{DC\_LEAK(IN^+)}$	IN^+ DC Leakage Current	Sleep Mode, IN^+ = GND	●	–10	1	10	nA
$I_{DC\_LEAK(IN^-)}$	IN^- DC Leakage Current	Sleep Mode, IN^- = GND	●	–10	1	10	nA
$I_{DC\_LEAK(REF^+)}$	REF^+ DC Leakage Current	Sleep Mode, $REF^+ = V_{CC}$	●	–100	1	100	nA
$I_{DC\_LEAK(REF^-)}$	REF^- DC Leakage Current	Sleep Mode, REF^- = GND	●	–100	1	100	nA
t_{OPEN}	MUX Break-Before-Make				50		ns
QIRR	MUX Off Isolation	$V_{IN} = 2V_{P-P}$ DC to 1.8MHz			120		dB

I²C INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	$0.7V_{CC}$			V
V_{IL}	Low Level Input Voltage		●			$0.3V_{CC}$	V
V_{IHA}	Low Level Input Voltage for Address Pins CA0, CA1 and Pin f_O		●			$0.05V_{CC}$	V
V_{ILA}	High Level Input Voltage for Address Pins CA0, CA1		●	$0.95V_{CC}$			V
R_{INH}	Resistance from CA0, CA1 to V_{CC} to Set Chip Address Bit to 1		●			10	kΩ
R_{INL}	Resistance from CA0, CA1 to GND to Set Chip Address Bit to 0		●			10	kΩ
R_{INF}	Resistance from CA0, CA1 to GND or V_{CC} to Set Chip Address Bit to Float		●	2			MΩ
I_I	Digital Input Current (f_O)		●	–10		10	µA
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	(Note 5)	●	$0.05V_{CC}$			V
V_{OL}	Low Level Output Voltage (SDA)	I = 3mA	●			0.4	V
t_{OF}	Output Fall Time $V_{IH(MIN)}$ to $V_{IL(MAX)}$	Bus Load C_B 10pF to 400pF (Note 14)	●	$20 + 0.1C_B$		250	ns
I_{IN}	Input Leakage (SDA, SCL)	$0.1V_{CC} \le V_{IN} \le 0.9V_{CC}$	●			1	µA
C_{CAX}	External Capacitative Load On-Chip Address Pins (CA0, CA1) for Valid Float		●			10	pF

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Current (Note 11)	●		160	275	µA
		Temperature Measurement (Note 11)	●		200	300	µA
		Sleep Mode (Note 11)	●		1	2	µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		50	µs
t_{LEO}	External Oscillator Low Period		●	0.125		50	µs
t_{CONV_1}	Conversion Time for 1× Speed Mode	50Hz Mode	●	157.2	160.3	163.5	ms
		60Hz Mode	●	131	133.6	136.3	ms
		Simultaneous 50Hz/60Hz Mode	●	144.1	146.9	149.9	ms
		External Oscillator (Note 10)			41036/f_{EOSC} (in kHz)		ms
t_{CONV_2}	Conversion Time for 2× Speed Mode	50Hz Mode	●	78.7	80.3	81.9	ms
		60Hz Mode	●	65.6	66.9	68.2	ms
		Simultaneous 50Hz/60Hz Mode	●	72.2	73.6	75.1	ms
		External Oscillator (Note 10)			20556/f_{EOSC} (in kHz)		ms

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3, 15)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
t_f	Fall Time for SDA Signals	(Note 14)	●	20 + 0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified: V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $f_S = 0.5V_{REF}$

$V_{IN} = IN^+ – IN^–$, $V_{IN(CM)} = (IN^+ – IN^–)/2$,
where IN^+ and $IN^–$ are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 11: The converter uses its internal oscillator.

Note 12: The output noise includes the contribution of the internal calibration operations.

Note 13: Guaranteed by design and test correlation.

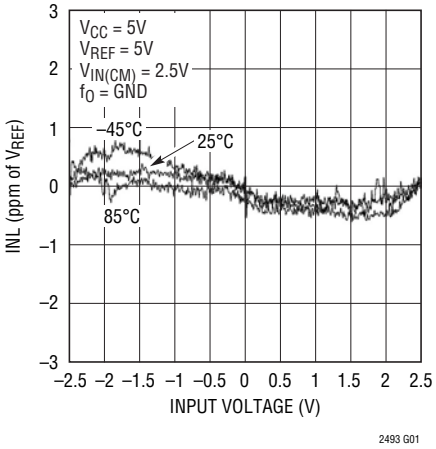
Note 14: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 15: All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

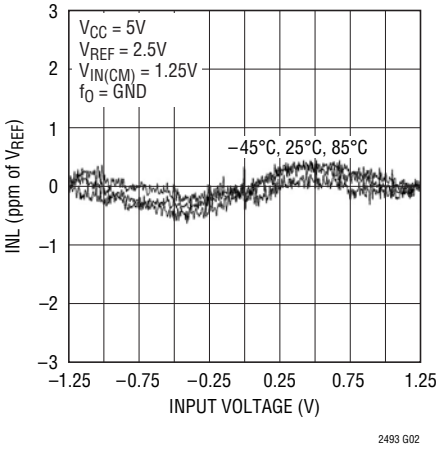
Note 16: Refer to Applications Information section for Performance vs Data Rate graphs.

TYPICAL PERFORMANCE CHARACTERISTICS

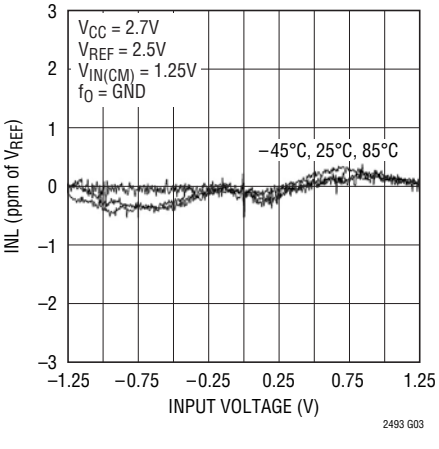
Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 5V)



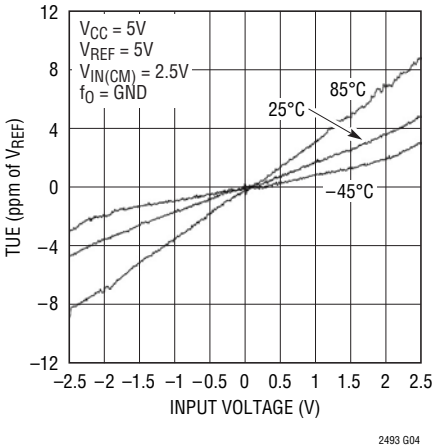
Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 2.5V)



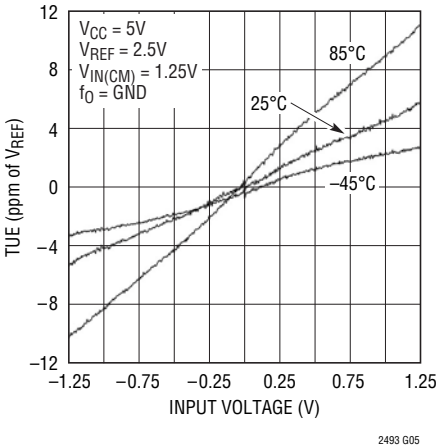
Integral Nonlinearity (V_{CC} = 2.7V, V_{REF} = 2.5V)



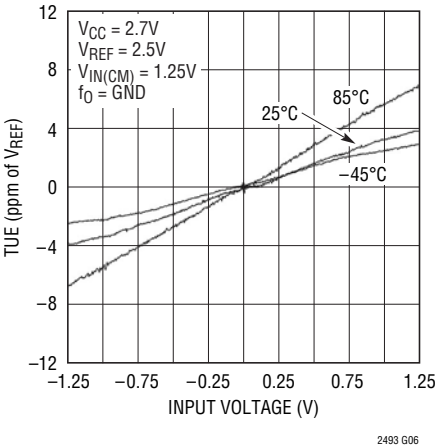
Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 5V)



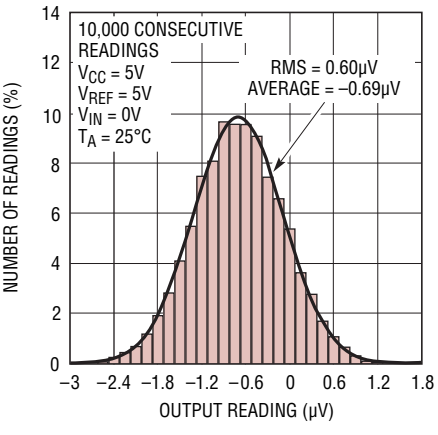
Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 2.5V)



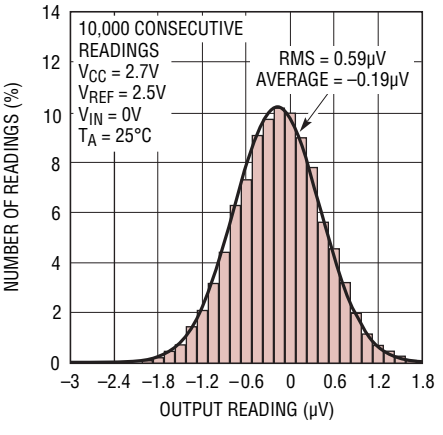
Total Unadjusted Error (V_{CC} = 2.7V, V_{REF} = 2.5V)



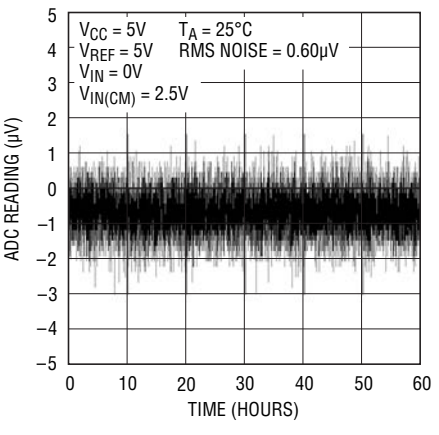
Noise Histogram (6.8sps)



Noise Histogram (7.5sps)

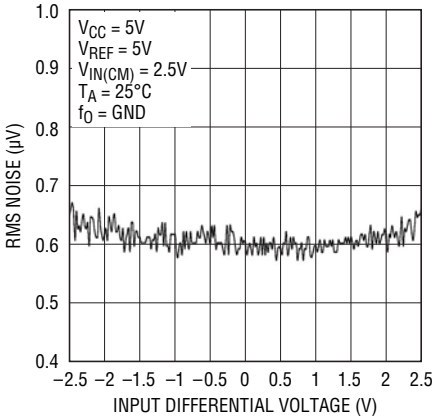


Long-Term ADC Readings

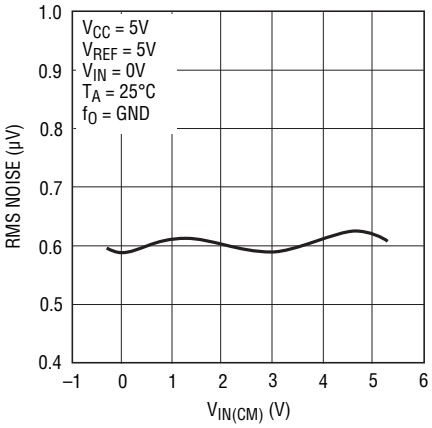


TYPICAL PERFORMANCE CHARACTERISTICS

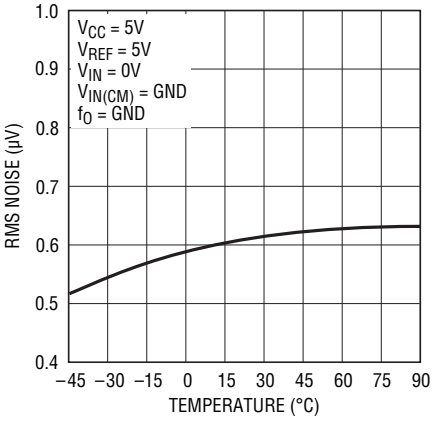
RMS Noise vs Input Differential Voltage



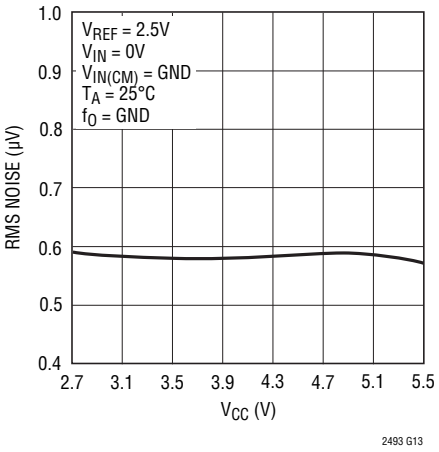
RMS Noise vs $V_{IN(CM)}$



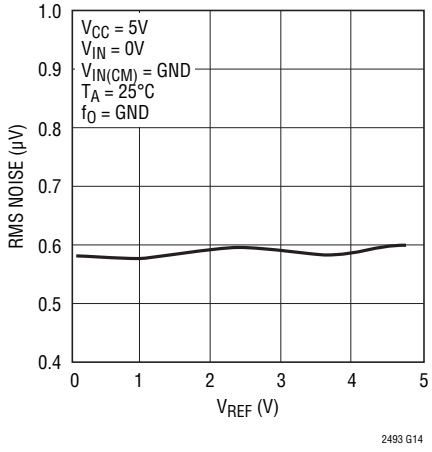
RMS Noise vs Temperature (T_A)



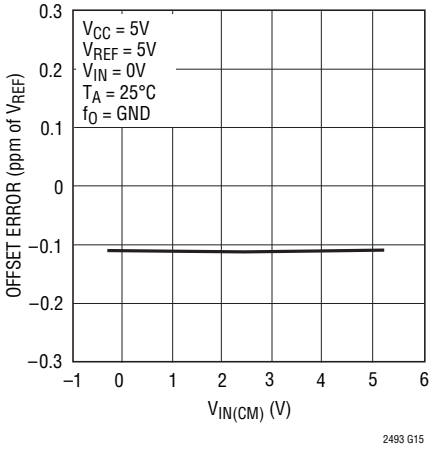
RMS Noise vs V_{CC}



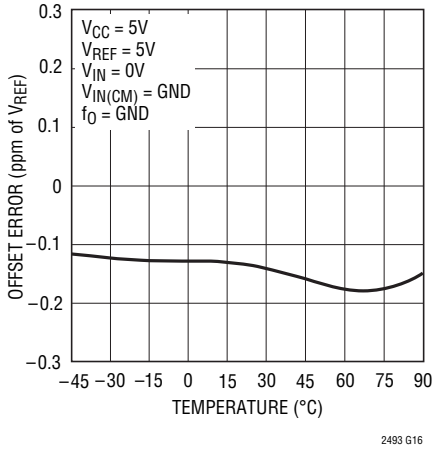
RMS Noise vs V_{REF}



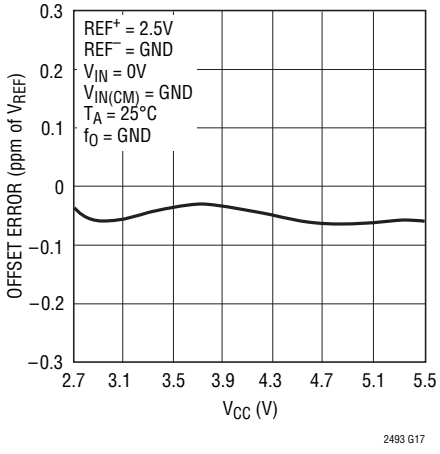
Offset Error vs $V_{IN(CM)}$



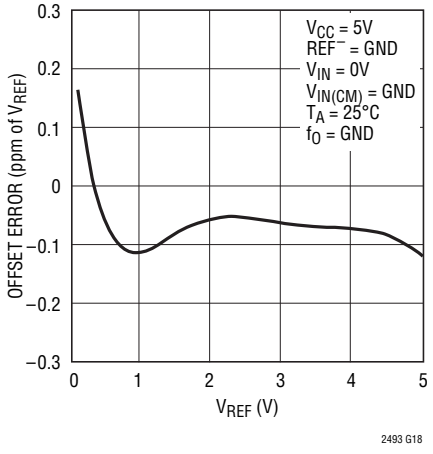
Offset Error vs Temperature



Offset Error vs V_{CC}

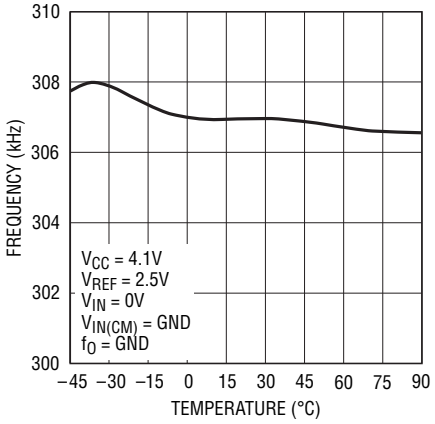


Offset Error vs V_{REF}



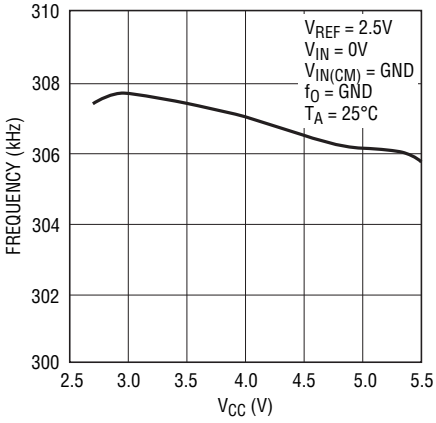
TYPICAL PERFORMANCE CHARACTERISTICS

On-Chip Oscillator Frequency vs Temperature



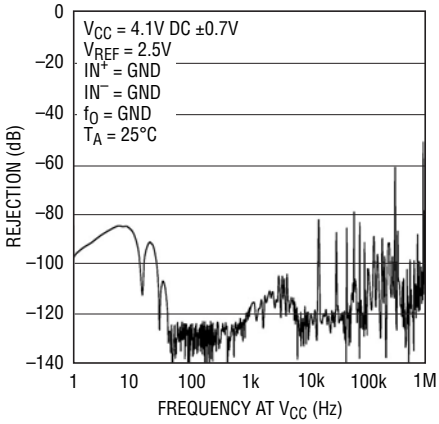
2493 G19

On-Chip Oscillator Frequency vs V_{CC}



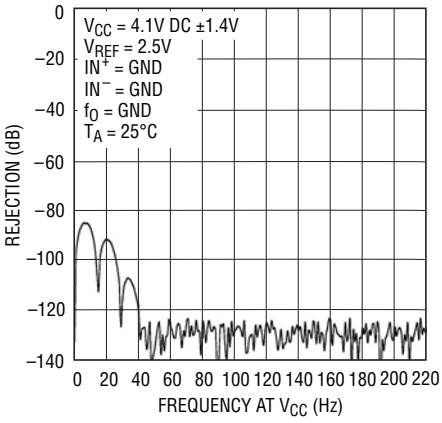
2493 G20

PSRR vs Frequency at V_{CC}



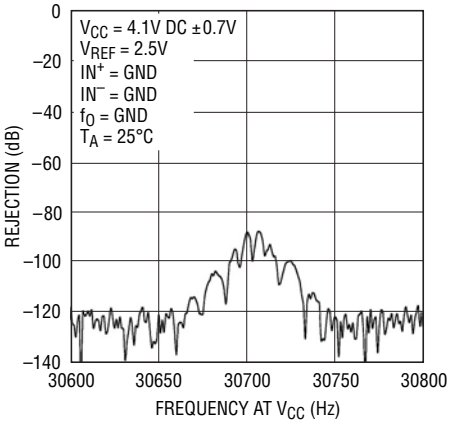
2493 G21

PSRR vs Frequency at V_{CC}



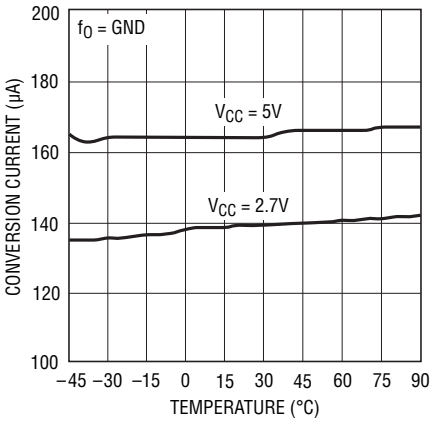
2493 G22

PSRR vs Frequency at V_{CC}



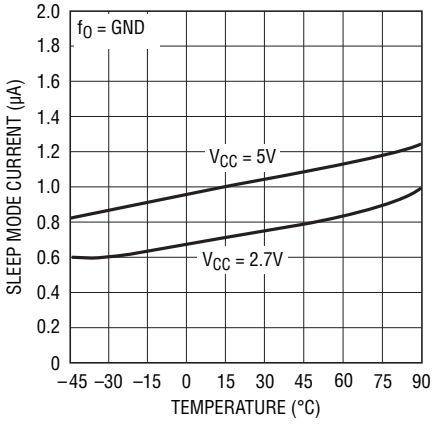
2493 G23

Conversion Current vs Temperature



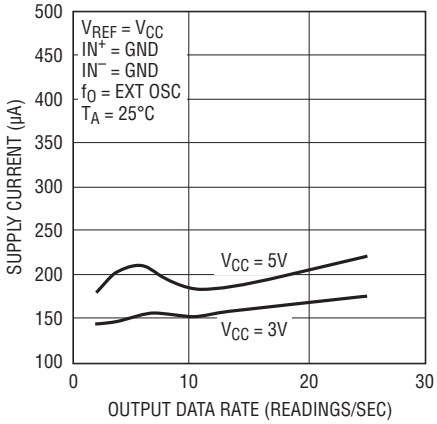
2493 G24

Sleep Mode Current vs Temperature



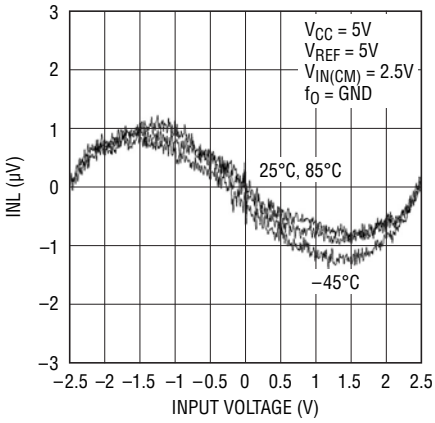
2493 G25

Conversion Current vs Output Data Rate



2493 G26

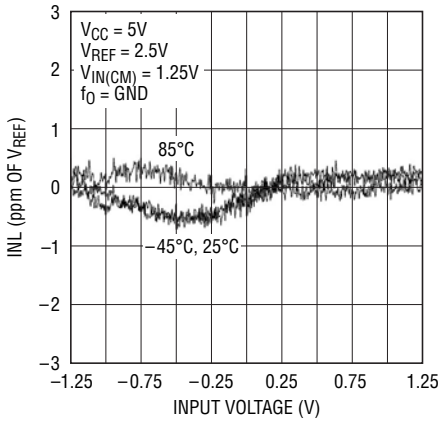
Integral Nonlinearity (2x Speed Mode; V_{CC} = 5V, V_{REF} = 5V)



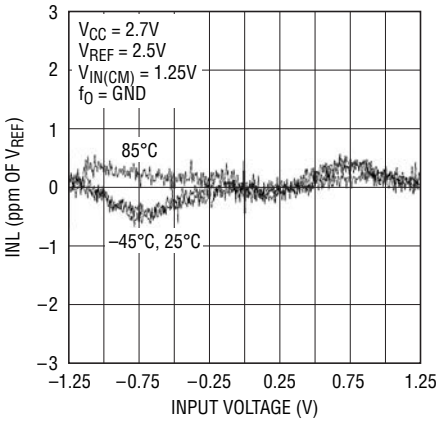
2493 G27

TYPICAL PERFORMANCE CHARACTERISTICS

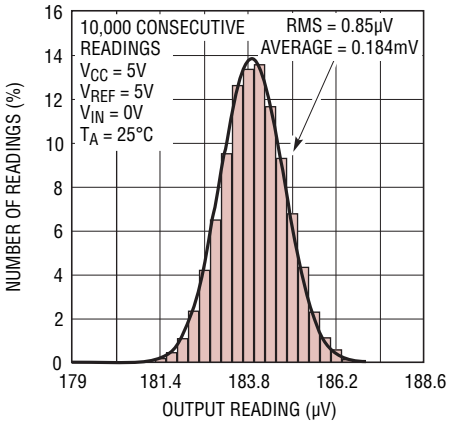
Integral Nonlinearity (2x Speed Mode; V_{CC} = 5V, V_{REF} = 2.5V)



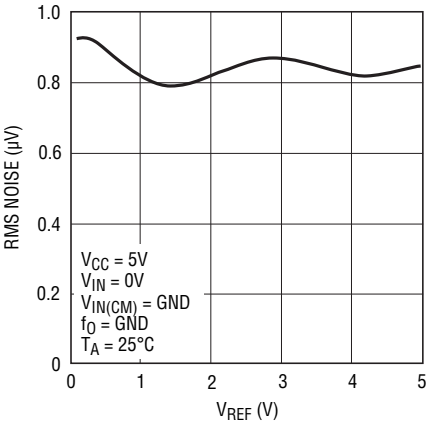
Integral Nonlinearity (2x Speed Mode; V_{CC} = 2.7V, V_{REF} = 2.5V)



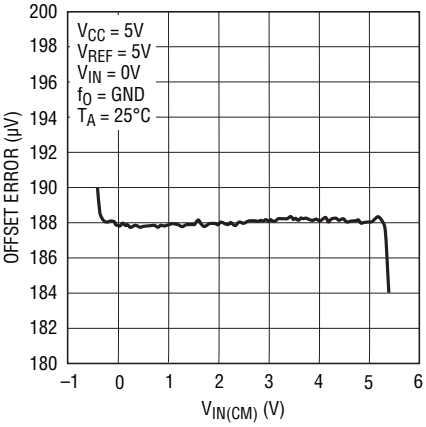
Noise Histogram (2x Speed Mode)



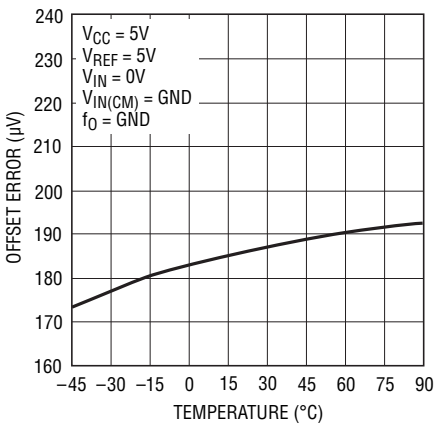
RMS Noise vs V_{REF} (2x Speed Mode)



Offset Error vs $V_{IN(CM)}$ (2x Speed Mode)

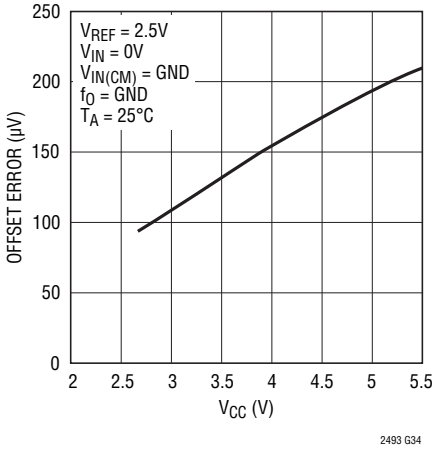


Offset Error vs Temperature (2x Speed Mode)

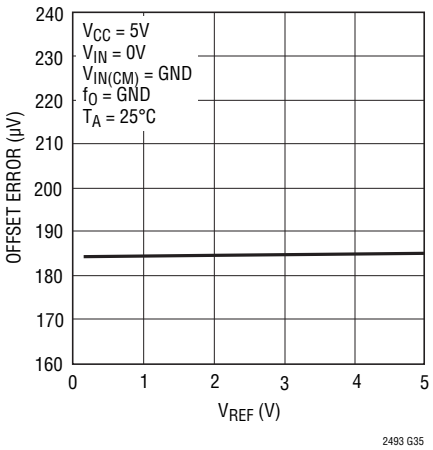


TYPICAL PERFORMANCE CHARACTERISTICS

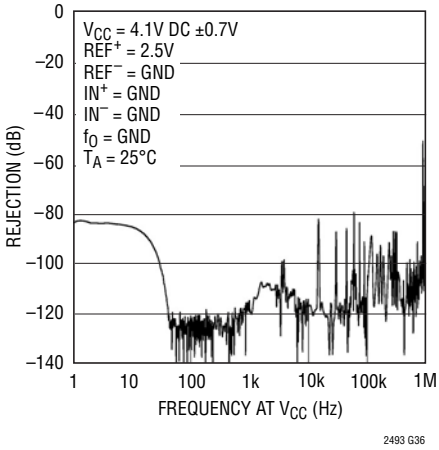
Offset Error vs V_{CC} (2x Speed Mode)



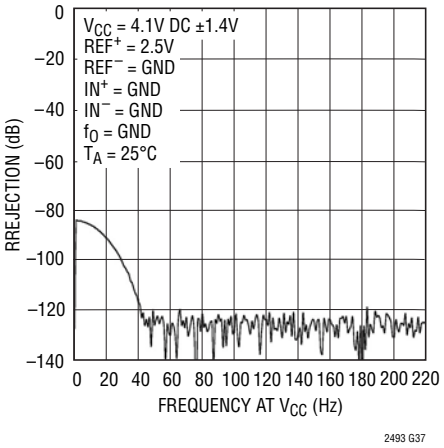
Offset Error vs V_{REF} (2x Speed Mode)



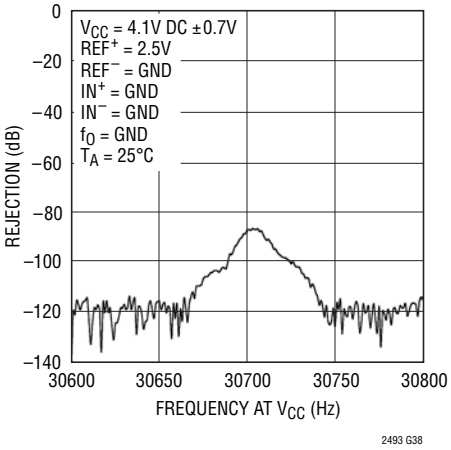
PSRR vs Frequency at V_{CC} (2x Speed Mode)



PSRR vs Frequency at V_{CC} (2x Speed Mode)



PSRR vs Frequency at V_{CC} (2x Speed Mode)



PIN FUNCTIONS

f_O (Pin 1): Frequency Control Pin. Digital input that controls the internal conversion clock rate. When f_O is connected to GND, the converter uses its internal oscillator running at 307.2kHz. The conversion clock may also be overridden by driving the f_O pin with an external clock in order to change the output rate and the digital filter rejection null.

CA0, CA1 (Pins 2, 3): Chip Address Control Pins. These pins are configured as a three-state (LOW, HIGH, floating) address control bits for the device's I^2C address.

SCL (Pin 4): Serial Clock Pin of the I^2C Interface. The LTC2493 can only act as a slave and the SCL pin only accepts an external serial clock. Data is shifted into the SDA pin on the rising edges of the SCL clock and output through the SDA pin on the falling edges of the SCL clock.

SDA (Pin 5): Bidirectional Serial Data Line of the I^2C Interface. In the transmitter mode (read), the conversion result is output through the SDA pin, while in the receiver mode (write), the device channel select and configuration bits are input through the SDA pin. The pin is high impedance during the data input mode and is an open-drain output (requires an appropriate pull-up device to V_{CC}) during the data output mode.

GND (Pin 6): Ground. Connect this pin to a common ground plane through a low impedance connection.

COM (Pin 7): The Common Negative Input (IN^-) for All Single-Ended Multiplexer Configurations. The voltage on CH0-CH3 and COM pins can have any value between GND – 0.3V to V_{CC} + 0.3V. Within these limits, the two selected inputs (IN^+ and IN^-) provide a bipolar input range ($V_{IN} = IN^+ – IN^-$) from $–0.5 • V_{REF}$ to $0.5 • V_{REF}$. Outside this input range, the converter produces unique over-range and underrange output codes.

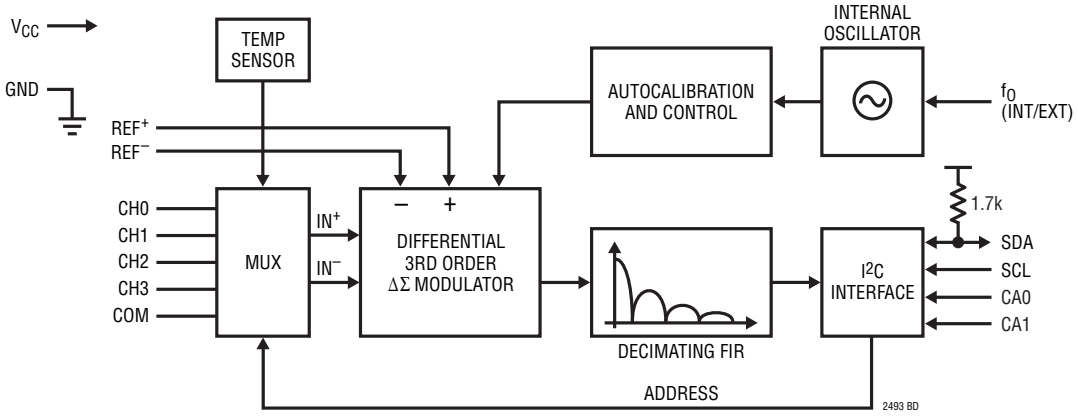
CH0 to CH3 (Pin 8-Pin 11): Analog Inputs. May be programmed for single-ended or differential mode.

V_{CC} (Pin 12): Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor as close to the part as possible.

REF^+, REF^- (Pin 13, Pin 14): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF^+, remains more positive than the negative reference input, REF^-, by at least 0.1V. The differential voltage ($V_{REF} = REF^+ – REF^-$) sets the full-scale range for all input channels. When performing an on-chip temperature measurement, the minimum value of REF = 2V.

Exposed Pad (Pin 15): Ground. This pin is ground and must be soldered to the PCB ground plane. For prototyping purposes, this pin may remain floating.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2493 is a multichannel, low power, delta-sigma analog-to-digital converter with a 2-wire, I^2C interface. Its operation is made up of four states (see Figure 1). The converter operating cycle begins with the conversion, followed by the sleep state and ends with the data input/output cycle.

Initially, at power-up, the LTC2493 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in the sleep state, power consumption is reduced by two orders of magnitude. The part remains in the sleep state as long it is not addressed for a read/write operation. The conversion result is held indefinitely in a static shift register while the part is in the sleep state.

The device will not acknowledge an external request during the conversion state. After a conversion is finished, the device is ready to accept a read/write request. Once the LTC2493 is addressed for a read operation, the device begins outputting the conversion result under the control of the serial clock (SCL). There is no latency in the conversion result. The data output is 32 bits long and contains a 24-bit plus sign conversion result. Data is updated on the falling edges of SCL allowing the user to reliably latch data on the rising edge of SCL. A new conversion is initiated by a STOP condition following a valid write operation or an incomplete read operation. The conversion automatically begins at the conclusion of a complete read cycle (all 32 bits read out of the device).

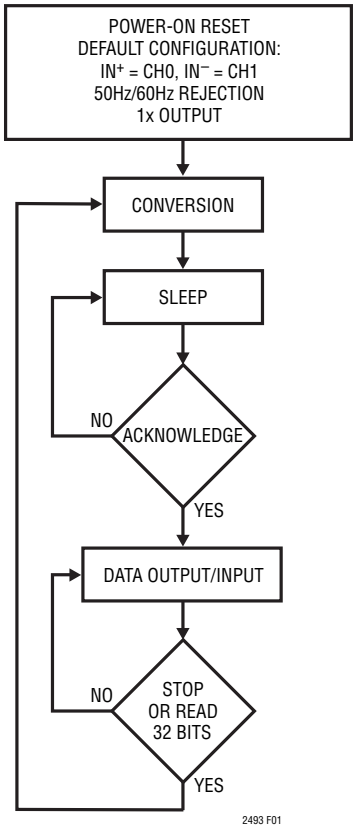


Figure 1. State Transition Table

Ease of Use

The LTC2493 data output has no latency, filter settling delay, or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog inputs is straightforward. Each conversion, immediately following a newly selected input or mode, is valid and accurate to the full specifications of the device.

The LTC2493 automatically performs offset and full-scale calibration every conversion cycle independent of the input channel selected. This calibration is transparent to the user and has no effect on the operation cycle previously described. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage variation, input channel and temperature drift.

Easy Drive Input Current Cancellation

The LTC2493 combines a high precision, delta-sigma ADC with an automatic, differential, input current cancellation front end. A proprietary front end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2493 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see the Automatic Differential Input Current Cancellation section). This unique

APPLICATIONS INFORMATION

architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full-scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2493 automatically enters an internal reset state when the power supply voltage, V_{CC}, drops below approximately 2.0V. This feature guarantees the integrity of the conversion result and input channel selection.

When V_{CC} rises above this threshold, the converter creates an internal power-on reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1 with simultaneous 50Hz/60Hz rejection and 1x output rate. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, or temperature selection can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2493 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits and, as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The LTC2493 input measurement range is $-0.5 \bullet V_{REF}$ to $+0.5 \bullet V_{REF}$ in both differential and single-ended configurations as shown in Figure 37. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 37b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

The analog inputs are truly differential with an absolute, common mode range for the CH0-CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2493 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from $-FS = -0.5 \bullet V_{REF}$ to $+FS = 0.5 \bullet V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

I²C INTERFACE

The LTC2493 communicates through an I^2C interface. The I^2C interface is a 2-wire open-drain interface supporting multiple devices and multiple masters on a single bus. The connected devices can only pull the data line (SDA) low and can never drive it high. SDA is required to be externally connected to the supply through a pull-up resistor. When the data line is not being driven, it is high. Data on the I^2C bus can be transferred at rates up to 100kbits/s in the standard mode and up to 400kbits/s in the fast mode. The V_{CC} power should not be removed from the device when the I^2C bus is active to avoid loading the I^2C bus lines through the internal ESD protection diodes.

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Each device on the I²C bus is recognized by a unique address stored in that device and can operate either as a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. Devices addressed by the master are considered a slave.

The LTC2493 can only be addressed as a slave. Once addressed, it can receive configuration bits (channel selection, rejection mode, speed mode) or transmit the last conversion result. The serial clock line, SCL, is always an input to the LTC2493 and the serial data line SDA is bidirectional. The device supports the standard mode and the fast mode for data transfer speeds up to 400kbits/s. Figure 2 shows the definition of the I²C timing.

The START and STOP Conditions

A START (S) condition is generated by transitioning SDA from high to low while SCL is high. The bus is considered to be busy after the START condition. When the data transfer is finished, a STOP (P) condition is generated by transitioning SDA from low to high while SCL is high. The bus is free after a STOP is generated. START and STOP conditions are always generated by the master.

When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START timing is functionally identical to the START and is used for writing and reading from the device before the initiation of a new conversion.

Data Transferring

After the START condition, the I²C bus is busy and data transfer can begin between the master and the addressed slave. Data is transferred over the bus in groups of nine bits, one byte followed by one acknowledge (ACK) bit. The master releases the SDA line during the ninth SCL clock cycle. The slave device can issue an ACK by pulling SDA low or issue a Not Acknowledge (NACK) by leaving the SDA line high impedance (the external pull-up resistor will hold the line high). Change of data only occurs while the clock line (SCL) is low.

DATA FORMAT

After a START condition, the master sends a 7-bit address followed by a read/write (R/W) bit. The R/W bit is 1 for a read request and 0 for a write request. If the 7-bit address matches the hard wired LTC2493's address (one of 9 pin-selectable addresses) the device is selected. When the device is addressed during the conversion state, it will not acknowledge R/W requests and will issue a NACK by leaving the SDA line high. If the conversion is complete, the LTC2493 issues an ACK by pulling the SDA line low.

The LTC2493 has two registers. The output register (32 bits long) contains the last conversion result. The input register (16 bits long) sets the input channel, selects the temperature sensor, rejection mode, and speed mode.

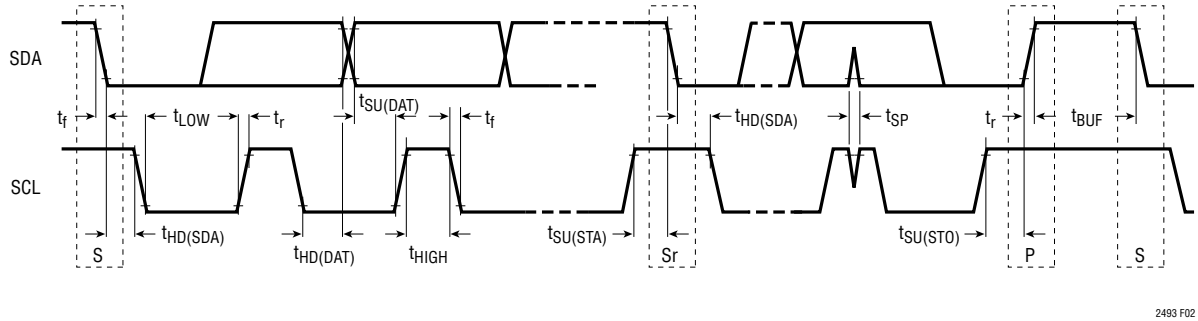

Figure 2. Definition of Timing for Fast/Standard Mode Devices on the I²C Bus

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DATA OUTPUT FORMAT

The output register contains the last conversion result. After each conversion is completed, the device automatically enters the sleep state where the supply current is reduced to 1µA. When the LTC2493 is addressed for a read operation, it acknowledges (by pulling SDA low) and acts as a transmitter. The master/receiver can read up to four bytes from the LTC2493. After a complete read operation (4 bytes), a new conversion is initiated. The device will NACK subsequent read operations while a conversion is being performed.

The data output stream is 32 bits long and is shifted out on the falling edges of SCL (see Figure 3a). The first bit is the conversion result sign bit (SIG) (see Tables 1 and 2). This bit is high if $V_{IN} \geq 0$ and low if $V_{IN} < 0$ (where V_{IN} corresponds to the selected input signal $IN^+ – IN^–$). The second bit is the most significant bit (MSB) of the result. The first two bits (SIG and MSB) can be used to indicate over and under range conditions (see Table 2). If both bits are high, the differential input voltage is equal to or above +FS. If both bits are set low, the input voltage is below –FS.

The function of these bits is summarized in Table 2. The 24 bits following the MSB bit are the conversion result in binary two's, complement format. The remaining six bits are sub LSBs below the 24-bit level.

As long as the voltage on the selected input channels (IN^+ and $IN^–$) remains between –0.3V and V_{CC} + 0.3V (absolute maximum operating range) a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to +FS. For differential input voltages below –FS, the conversion result is clamped to the value –FS – 1 LSB.

Table 2. LTC2493 Status Bits

INPUT RANGE	BIT 31 SIG	BIT 30 MSB
$V_{IN} \geq FS$	1	1
$0V \leq V_{IN} < FS$	1/0	0
$–FS \leq V_{IN} < 0V$	0	1
$V_{IN} < –FS$	0	0

Table 1. Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 SIG	BIT 30 MSB	BIT 29	BIT 28	BIT 27	…	BIT 6 LSB	BITS 5-0 Sub LSBs
V_{IN}* ≥ FS**	1	1	0	0	0	…	0	00000
FS** – 1 LSB	1	0	1	1	1	…	1	XXXXX
0.5 • FS**	1	0	1	0	0	…	0	XXXXX
0.5 • FS** – 1 LSB	1	0	0	1	1	…	1	XXXXX
0	1/0†	0	0	0	0	…	0	XXXXX
–1 LSB	0	1	1	1	1	…	1	XXXXX
–0.5 • FS**	0	1	1	0	0	…	0	XXXXX
–0.5 • FS** – 1 LSB	0	1	0	1	1	…	1	XXXXX
–FS**	0	1	0	0	0	…	0	XXXXX
V_{IN}* < –FS**	0	0	1	1	1	…	X	XXXXX‡

* The differential input voltage $V_{IN} = IN^+ – IN^–$.
** The full-scale voltage FS = 0.5 • V_{REF}. Sub LSBs are below the 24-bit level. They may be included in averaging, or discarded without loss of resolution.
† The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.
‡ The underrange output code is 0X3FFFFXXX in 2x mode.

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INPUT DATA FORMAT

The serial input word to the LTC2493 is 13 bits long and is written into the device input register in two 8-bit words. The first word (SGL, ODD, A2, A1, A0) is used to select the input channel. The second word of data (IM, FA, FB, SPD) is used to select the frequency rejection, speed mode (1×, 2×), and temperature measurement.

After power-up, the device initiates an internal reset cycle which sets the input channel to CH0-CH1 (IN^+ = CH0, IN^- = CH1), the frequency rejection to simultaneous 50Hz/60Hz, and 1× output rate (auto-calibration enabled). The first conversion automatically begins at power-up using this default configuration. Once the conversion is complete, up to two words may be written into the device.

The first three bits of the first input word consist of two preamble bits and one enable bit. Valid settings for these three bits are 000, 100, and 101. Other combinations should be avoided.

If the first three bits are 000 or 100, the following data is ignored (don't care) and the previously selected input channel remains valid for the next conversion.

If the first three bits shifted into the device are 101, then the next five bits select the input channel for the next conversion cycle (see Table 3).

Table 3. Channel Selection

MUX ADDRESS					CHANNEL SELECTION				
SGL	ODD/ SIGN	A2	A1	A0	0	1	2	3	COM
*0	0	0	0	0	IN^+	IN^-			
0	0	0	0	1			IN^+	IN^-	
0	1	0	0	0	IN^-	IN^+			
0	1	0	0	1			IN^-	IN^+	
1	0	0	0	0	IN^+				IN^-
1	0	0	0	1			IN^+		IN^-
1	1	0	0	0		IN^+			IN^-
1	1	0	0	1				IN^+	IN^-

*Default at power-up

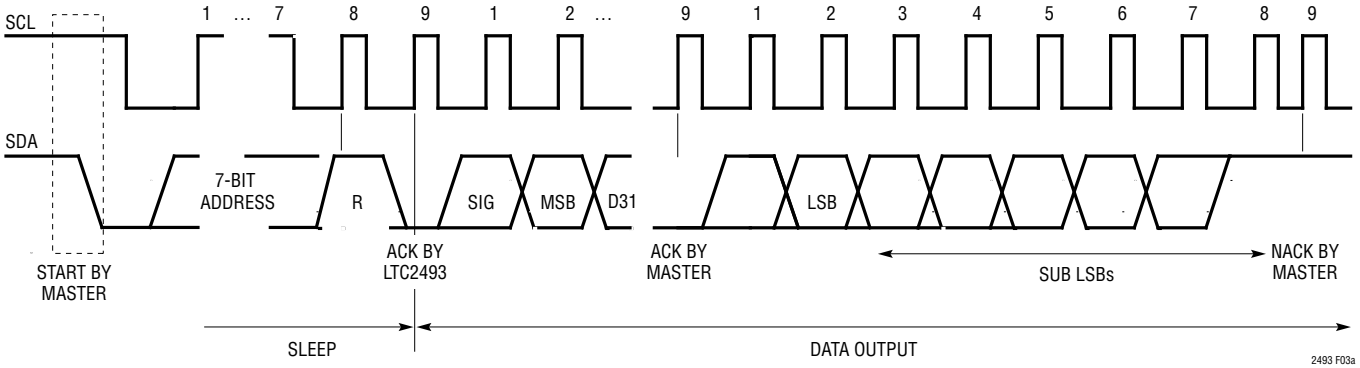

Figure 3a. Timing Diagram for Reading from the LTC2493

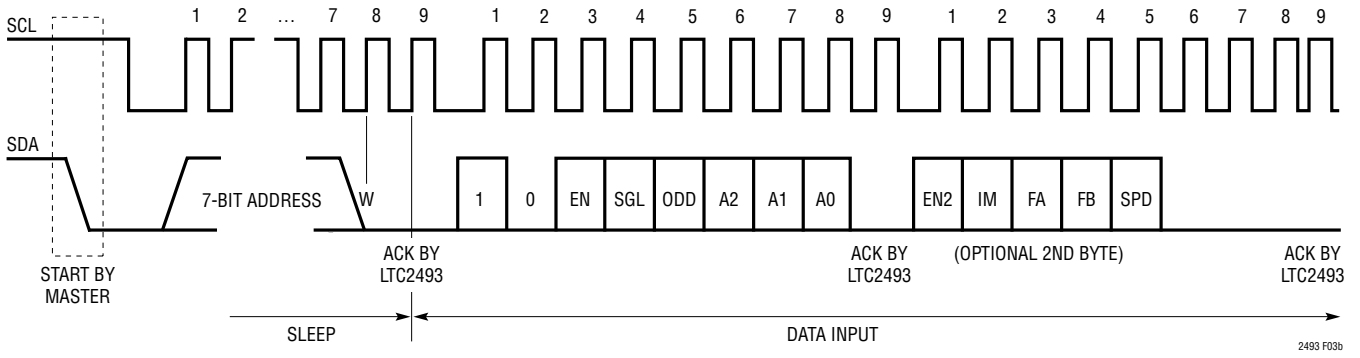

Figure 3b. Timing Diagram for Writing to the LTC2493

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The first input bit (SGL) following the 101 sequence determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of four channels is selected as the positive input. The negative input is COM for all single-ended operations. The remaining four bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

Once the first word is written into the device, a second word may be input in order to select a configuration mode. The first bit of the second word is the enable bit for the conversion configuration (EN2). If this bit is set to 0, then the next conversion is performed using the previously selected converter configuration.

The second set of configuration data can be loaded into the device by setting EN2 = 1 (see Table 4). The first bit (IM) is used to select the internal temperature sensor. If IM = 1, the following conversion will be performed on the internal temperature sensor rather than the selected input channel. The next two bits (FA and FB) are used to set the rejection frequency. The final bit (SPD) is used to select either the 1× output rate if SPD = 0 (auto-calibration is enabled and the offset is continuously calibrated and removed from the final conversion result) or the 2× output rate if SPD = 1 (offset calibration disabled, multiplexing output rates up to 15Hz with no latency). When IM = 1 (temperature measurement) SPD will be ignored and the device will operate in 1× mode.

The configuration remains valid until a new input word with EN = 1 (the first three bits are 101 for the first word) and EN2 = 1 (for the second write byte) is shifted into the device.

Rejection Mode (FA, FB)

The LTC2493 includes a high accuracy on-chip oscillator with no required external components. Coupled with an integrated fourth order digital lowpass filter, the LTC2493 rejects line frequency noise. In the default mode, the LTC2493 simultaneously rejects 50Hz and 60Hz by at least 87dB. If more rejection is required, the LTC2493 can be configured to reject 50Hz or 60Hz to better than 110dB.

Table 4. Converter Configuration

1	0	EN	SGL	ODD	A2	A1	A0	EN2	IM	FA	FB	SPD	CONVERTER CONFIGURATION
1	0	0	X	X	X	X	X	X	X	X	X	X	Keep Previous
1	0	1	X	X	X	X	X	0	X	X	X	X	Keep Previous
0	0	1	X	X	X	X	X	X	X	X	X	X	Keep Previous
1	0	1	X	X	X	X	X	1	0	0	0	0	External Input (See Table 3) 50Hz/60Hz Rejection, 1×
1	0	1	X	X	X	X	X	1	0	0	1	0	External Input (See Table 3) 50Hz Rejection, 1×
1	0	1	X	X	X	X	X	1	0	1	0	0	External Input (See Table 3) 60Hz Rejection, 1×
1	0	1	X	X	X	X	X	1	0	0	0	1	External Input (See Table 3) 50Hz/60Hz Rejection, 2×
1	0	1	X	X	X	X	X	1	0	0	1	1	External Input (See Table 3) 50Hz Rejection, 2×
1	0	1	X	X	X	X	X	1	0	1	0	1	External Input (See Table 3) 60Hz Rejection, 2×
1	0	1	X	X	X	X	X	1	1	0	0	X	Measure Temperature 50Hz/60Hz Rejection, 1×
1	0	1	X	X	X	X	X	1	1	0	1	X	Measure Temperature 50Hz Rejection, 1×
1	0	1	X	X	X	X	X	1	1	1	0	X	Measure Temperature 60Hz Rejection, 1×
1	0	1	X	X	X	X	X	1	X	1	1	X	Reserved, Do Not Use

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Speed Mode (SPD)

Every conversion cycle, two conversions are combined to remove the offset (default mode). This result is free from offset and drift. In applications where the offset is not critical, the auto-calibration feature can be disabled with the benefit of twice the output rate.

While operating in the 2× mode (SPD = 1), the linearity and full-scale errors are unchanged from the 2× mode performance. In both the 2× and 2× mode there is no latency. This enables input steps or multiplexer changes to settle in a single conversion cycle, easing system overhead and increasing the effective conversion rate. During temperature measurements, the 1× mode is always used independent of the value of SPD.

Temperature Sensor

The LTC2493 includes an integrated temperature sensor. The temperature sensor is selected by setting IM = 1. The ADC internally connects to the temperature sensor and performs a conversion.

The digital output is proportional to the absolute temperature of the device. This feature allows the converter to perform cold junction compensation for external thermocouples or continuously remove the temperature effects of external sensors.

The internal temperature sensor output is 28mV at 27°C (300°K), with a slope of 93.5µV/°C independent of V_{REF} (see Figures 4 and 5). Slope calibration is not required if the reference voltage (V_{REF}) is known. A 5V reference has a slope of 314 $LSBs_{24}$/°C. The temperature is calculated from the output code (where $DATAOUT_{24}$ is the decimal representation of the 24-bit result) for a 5V reference using the following formula:

$$T_K = \frac{DATAOUT_{24}}{314} \text{ in Kelvin}$$

If a different value of V_{REF} is used, the temperature output is:

$$T_K = \frac{DATAOUT_{24} \bullet V_{REF}}{1570} \text{ in Kelvin}$$

If the value of V_{REF} is not known, the slope is determined by measuring the temperature sensor at a known temperature T_N (in K) and using the following formula:

$$SLOPE = \frac{DATAOUT_{24}}{T_N}$$

This value of slope can be used to calculate further temperature readings using:

$$T_K = \frac{DATAOUT_{24}}{SLOPE}$$

All Kelvin temperature readings can be converted to T_C (°C) using the fundamental equation:

$$T_C = T_K - 273$$

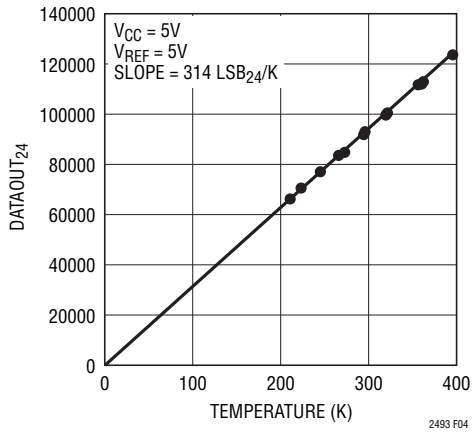

Figure 4. Internal PTAT Digital Output vs Temperature

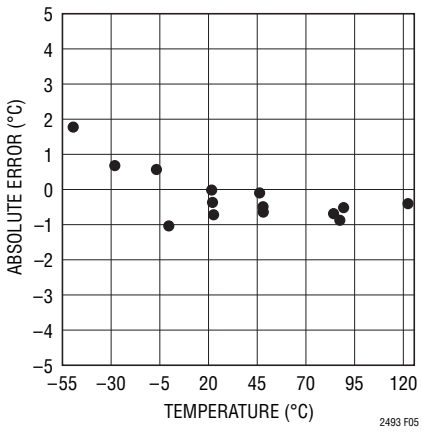

Figure 5. Absolute Temperature Error

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Initiating a New Conversion

When the LTC2493 finishes a conversion, it automatically enters the sleep state. Once in the sleep state, the device is ready for a read operation. After the device acknowledges a read request, the device exits the sleep state and enters the data output state. The data output state concludes and the LTC2493 starts a new conversion once a STOP condition is issued by the master or all 32 bits of data are read out of the device.

During the data read cycle, a STOP command may be issued by the master controller in order to start a new conversion and abort the data transfer. This STOP command must be issued during the ninth clock cycle of a byte read when the bus is free (the ACK/NACK cycle).

LTC2493 Address

The LTC2493 has two address pins (CA0, CA1). Each may be tied HIGH, LOW, or left floating enabling one of nine possible addresses (see Table 5).

In addition to the configurable addresses listed in Table 5, the LTC2493 also contains a global address (1110111) which may be used for synchronizing multiple LTC2493s or other LTC24XX delta-sigma I^2C devices (see Synchronizing Multiple LTC2493s with a Global Address Call section).

Operation Sequence

The LTC2493 acts as a transmitter or receiver, as shown in Figure 6. The device may be programmed to perform several functions. These include input channel selection, measure the internal temperature, selecting the line frequency rejection (50Hz, 60Hz, or simultaneous 50Hz and 60Hz) and a 2× speed mode.

Table 5. Address Assignment

CA1	CA0	ADDRESS
LOW	LOW	0010100
LOW	HIGH	0010110
LOW	Float	0010101
HIGH	LOW	0100110
HIGH	HIGH	0110100
HIGH	Float	0100111
Float	LOW	0010111
Float	HIGH	0100101
Float	Float	0100100

Continuous Read

In applications where the input channel/configuration does not need to change for each cycle, the conversion can be continuously performed and read without a write cycle (see Figure 7). The configuration/input channel remains unchanged from the last value written into the device. If the device has not been written to since power-up, the configuration is set to the default value. At the end of a read operation, a new conversion automatically begins. At the conclusion of the conversion cycle, the next result may be read using the method described above. If the conversion cycle is not concluded and a valid address selects the device, the LTC2493 generates a NACK signal indicating the conversion cycle is in progress.

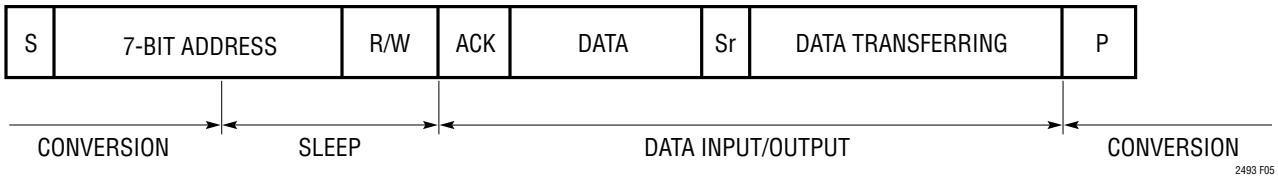

Figure 6. Conversion Sequence

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Continuous Read/Write

Once the conversion cycle is concluded, the LTC2493 can be written to and then read from using the repeated START (Sr) command.

Figure 8 shows a cycle which begins with a data write, a repeated START, followed by a read and concluded with a STOP command. The following conversion begins after all 32 bits are read out of the device or after a STOP command. The following conversion will be performed using the newly programmed data. In cases where the same speed (1×/2× mode) and rejection frequency (50Hz, 60Hz, 50Hz and 60Hz) is used but the channel is changed, a STOP or repeated START may be issued after the first byte (channel selection data) is written into the device.

Discarding a Conversion Result and Initiating a New Conversion with Optional Write

At the conclusion of a conversion cycle, a write cycle can be initiated. Once the write cycle is acknowledged, a STOP command will start a new conversion. If a new input channel or conversion configuration is required, this data can be written into the device and a STOP command will initiate the next conversion (see Figure 9).

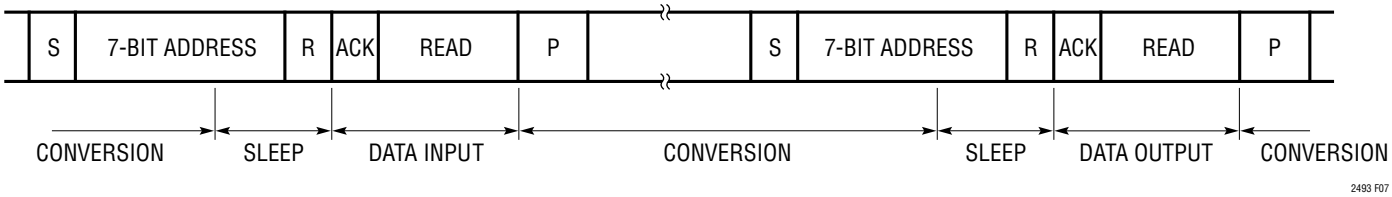

Figure 7. Consecutive Reading with the Same Input/Configuration

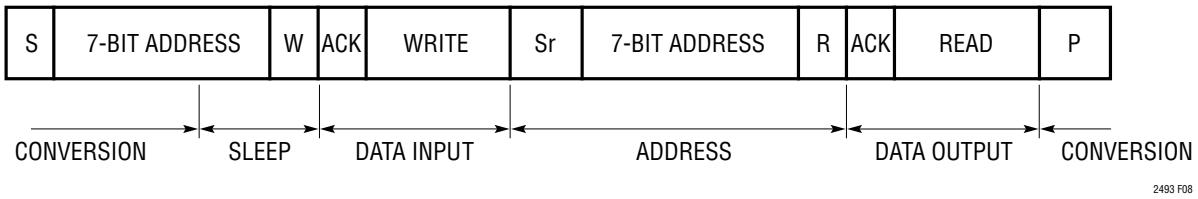

Figure 8. Write, Read, START Conversion

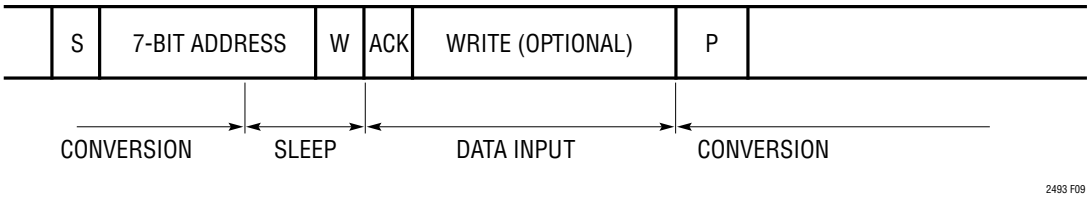

Figure 9. Start a New Conversion Without Reading Old Conversion Result

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Synchronizing Multiple LTC2493s with a Global Address Call

In applications where several LTC2493s (or other I²C delta-sigma ADCs from Linear Technology Corporation) are used on the same I²C bus, all converters can be synchronized through the use of a global address call. Prior to issuing the global address call, all converters must have completed a conversion cycle. The master then issues a START, followed by the global address 1110111, and a write request. All converters will be selected and acknowledge the request. The master then sends a write byte (optional) followed by the STOP command. This will update the channel selection (optional) converter configuration (optional) and simultaneously initiate a start of conversion for all delta-sigma ADCs on the bus (see Figure 10). In order to synchronize multiple converters without changing the channel or configuration, a STOP may be issued after acknowledgement of the global write command. Global read commands are not allowed and the converters will NACK a global read request.

Driving the Input and Reference

The input and reference pins of the LTC2493 are connected directly to a switched capacitor network. Depending on the relationship between the differential input voltage and the differential reference voltage, these capacitors are switched between these four pins. Each time a capacitor is switched between two of these pins, a small amount of charge is transferred. A simplified equivalent circuit is shown in Figure 11.

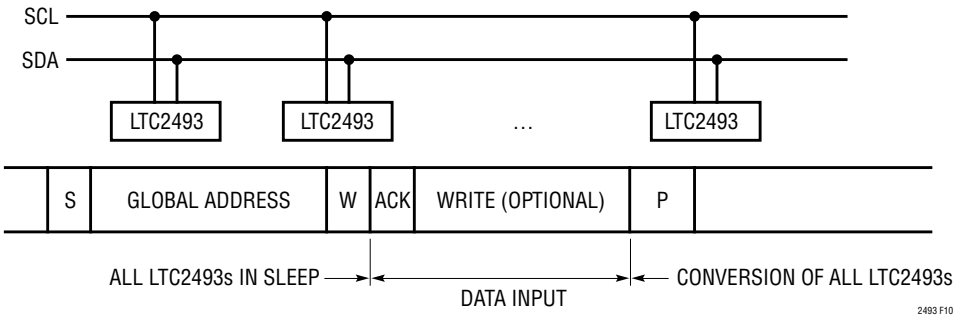
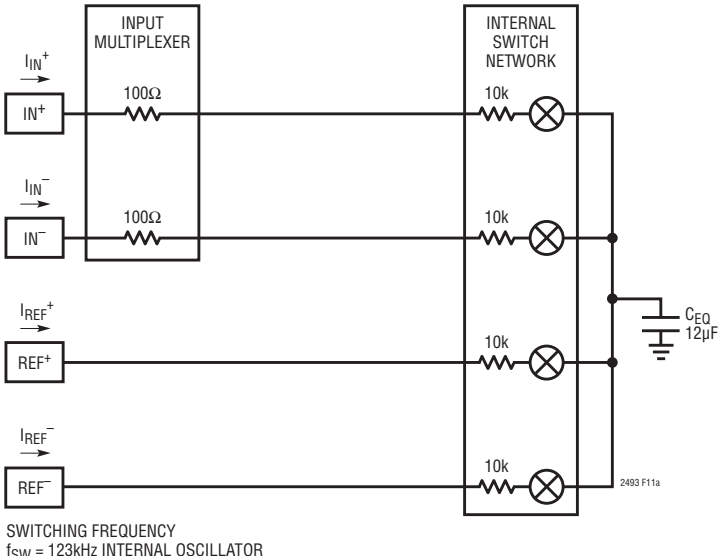


Figure 10. Synchronize Multiple LTC2493s with a Global Address Call



$$I(IN^+)_{AVG} = I(IN^-)_{AVG} = \frac{V_{IN(CM)} - V_{REF(CM)}}{0.5 \bullet R_{EQ}}$$

$$I(REF^+)_{AVG} \approx \frac{1.5V_{REF} + (V_{REF(CM)} - V_{IN(CM)})}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

where:

$V_{REF} = REF^+ - REF^-$

$V_{REF(CM)} = \left(\frac{REF^+ - REF^-}{2}\right)$

$V_{IN} = IN^+ - IN^-$, WHERE IN^+ AND IN^- ARE THE SELECTED INPUT CHANNELS

$V_{IN(CM)} = \left(\frac{IN^+ - IN^-}{2}\right)$

$R_{EQ} = 2.71M\Omega$ INTERNAL OSCILLATOR 60Hz MODE

$R_{EQ} = 2.98M\Omega$ INTERNAL OSCILLATOR 50Hz/60Hz MODE

$R_{EQ} = \left(0.833 \bullet 10^{12}\right) / f_{EOSC}$ EXTERNAL OSCILLATOR

Figure 11. Equivalent Analog Input Circuit

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When using the LTC2493's internal oscillator, the input capacitor array is switched at 123kHz. The effect of the charge transfer depends on the circuitry driving the input/reference pins. If the total external RC time constant is less than 580ns the errors introduced by the sampling process are negligible since complete settling occurs.

Typically, the reference inputs are driven from a low impedance source. In this case, complete settling occurs even with large external bypass capacitors. The inputs (CH0-CH3, COM), on the other hand, are typically driven from larger source resistances. Source resistances up to 10k may interface directly to the LTC2493 and settle completely; however, the addition of external capacitors at the input terminals in order to filter unwanted noise (anti-aliasing) results in incomplete settling.

Automatic Differential Input Current Cancellation

In applications where the sensor output impedance is low (up to 10kΩ with no external bypass capacitor or up to 500Ω with 0.001µF bypass), complete settling of the input occurs. In this case, no errors are introduced and direct digitization is possible.

For many applications, the sensor output impedance combined with external input bypass capacitors produces RC time constants much greater than the 580ns required for 1ppm accuracy. For example, a 10k bridge driving a 0.1µF capacitor has a time constant an order of magnitude greater than the required maximum.

The LTC2493 uses a proprietary switching algorithm that forces the average differential input current to zero independent of external settling errors. This allows direct digitization of high impedance sensors without the need for buffers.

The switching algorithm forces the average input current on the positive input (I_{IN}^+) to be equal to the average input current on the negative input (I_{IN}^-). Over the complete conversion cycle, the average differential input current ($I_{IN}^+ – I_{IN}^-$) is zero. While the differential input current is zero, the common mode input current ($I_{IN}^+ + I_{IN}^-$)/2 is proportional to the difference between the common mode input voltage ($V_{IN(CM)}$) and the common mode reference voltage ($V_{REF(CM)}$).

In applications where the input common mode voltage is equal to the reference common mode voltage, as in the case of a balanced bridge, both the differential and common mode input current are zero. The accuracy of the converter is not compromised by settling errors.

In applications where the input common mode voltage is constant but different from the reference common mode voltage, the differential input current remains zero while the common mode input current is proportional to the difference between $V_{IN(CM)}$ and $V_{REF(CM)}$. For a reference common mode voltage of 2.5V and an input common mode of 1.5V, the common mode input current is approximately 0.74µA (in simultaneous 50Hz/60Hz rejection mode). This common mode input current does not degrade the accuracy if the source impedances tied to IN^+ and IN^- are matched. Mismatches in source impedance lead to a fixed offset error but do not effect the linearity or full-scale reading. A 1% mismatch in a 1k source resistance leads to a 74µV shift in offset voltage.

In applications where the common mode input voltage varies as a function of the input signal level (single-ended type sensors), the common mode input current varies proportionally with input voltage. For the case of balanced input impedances, the common mode input current effects are rejected by the large CMRR of the LTC2493, leading to little degradation in accuracy. Mismatches in source impedances lead to gain errors proportional to the difference between the common mode input and common mode reference. 1% mismatches in 1k source resistances lead to gain errors on the order of 15ppm. Based on the stability of the internal sampling capacitors and the accuracy of the internal oscillator, a one-time calibration will remove this error.

In addition to the input sampling current, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA max), results in a small offset shift. A 1k source resistance will create a 1µV typical and a 10µV maximum offset voltage.

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Reference Current

Similar to the analog inputs, the LTC2493 samples the differential reference pins (REF^+ and REF^-) transferring small amounts of charge to and from these pins, thus producing a dynamic reference current. If incomplete settling occurs (as a function the reference source resistance and reference bypass capacitance) linearity and gain errors are introduced.

For relatively small values of external reference capacitance (C_{REF} < 1nF), the voltage on the sampling capacitor settles for reference impedances of many kΩ (if C_{REF} = 100pF up to 10k will not degrade the performance (see Figures 12 and 13)).

In cases where large bypass capacitors are required on the reference inputs (C_{REF} > .01µF), full-scale and linearity errors are proportional to the value of the reference resistance. Every ohm of reference resistance produces a full-scale error of approximately 0.5ppm (while operating in simultaneous 50Hz/60Hz mode (see Figures 14 and 15)). If the input common mode voltage is equal to

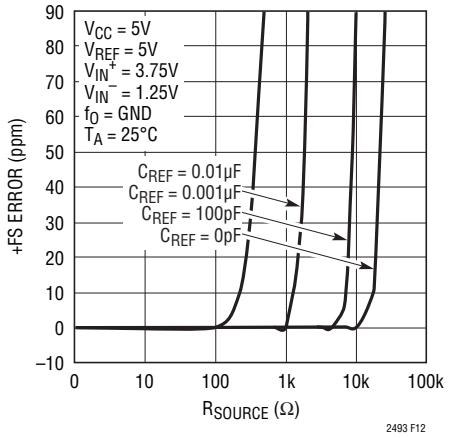

Figure 12. +FS Error vs R_{SOURCE} at V_{REF} (Small C_{REF})

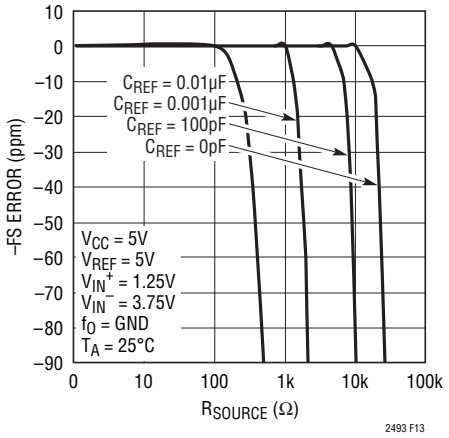

Figure 13. –FS Error vs R_{SOURCE} at V_{REF} (Small C_{REF})

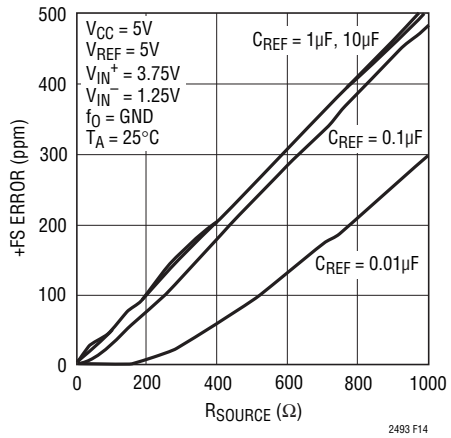

Figure 14. +FS Error vs R_{SOURCE} at V_{REF} (Large C_{REF})

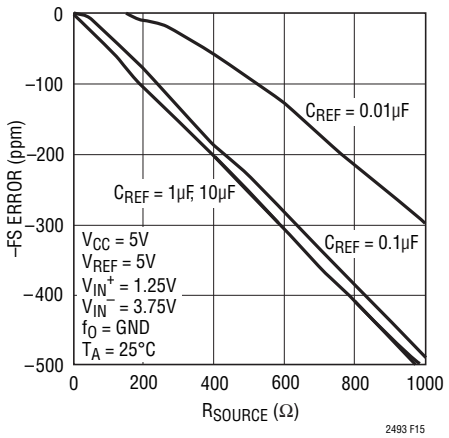

Figure 15. –FS Error vs R_{SOURCE} at V_{REF} (Large C_{REF})

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the reference common mode voltage, a linearity error of approximately 0.67ppm per 100Ω of reference resistance results (see Figure 16). In applications where the input and reference common mode voltages are different, the errors increase. A 1V difference in between common mode input and common mode reference results in a 6.7ppm INL error for every 100Ω of reference resistance.

In addition to the reference sampling charge, the reference ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max) results in a small gain error. A 100Ω reference resistance will create a 0.5µV full-scale error.

Normal Mode Rejection and Anti-Aliasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversample ratio, the LTC2493 significantly simplifies anti-aliasing filter requirements. Additionally, the input current cancellation feature allows external lowpass filtering without degrading the DC performance of the device.

The SINC^4 digital filter provides excellent normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency (f_S) (see Figures 17 and 18). The modulator sampling frequency is f_S = 15,360Hz while operating with its internal oscillator and $f_S = f_{EOSC}/20$ when operating with an external oscillator of frequency f_{EOSC}.

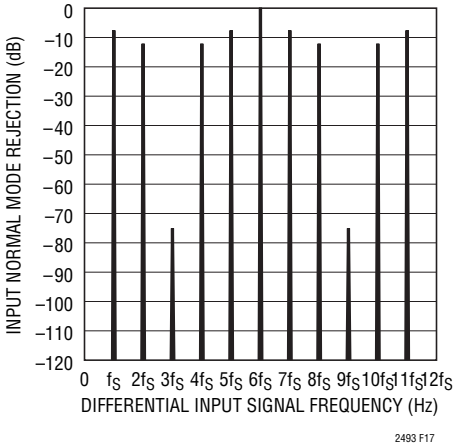

Figure 17. Input Normal Mode Rejection, Internal Oscillator and 50Hz Rejection Mode

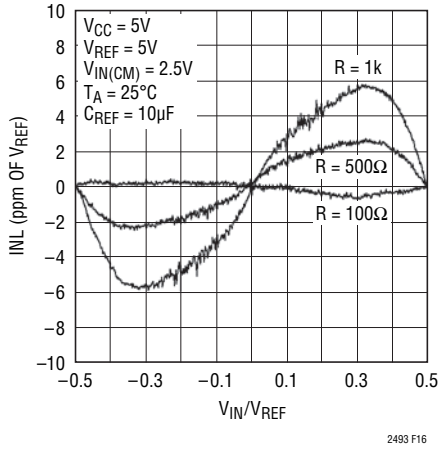

Figure 16. INL vs Differential Input Voltage and Reference Source Resistance for C_{REF} > 1µF

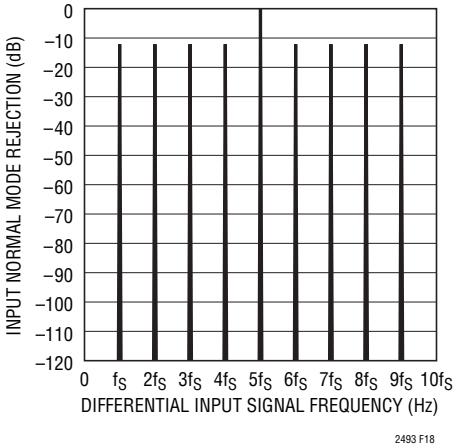

Figure 18. Input Normal Mode Rejection, Internal Oscillator and 60Hz Rejection Mode

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When using the internal oscillator, the LTC2493 is designed to reject line frequencies. As shown in Figure 19, rejection nulls occur at multiples of frequency f_N, where f_N is determined by the input control bits FA and FB (f_N = 50Hz or 60Hz or 55Hz for simultaneous rejection). Multiples of the modulator sampling rate ($f_S = f_N \bullet 256$) only reject noise to 15dB (see Figure 20); if noise sources are present at these frequencies anti-aliasing will reduce their effects.

The user can expect to achieve this level of performance using the internal oscillator, as shown in Figures 21, 22, and 23. Measured values of normal mode rejection are shown superimposed over the theoretical values in all three rejection modes.

Traditional high order delta-sigma modulators suffer from potential instabilities at large input signal levels. The proprietary architecture used for the LTC2493 third order modulator resolves this problem and guarantees stability with input signals 150% of full-scale. In many industrial applications, it is not uncommon to have microvolt level signals superimposed over unwanted error sources with several volts if peak-to-peak noise. Figures 24 and 25 show measurement results for the rejection of a 7.5V peak-to-peak noise source (150% of full-scale) applied to the LTC2493. These curves show that the rejection performance is maintained even in extremely noisy environments.

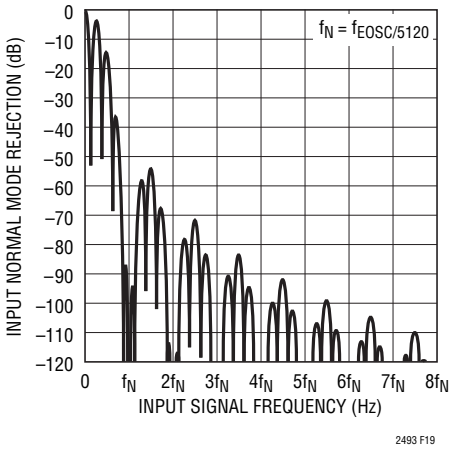


Figure 19. Input Normal Mode Rejection at DC

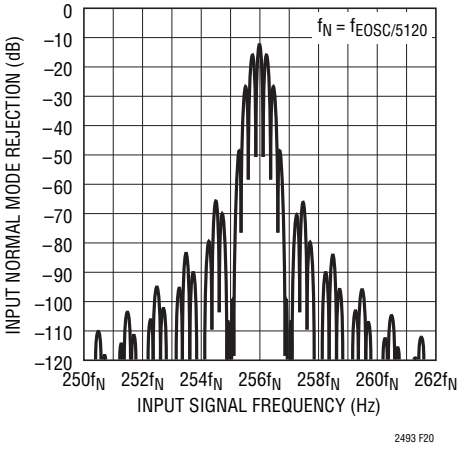


Figure 20. Input Normal Mode Rejection at $f_S = 256 \bullet f_N$

APPLICATIONS INFORMATION

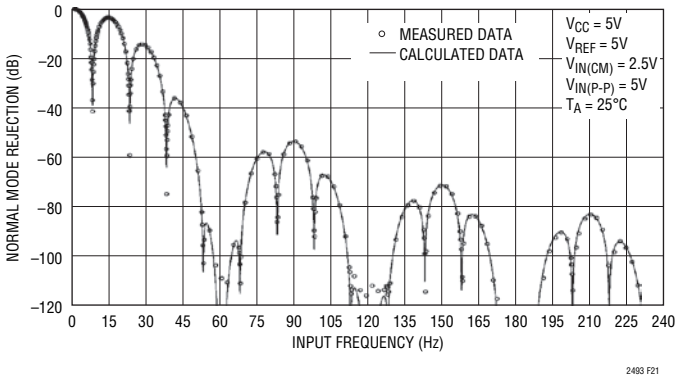


Figure 21. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% (60Hz Notch)

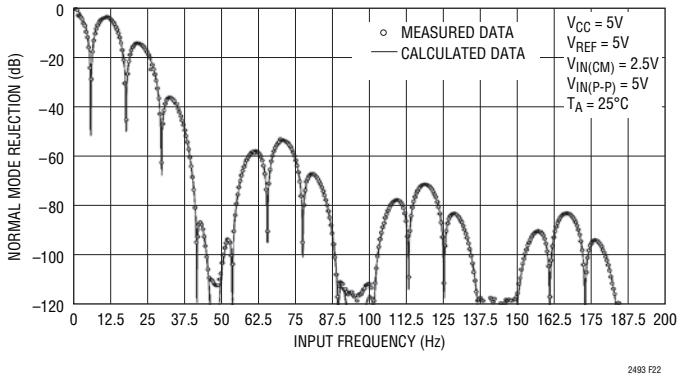


Figure 22. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% (50Hz Notch)

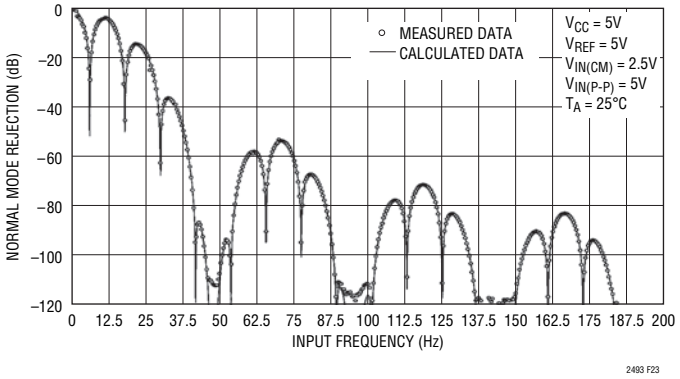


Figure 23. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% (50Hz/60Hz Notch)

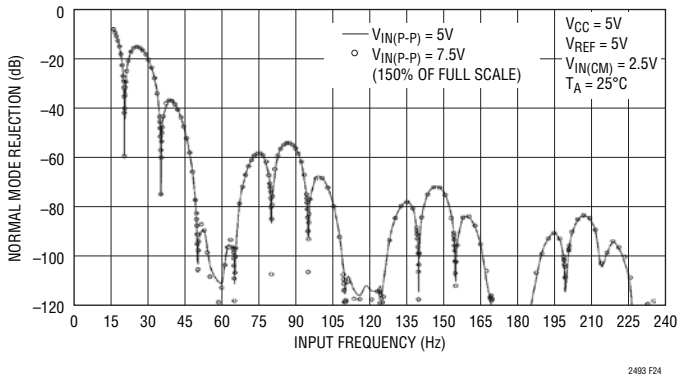


Figure 24. Measure Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% (60Hz Notch)

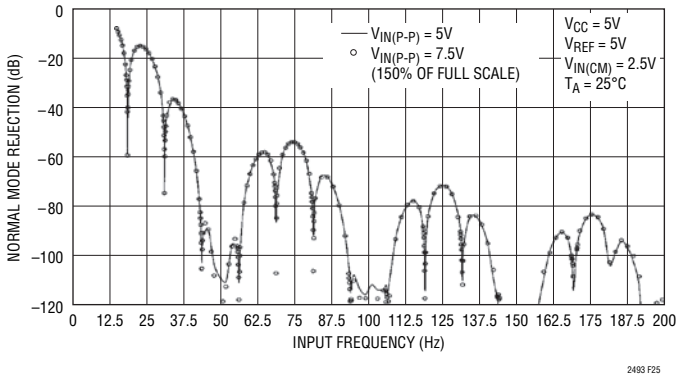


Figure 25. Measure Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% (50Hz Notch)

APPLICATIONS INFORMATION

Using the 2× speed mode of the LTC2493 alters the rejection characteristics around DC and multiples of f_S. The device bypasses the offset calibration in order to increase the output rate. The resulting rejection plots are shown in Figures 26 and 27. 1× type frequency rejection can be achieved using the 2× mode by performing a running average of the previous two conversion results (see Figure 28).

Output Data Rate

When using its internal oscillator, the LTC2493 produces up to 15 samples per second (sps) with a notch frequency of 60Hz. The actual output data rate depends upon the length of the sleep and data output cycles which are controlled by the user and can be made insignificantly short. When operating with an external conversion clock (f_O connected to an external oscillator), the LTC2493 output data rate can be increased. The duration of the conversion cycle is $41036/f_{EOSC}$. If f_{EOSC} = 307.2kHz, the converter behaves as if the internal oscillator is used.

An increase in f_{EOSC} over the nominal 307.2kHz will translate into a proportional increase in the maximum output data rate (up to a maximum of 100sps). The increase in output rate leads to degradation in offset, full-scale error, and effective resolution as well as a shift in frequency rejection. When using the integrated temperature sensor, the internal oscillator should be used or an external oscillator f_{EOSC} = 307.2kHz maximum.

A change in f_{EOSC} results in a proportional change in the internal notch position. This leads to reduced differential mode rejection of line frequencies. The common mode rejection of line frequencies remains unchanged, thus fully differential input signals with a high degree of symmetry on both the IN^+ and IN^- pins will continue to reject line frequency noise.

An increase in f_{EOSC} also increases the effective dynamic input and reference current. External RC networks will continue to have zero differential input current, but the time required for complete settling (580ns for f_{EOSC} = 307.2kHz) is reduced, proportionally.

Once the external oscillator frequency is increased above 1MHz (a more than 3× increase in output rate) the effectiveness of internal auto-calibration circuits begins to degrade. This results in larger offset errors, full-scale errors, and decreased resolution, as seen in Figures 29-36.

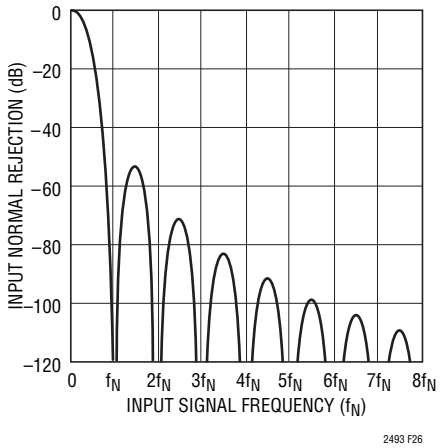


Figure 26. Input Normal Mode Rejection 2× Speed Mode

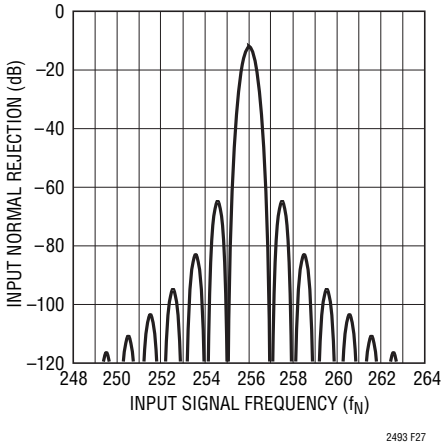


Figure 27. Input Normal Mode Rejection 2× Speed Mode

APPLICATIONS INFORMATION

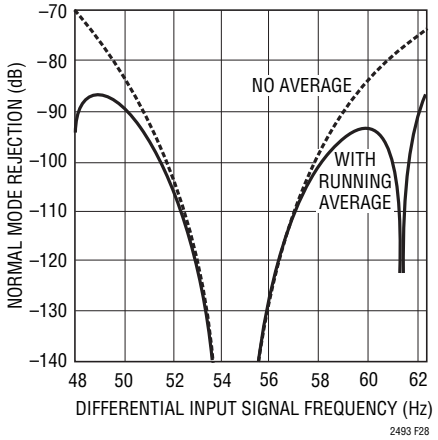


Figure 28. Input Normal Mode Rejection 2× Speed Mode with and Without Running Averaging

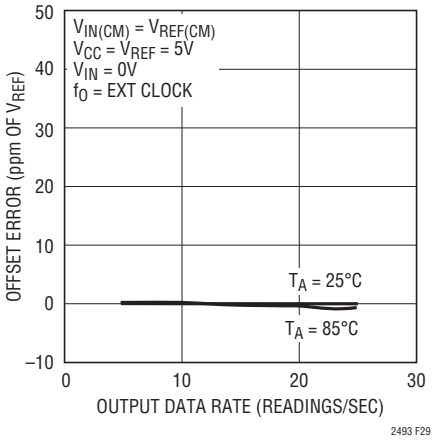


Figure 29. Offset Error vs Output Data Rate and Temperature

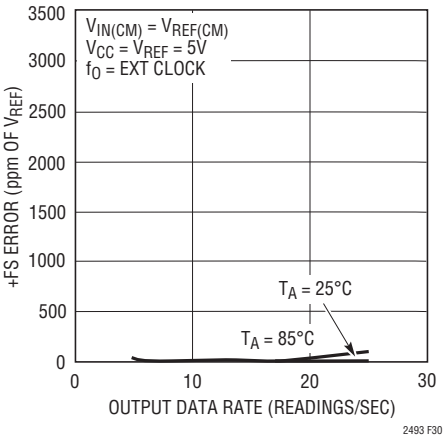


Figure 30. +FS Error vs Output Data Rate and Temperature

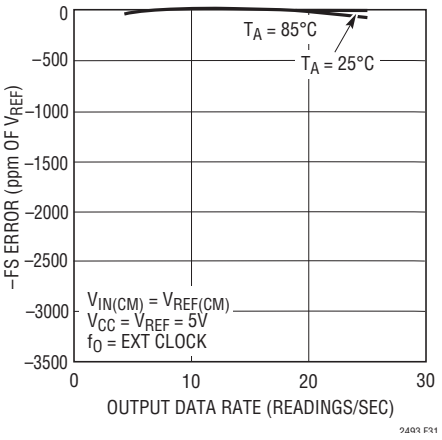


Figure 31.–FS Error vs Output Data Rate and Temperature

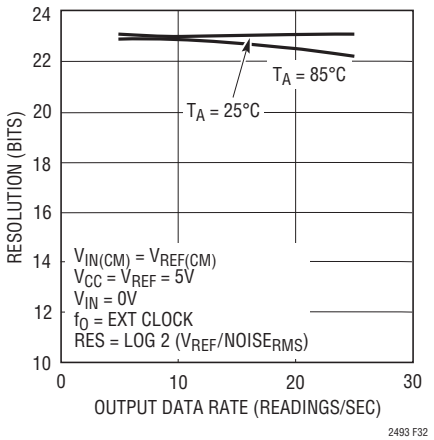


Figure 32. Resolution ($Noise_{RMS}$ ≤ 1 LSB) vs Output Data Rate and Temperature

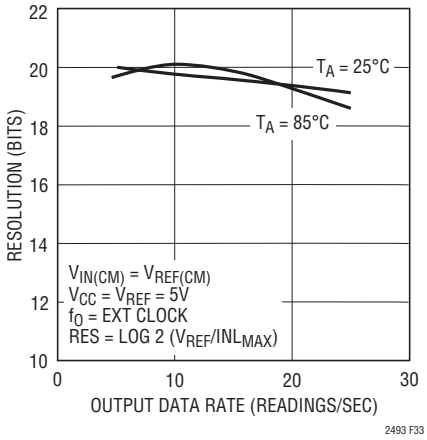


Figure 33. Resolution (INL_{MAX} ≤ 1 LSB) vs Output Data Rate and Temperature

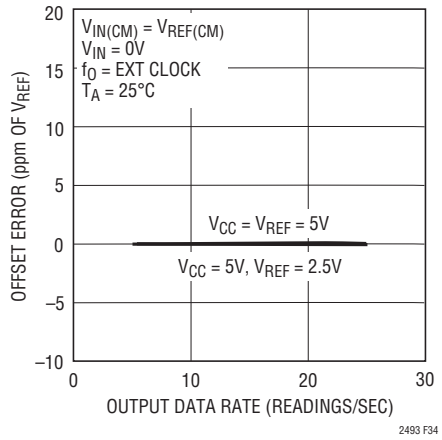


Figure 34. Offset Error vs Output Data Rate and Reference Voltage

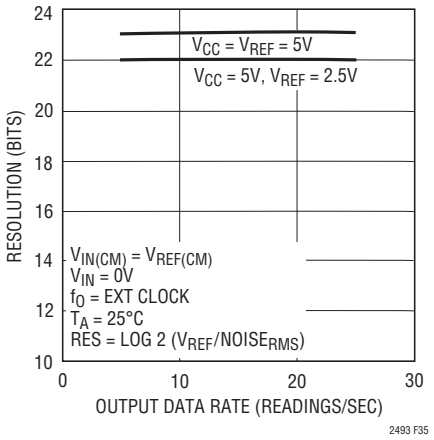


Figure 35. Resolution ($Noise_{RMS}$ ≤ 1 LSB) vs Output Data Rate and Reference Voltage

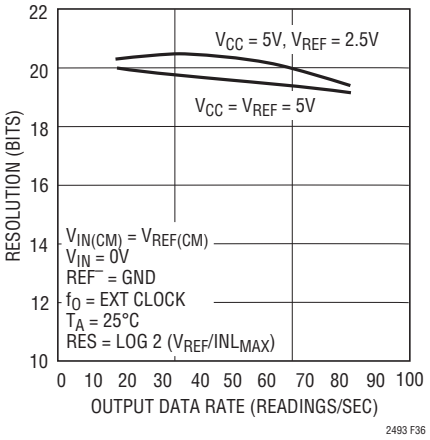


Figure 36. Resolution (INL_{MAX} ≤ 1 LSB) vs Output Data Rate and Reference Voltage

APPLICATIONS INFORMATION

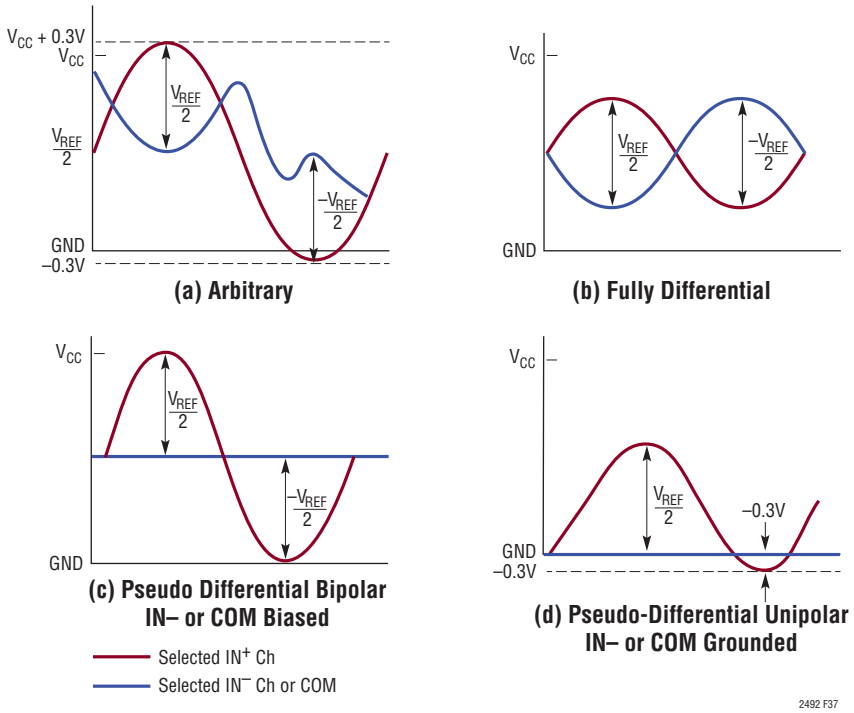


Figure 37. Input Range

Easy Drive ADCs Simplify Measurement of High Impedance Sensors

Delta-sigma ADCs, with their high accuracy and high noise immunity, are ideal for directly measuring many types of sensors. Nevertheless, input sampling currents can overwhelm high source impedances or low bandwidth, micropower signal conditioning circuits. The LTC2493 solves this problem by balancing the input currents, thus simplifying or eliminating the need for signal conditioning circuits.

A common application for a delta-sigma ADC is thermistor measurement. Figure 38 shows two examples of thermistor digitization benefiting from the Easy Drive technology.

The first circuit (applied to input channels CH0 and CH1) uses balanced reference resistors in order to balance the common mode input/reference voltage and balance the differential input source resistance. If reference resistors R1 and R4 are exactly equal, the input current is zero and no errors result. If these resistors have a 1% tolerance, the maximum error in measured resistance is 1.6Ω due to a shift in common mode voltage; far less than the 1% error of the reference resistors themselves. No amplifier is required, making this an ideal solution in micropower applications.

Easy Drive also enables very low power, low bandwidth amplifiers to drive the input to the LTC2493. As shown in Figure 38, CH2 is driven by the LT1494. The LT1494 has excellent DC specs for an amplifier with 1.5µA supply current (the maximum offset voltage is 150µV and the open-loop gain is 100,000). Its 2kHz bandwidth makes it unsuitable for driving conventional delta-sigma ADCs. Adding a 1k, 0.1µF filter solves this problem by providing a charge reservoir that supplies the LTC2493 instantaneous current, while the 1k resistor isolates the capacitive load from the LT1494.

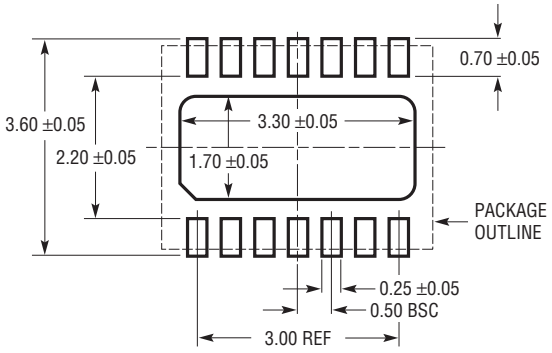
Conventional delta-sigma ADCs input sampling current lead to DC errors as a result of incomplete settling in the external RC network.

The Easy Drive technology cancels the differential input current. By balancing the negative input (CH3) with a 1k, 0.1µF network errors due to the common mode input current are cancelled.

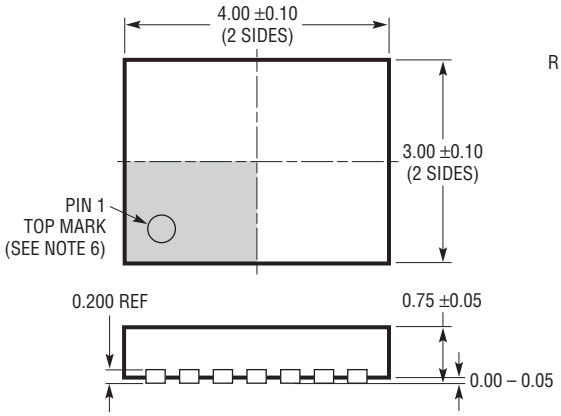
PACKAGE DESCRIPTION

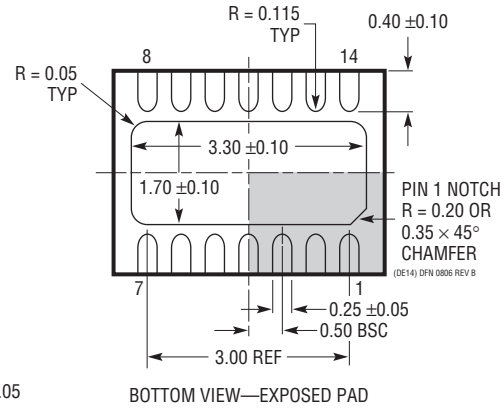
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/09	Update Tables 1 and 2	16
D	07/10	Revised Typical Application drawing	1
		Added f_O pin to parameters of V_{IHA} in I^2C Inputs and Digital Outputs section	4
		Added information to I^2C Interface section	14
E	11/14	Clarified performance vs f_O frequency, reduced external oscillator maximum frequency to 1MHz.	5, 8, 28
		Clarified Input Voltage Range.	4, 13, 29
		Added underrange note to Table 1.	15

TYPICAL APPLICATION

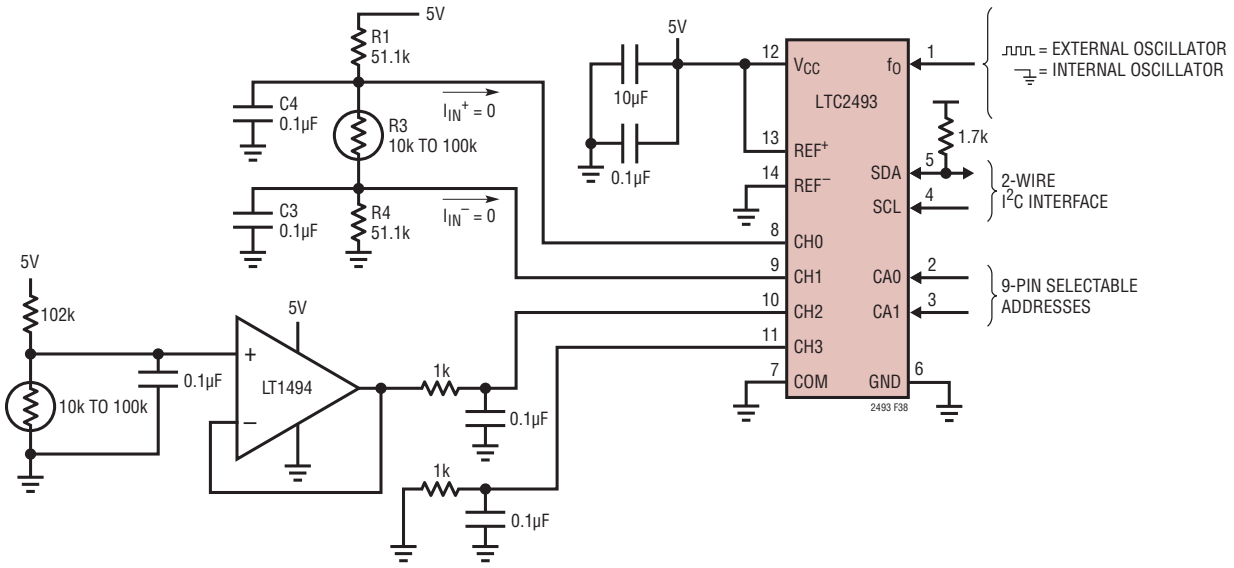


Figure 38. Easy Drive ADCs Simplify Measurement of High Impedance Sensors

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max Initial Accuracy, 5ppm/°C Drift
LT1460	Micropower Series Reference	0.075% Max Initial Accuracy, 10ppm/°C Max Drift
LT1790	Micropower SOT-23 Low Dropout Reference Family	0.05% Max Initial Accuracy, 10ppm/°C Max Drift
LTC2400	24-Bit, No Latency ΔΣ ADC in SO-8	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2410	24-Bit, No Latency ΔΣ ADC with Differential Inputs	0.8μV_{RMS} Noise, 2ppm INL
LTC2440	24-Bit, High Speed, Low Noise ΔΣ ADC	3.5kHz Output Rate, 200nV_{RMS} Noise, 24.6 ENOBs
LTC2442	24-Bit, High Speed, 2-/4-Channel ΔΣ ADC with Integrated Amplifier	8kHz Output Rate, 200nV_{RMS} Noise, Simultaneous 50Hz/60Hz Rejection
LTC2449	24-Bit, High Speed, 8-/16-Channel ΔΣ ADC	8kHz Output Rate, 200nV_{RMS} Noise, Simultaneous 50Hz/60Hz Rejection
LTC2480/LTC2482/ LTC2484	16-Bit/24-Bit ΔΣ ADCs with Easy Drive Inputs, 600nV_{RMS} Noise, Programmable Gain, and Temperature Sensor	Pin Compatible 16-Bit and 24-Bit Versions
LTC2481/LTC2483/ LTC2485	16-Bit/24-Bit ΔΣ ADCs with Easy Drive Inputs, 600nV_{RMS} Noise, I^2C Interface, Programmable Gain, and Temperature Sensor	Pin Compatible 16-Bit and 24-Bit Versions
LTC2486/LTC2488/ LTC2492	16-Bit/24-Bit 2-/4-Channel ΔΣ ADC with Easy Drive Inputs, SPI Interface, Programmable Gain, and Temperature Sensor	Pin-Compatible 16-Bit and 24-Bit Versions
LTC2487	16-Bit 2-/4-Channel ΔΣ ADC with Easy Drive Inputs and I^2C Interface, Temperature Sensor	Pin-Compatible with LTC2493/LTC2489
LTC2489	16-Bit 2-/4-Channel ΔΣ ADC with Easy Drive Inputs	Pin-Compatible with LTC2487/LTC2493
LTC2495/LTC2497/ LTC2499	16-Bit/24-Bit 8-/16-Channel ΔΣ ADC with Easy Drive Inputs and I^2C Interface, Programmable Gain, and Temperature Sensor	Pin-Compatible 16-Bit and 24-Bit Versions
LTC2496/LTC2498	16-Bit/24-Bit 8-/16-Channel ΔΣ ADC with Easy Drive Inputs and SPI Interface	Pin-Compatible with LTC2498/LTC2449

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