

Description

The SXJ6N80D protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, low operating voltage. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.

General Features

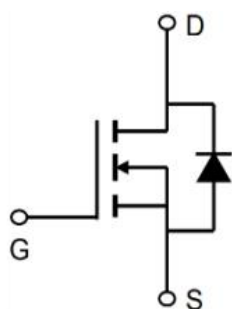
$V_{DS} = 800V$ (Type: 890V) $IDM = 12A$

$R_{DS(ON)} < 900m\Omega$ @ $V_{GS} = 10V$

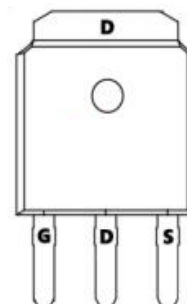
Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



TO-252-3L



Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	800	V
I_D	Continuous Drain Current	6	A
IDM	Pulsed Drain Current (note1)	12	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	225	mJ
P_D	Power Dissipation ($T_c = 25^\circ C$)	25.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	2	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ C/W$

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source breakdown voltage	VGS=0V, ID=250μA	800	-	-	V
V(GS)th	Gate threshold voltage	VDS=VGS, ID=250μA	2.5	3.5	4.5	V
IDSS	Zero gate voltage drain current	VDS=800V, VGS=0V, T _J =25°C	-	-	1	μA
IDSS	Zero gate voltage drain current	VDS=800V, VGS=0V, T _J =150°C			10	μA
IGSS	Gate-source leakage current	VGS=±30V, VDS=0V	-	-	±100	nA
RDS(on)	Drain-source on-state resistance	VGS=10V, ID=2.5A, T _J =25°C	-	800	900	mΩ
RDS(on)	Drain-source on-state resistance	VGS=10V, ID=2.5A, T _J =150°C		2000	5000	mΩ
Ciss	Input capacitance	VGS=0V, VDS=50V, f=1MHz	-	541	-	pF
Coss	Output capacitance		-	31.6	-	pF
Crss	Reverse transfer capacitance		-	1.33	-	pF
td(on)	Turn-on delay time	VDD=400V, VGS=13V, ID=2.2A,	-	17.6	-	ns
tr	Rise time		-	22.4	-	ns
td(off)	Turn-off delay time		-	64.2	-	ns
tf	Fall time		-	28.2	-	ns
Qgs	Gate to source charge	VDD=400V, ID=4A, VGS=0 to 10V	-	2.7	-	nC
Qgd	Gate to drain charge		-	4.97	-	nC
Qg	Gate charge total		-	10.7	-	nC
Vplateau	Gate plateau voltage		-	5.42	-	V
VSD	Diode forward voltage	VGS=0V, IF=5A, T _f =25°C	-	0.86	-	V
trr	Reverse recovery time	VR=400V, IF=1.1A, diF/dt=100A/μs	-	181	-	ns
Qrr	Reverse recovery charge		-	0.74	-	μC
Irrm	Peak reverse recovery current		-	8.68	-	A

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The EAS data shows Max. rating . L=0.5mH, IAS =5.0A, VDD =50V, RG=25Ω
- 3、The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD≤ BVDSS, Starting at T_J =25°C
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

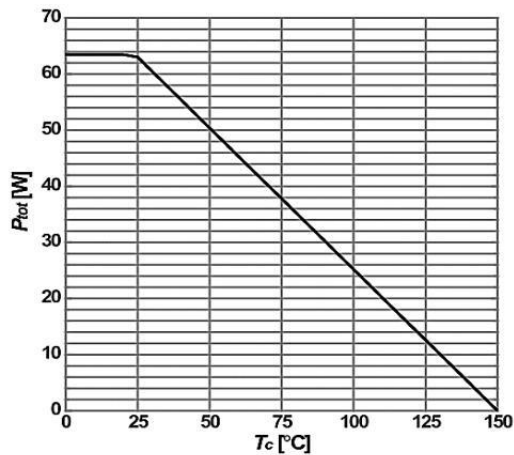


Figure1: Power dissipation (Non FullPAK)

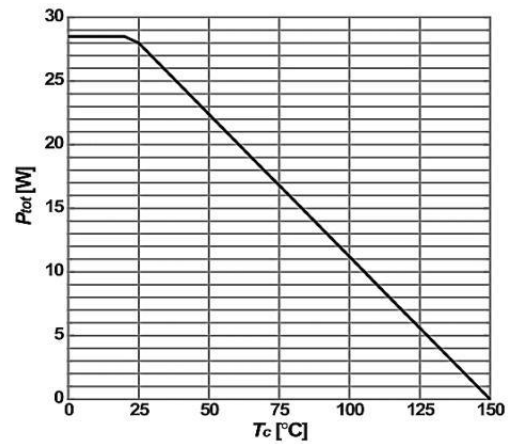


Figure2: Power dissipation (FullPAK)

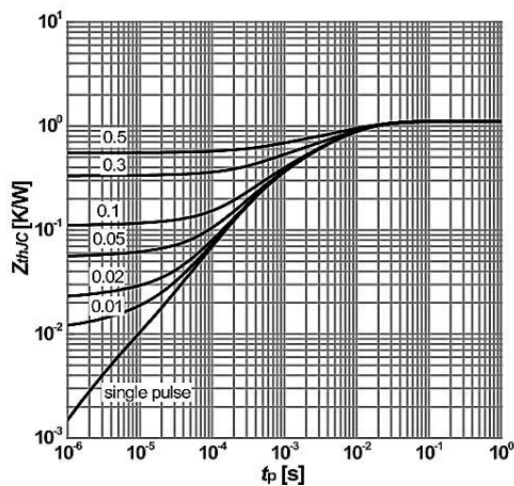


Figure3: Max. transient thermal impedance
zn. c=f(t_p);parameter:D=tT

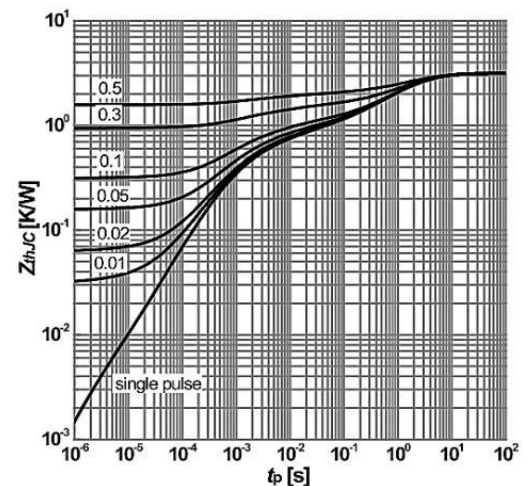


Figure4: Max. transient thermal impedance
zn. c=f(t_p);parameter:D=t pT

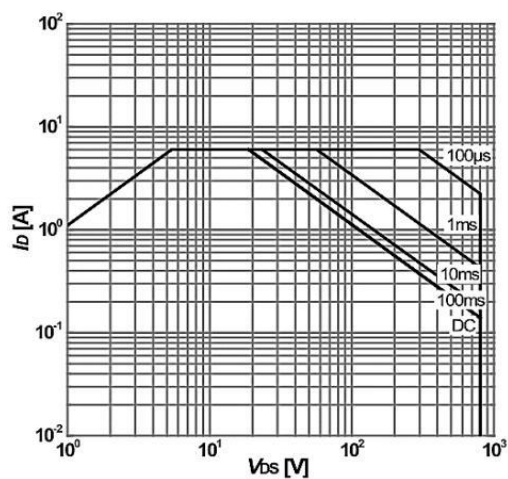


Figure5: Safe operating area (Non FullPAK)
o=f(v_{os});T=25°C;D=0;parameter:tb

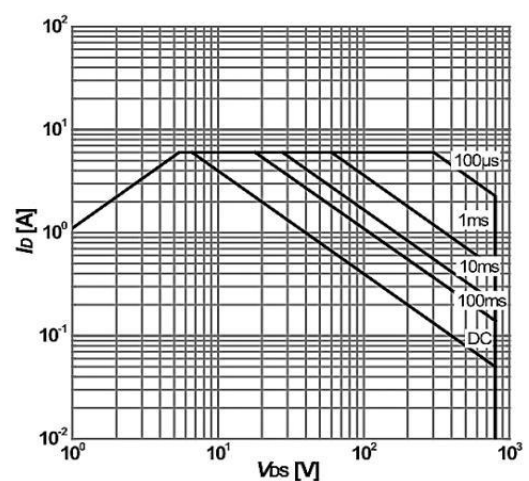


Figure6: Safe operating area (FullPAK)
o=f(v_{os});T=25°C;D=0;parameter:tb

Typical Characteristics

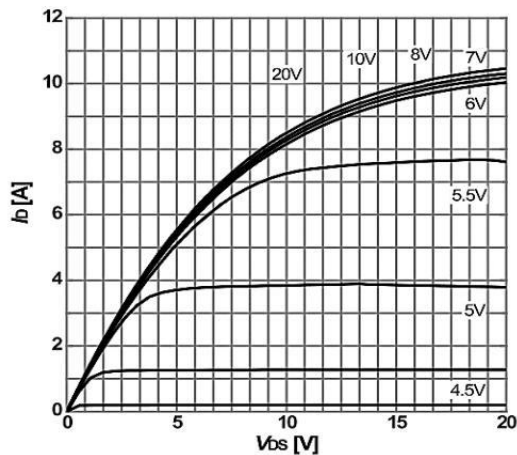


Figure 7: Typ. output characteristics
 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

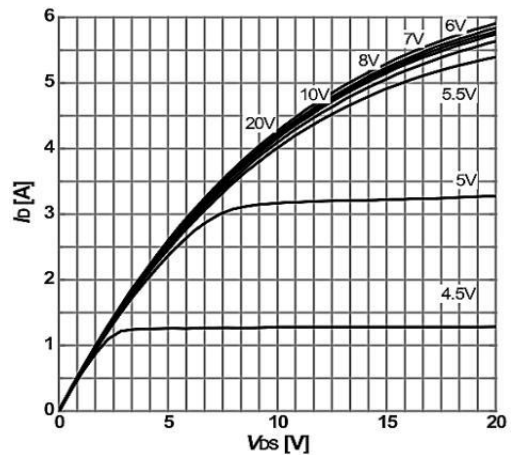


Figure 8: Typ. output characteristics
 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

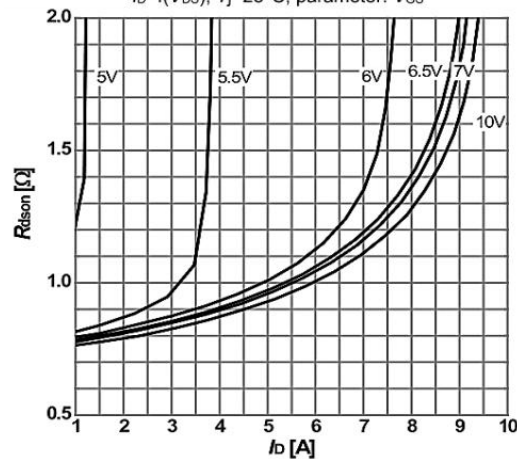


Figure 9: Typ. drain-source on-state resistance
 $R_{DS(on)} = f(I_D); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

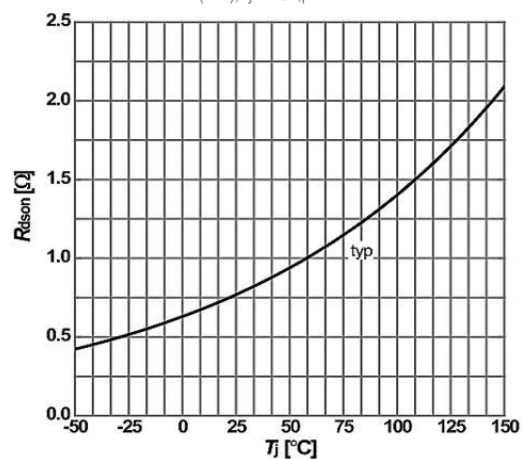


Figure 10: drain-source on-state resistance
 $R_{DS(on)} = f(T_J); I_D = 3.2\text{A}; V_{GS} = 10\text{V}$

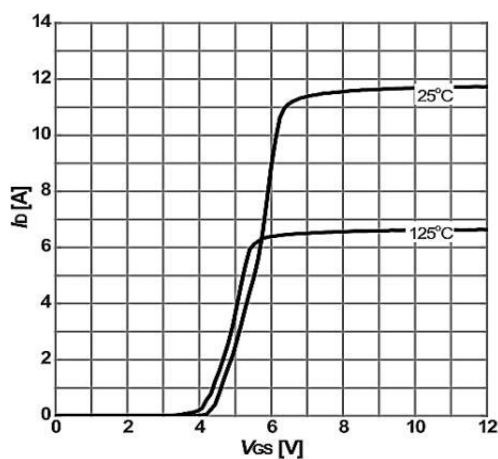


Figure 11: Type. transfer characteristics
 $I_D = f(V_{GS}); V_{DS} = 20\text{V}; \text{parameter: } T$

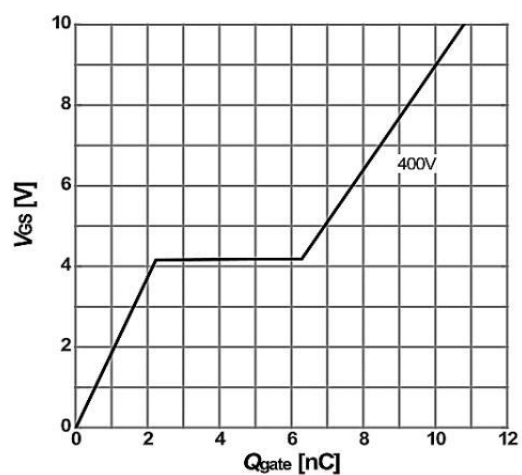
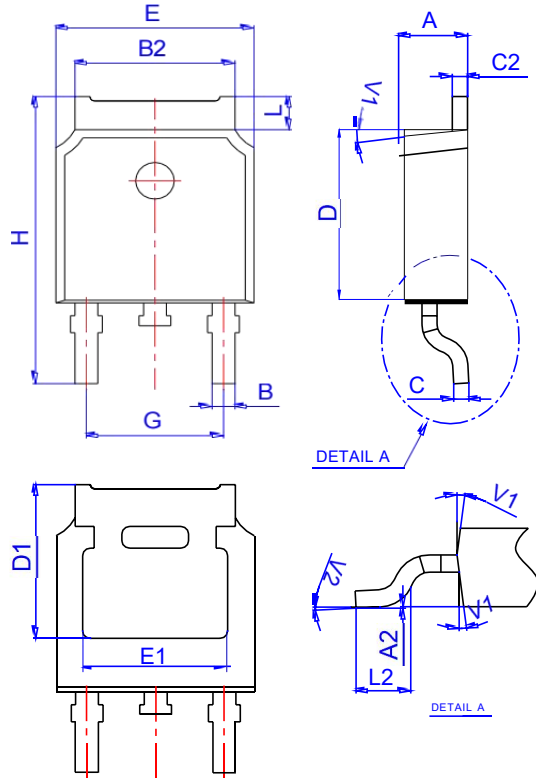


Figure 12: Type. gate charge
 $V_{DS} = f(Q_{gate}); I_D = 3.2\text{A pulsed}; V_{GS} = 480\text{V}$

Package Mechanical Data:TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-252-3L		2500