

74LVC1G04 Single Inverter Gate

1. General Description

1.1 Description

This single inverter gate is designed for 1.65-V to 5.5-V V_{CC} operation. The 74LVC1G04 device performs the Boolean function $Y = \overline{A}$.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

1.2 Features

- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Provides down translation to V_{CC}

- Low power consumption, 10 μ A max I_{CC}
- ± 24 mA output drive at 3.3V
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection

1.3 Device Information

PART NUMBER	PACKAGE
74LVC1G04	SOT23
	SC70
	SOT5X3
	DFN
	DSBGA

2. Connection Diagrams and Pin Description

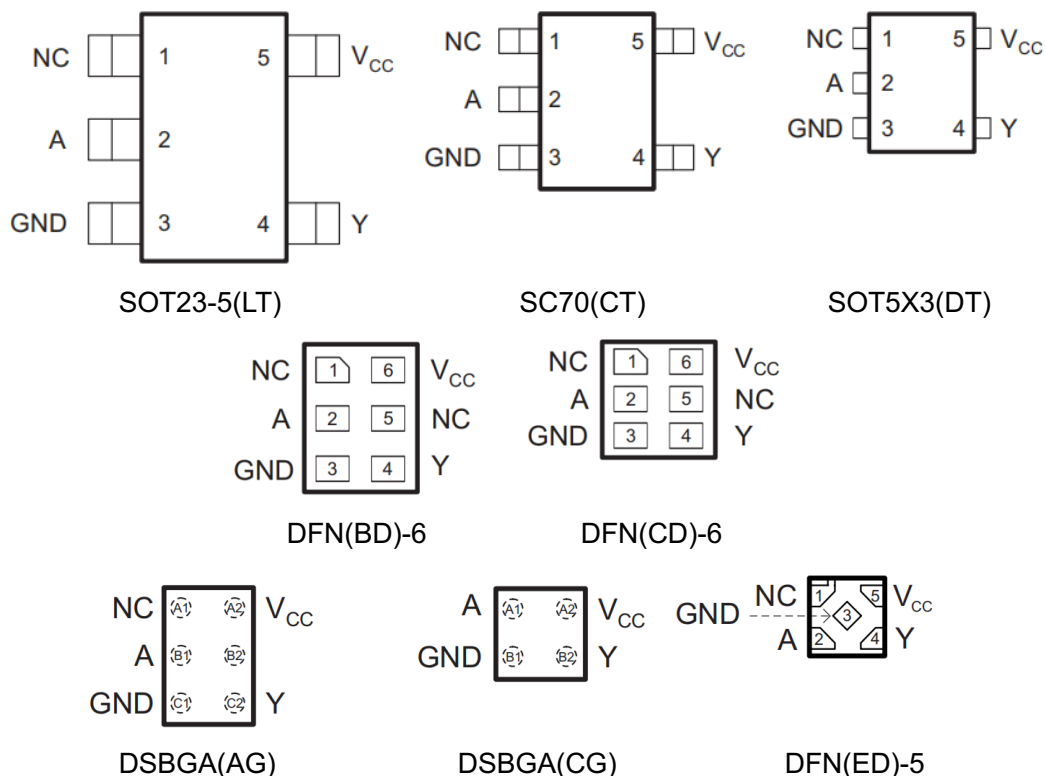


Figure 2.1: Top View

PIN No.					NAME	I/O	FUNCTION
LT/CT/DT	BD/CD	AG	CG	ED			
1	1,5	A1,B2	--	1	NC		No Connected
2	2	B1	A1	2	A	I	Input
3	3	C1	B1	3	GND		Ground
4	4	C2	B2	4	Y	O	Output
5	6	A2	A2	5	VCC		Supply Voltage

3. System Diagram

3.1 Logic Diagram



Figure 3.1: 74LVC1G04 Logic Diagram

3.2 Function Table

Input	Output
A	Y
1	0
0	1

1≡High State, 0≡Low State

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V_{CC}	Supply Voltage	-0.5	6.5	V
V_I	Input Voltage Range	-0.5	6.5	V
V_O	Voltage Range(applied to any output in the high-impedance or power-off state) ⁽¹⁾	-0.5	6.5	V
	Voltage Range(applied to any output in the high or low state)	-0.5	$V_{CC} + 0.5$	V
I_O	Continuous Output Current		± 50	mA
T_J	Junction Temperature		125	°C
T_{OP}	Operating Temperature	0	70	°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged, These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under normal operating conditions.

- (1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Electrical Characteristics

4.2.1 DC Specifications

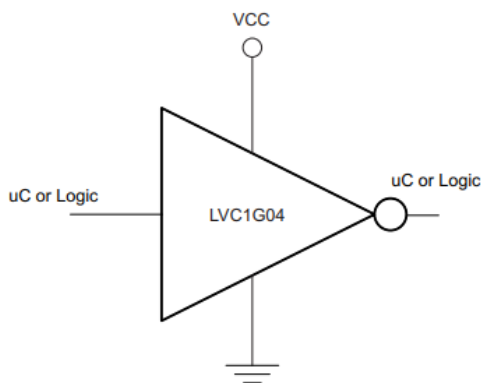
($T_a=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), All typical values are at $V_{CC}=3.3\text{V}$, unless otherwise specified)

Symbol	Parameter	Test Condition	MIN	TYP	MAX	Unit
V_{IH}	High Level Input Voltage	$V_{CC}=1.65\text{V to }1.95\text{V}$	$0.65V_{CC}$	--	--	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$	1.7	--	--	V
		$V_{CC}=3\text{V to }5.5\text{V}$	$0.7V_{CC}$	--	--	V
V_{IL}	Low Level Input Voltage	$V_{CC}=1.65\text{V to }1.95\text{V}$	--	--	$0.35V_{CC}$	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$	--	--	0.7	V
		$V_{CC}=3\text{V to }3.6\text{V}$	--	--	0.8	V
		$V_{CC}=4.5\text{V to }5.5\text{V}$	--	--	$0.3V_{CC}$	V
I_{OH}	High Level Output Current	$V_{CC}=1.65\text{V}$	--	--	-4	mA
		$V_{CC}=2.3\text{V}$	--	--	-8	mA
		$V_{CC}=3\text{V}$	--	--	-16	mA
			--	--	-24	mA
		$V_{CC}=4.5\text{V}$	--	--	-32	mA
I_{OL}	Low Level Output Current	$V_{CC}=1.65\text{V}$	--	--	4	mA
		$V_{CC}=2.3\text{V}$	--	--	8	mA
		$V_{CC}=3\text{V}$	--	--	16	mA
			--	--	24	mA
		$V_{CC}=4.5\text{V}$	--	--	32	mA

Symbol	Parameter	Test Condition	MIN	TYP	MAX	Unit
V_{OH}	High Level Output Voltage	$V_{CC}=1.65V$ to $5.5V, I_{OH}=-100\mu A$	$V_{CC}-0.1$	--	--	V
		$V_{CC}=1.65V, I_O=-4mA$	--	1.47	--	V
		$V_{CC}=2.3V, I_O=-8mA$	--	2.15	--	V
		$V_{CC}=3V, I_O=-16mA$	--	2.8	--	V
		$V_{CC}=3V, I_O=-24mA$	--	2.7	--	V
		$V_{CC}=4.5V, I_O=-32mA$	--	4.2	--	V
V_{OL}	Low Level Output Voltage	$V_{CC}=1.65V$ to $5.5V, I_{OH}=100\mu A$	--	--	0.1	V
		$V_{CC}=1.65V, I_O=4mA$	--	0.09	--	V
		$V_{CC}=2.3V, I_O=8mA$	--	0.1	--	V
		$V_{CC}=3V, I_O=16mA$	--	0.15	--	V
		$V_{CC}=3V, I_O=24mA$	--	0.25	--	V
		$V_{CC}=4.5V, I_O=32mA$	--	0.25	--	V
I_I	A Input Leakage Current	$V_{CC}=0$ to $5.5V, V_I=V_{CC}$ or GND	--	0	± 1	μA
I_{off}	Power Off Leakage Current	$V_{CC}=0V, V_I$ or $V_O=5.5V$	--	0	± 10	μA
I_{CC}	Quiescent Supply Current	$V_{CC}=1.65V$ to $5.5V, V_I=V_{CC}$ or GND, $I_O=0$	--	0	10	μA
ΔI_{CC}	Additional Quiescent Supply Current Per Input Pin	$V_{CC}=3V$ to $5.5V$, one input at $V_{CC}-0.6V$, other inputs at V_{CC} or GND	--	--	500	μA

5. Application Information

Inverter Logic Function



Basic LED Driver

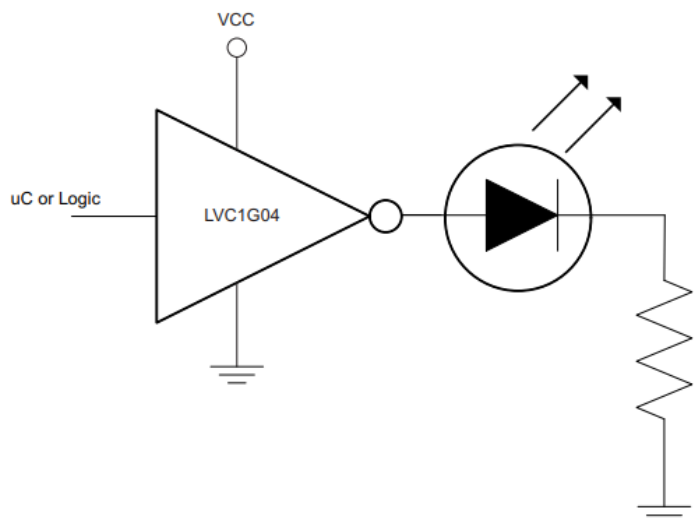


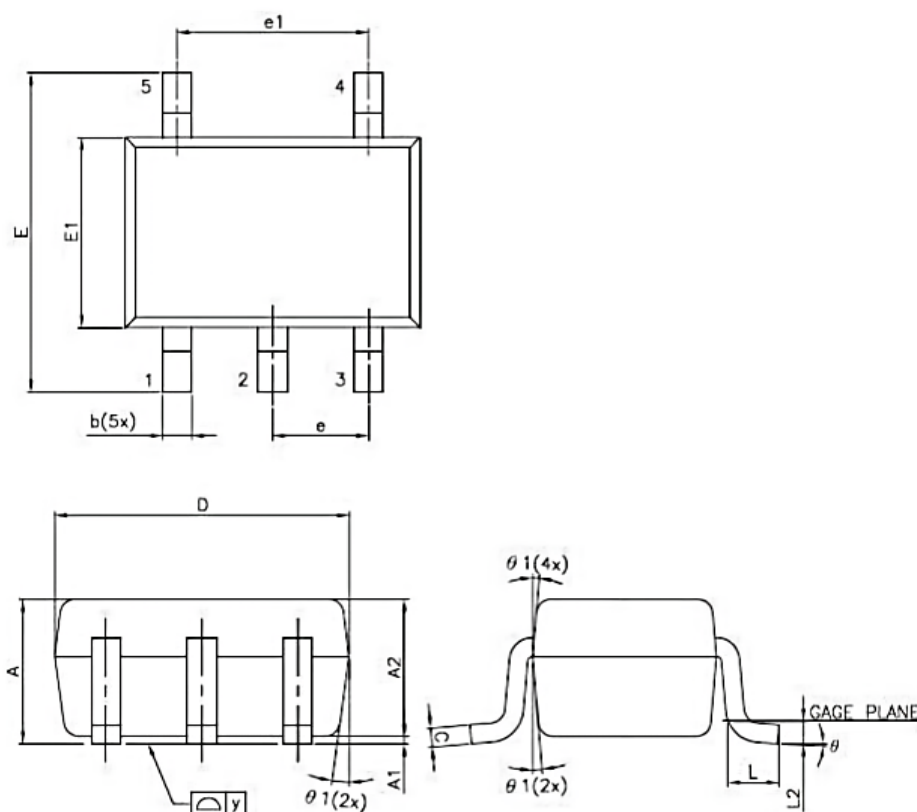
Figure 5.1: Application Schematic



6. Ordering Information

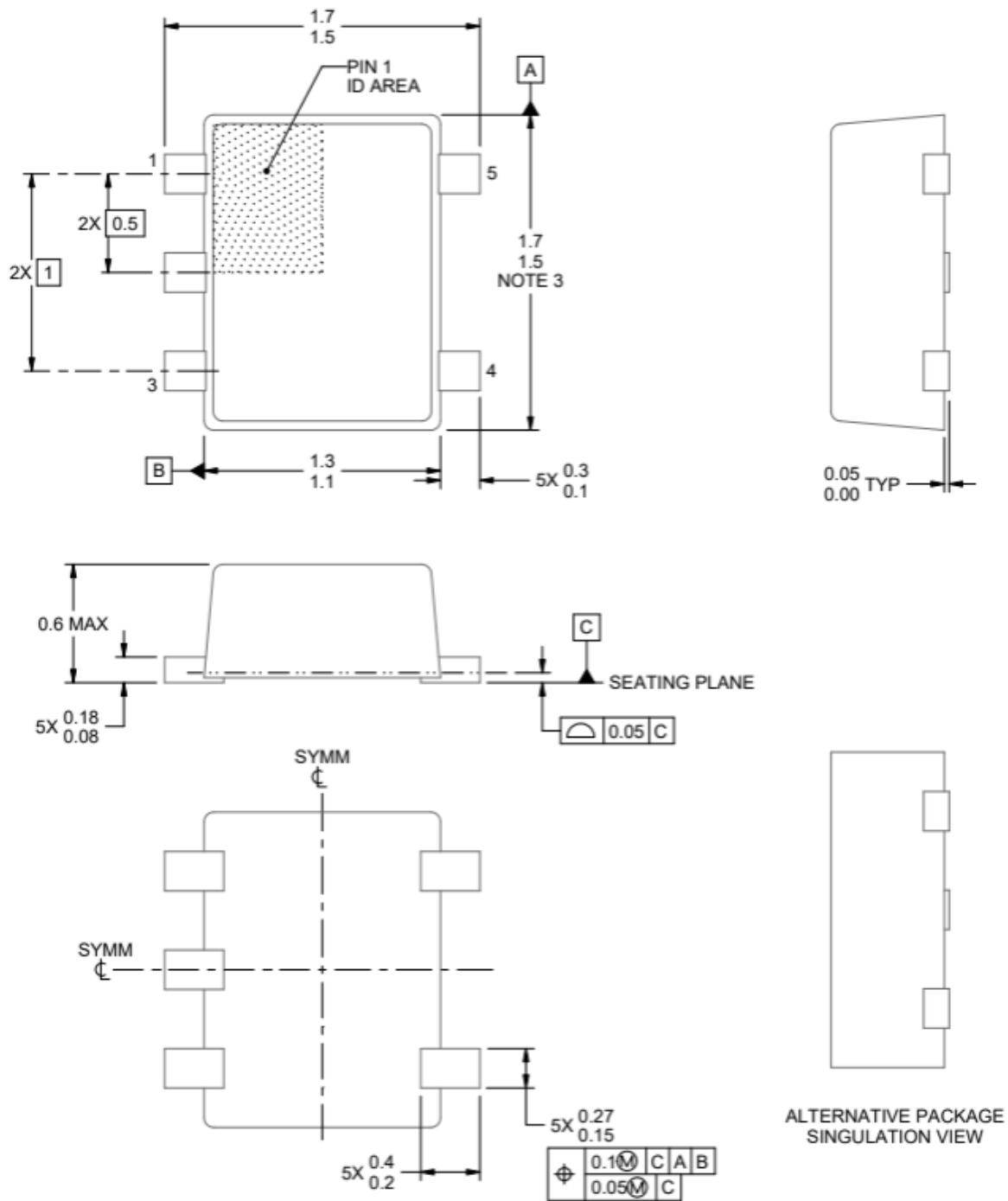
Orderable Device	Package Type	Pins	Packing	Package Qty
74LVC1G04LT05ARCQ	SOT23	5	Tape & Reel	3000
74LVC1G04CT05ARCQ	SC70	5	Tape & Reel	3000
74LVC1G04DT05ARDQ	SOT5x3	5	Tape & Reel	4000
74LVC1G04BD06AREQ	DFN(BD)	6	Tape & Reel	5000
74LVC1G04CD06AREQ	DFN(CD)	6	Tape & Reel	5000
74LVC1G04ED05ARCQ	DFN	5	Tape & Reel	3000
74LVC1G04AG05ARCQ	DSBGA	5	Tape & Reel	3000
74LVC1G04CG04ARCQ	DSBGA	4	Tape & Reel	3000

7.2 SC70

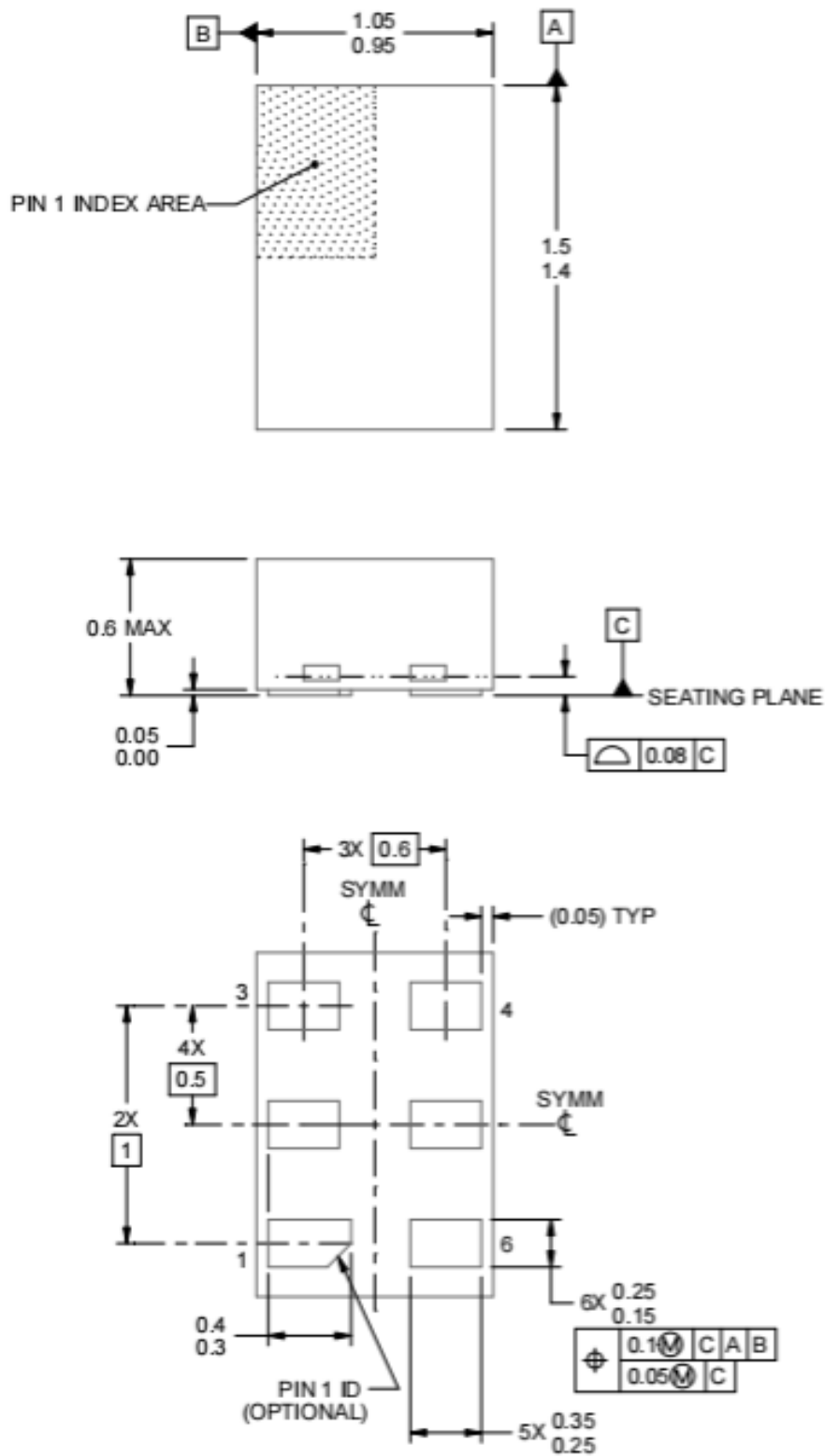


Symbol	Dim in mm		
	MIN	TYP	MAX
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.90	0.95	1.00
b	0.15	0.25	0.35
C	0.10	0.12	0.15
D	1.80	2.00	2.20
E	2.15	2.25	2.35
E1	1.15	1.25	1.35
e	0.650TYP.		
e1	1.20	1.30	1.40
L	0.25	0.30	0.40
L2	0.15TYP.		
Y	0.00	0.05	0.10
θ	4°	8°	12°

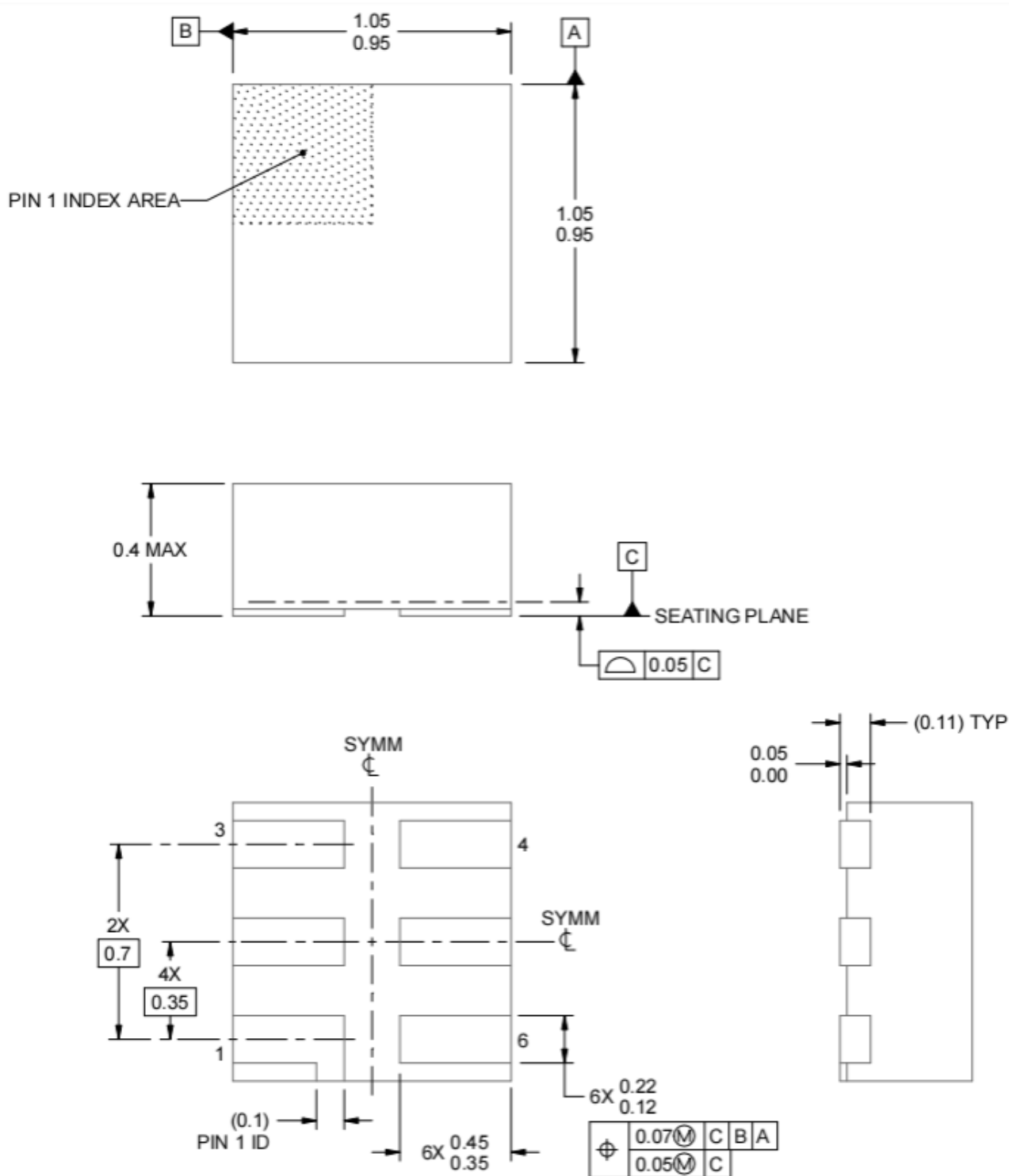
7.3 SOT5X3



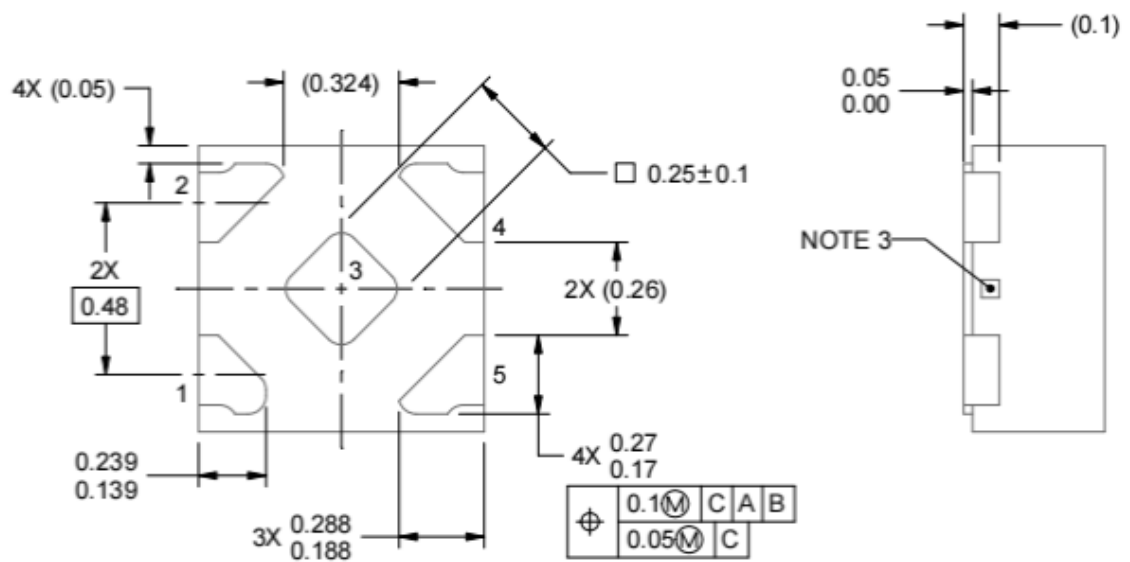
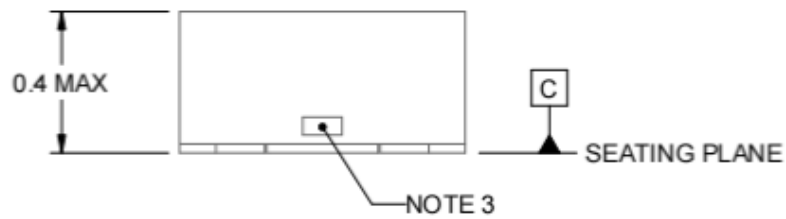
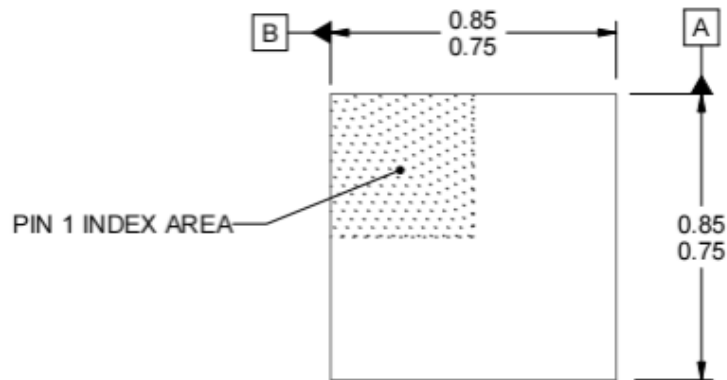
7.4 DFN(BD)-6

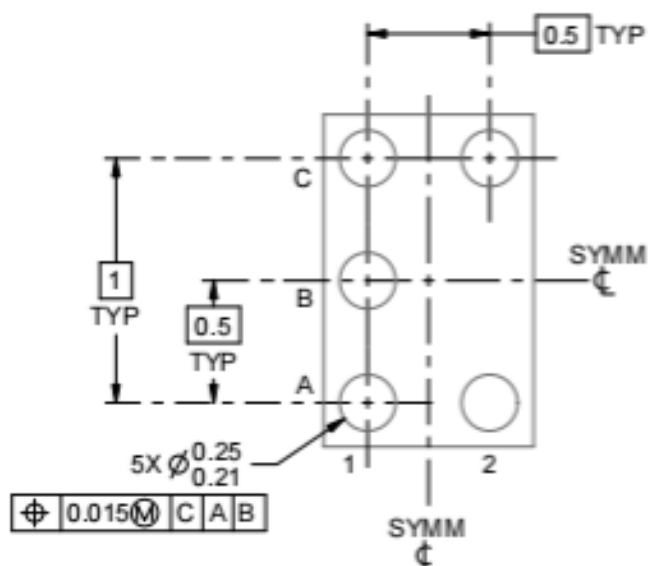
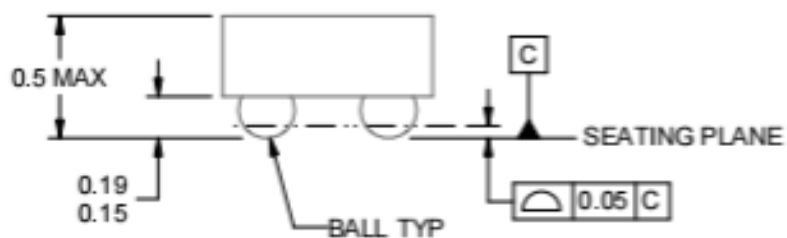


7.5 DFN(CE)-6



7.6 DFN5





E: Max = 0.918 mm, Min = 0.858 mm

7.8 DSBGA(CG)

