38C1 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0075-0240Z
Rev.2.40
2004.6.14

DESCRIPTION

The 38C1 group is the 8-bit microcomputer based on the 740 family core technology.

The 38C1 group has the LCD drive control circuit, an 8-channel A/D converter, and serial I/O as additional functions.

The various microcomputers in the 38C1 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

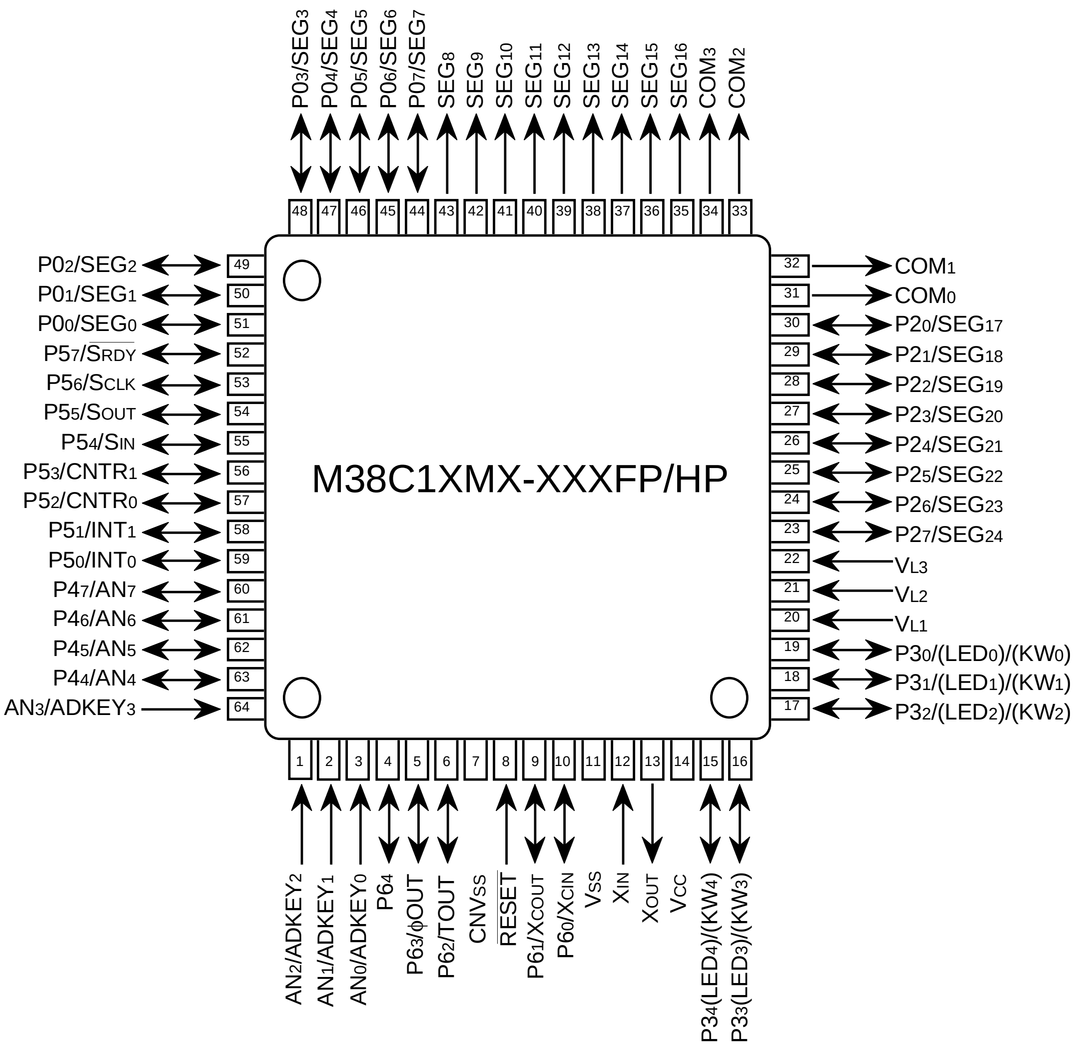
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .... 0.5 µs (at 8 MHz oscillation frequency)
- Memory size
  - ROM .... 16 K to 24 K bytes
  - RAM .... 384 to 512 bytes
- Programmable input/output ports (Ports P2–P6) 30
- Segment output pin/Input port (Port P0) 8
- Software pull-up/pull-down resistor .... Ports P0, P2–P6
- Interrupts .... 13 sources, 13 vectors (includes key input interrupt)
- Timers .... 8-bit × 3, 16-bit × 2
- Serial I/O .... 8-bit × 1 (Clock-synchronous)
- A/D converter .... 8-bit × 8 channels (It can be used in the low-speed mode.)
- LCD drive control circuit
  - Bias 1/1, 1/2, 1/3
  - Duty .... Static, 1/2, 1/3, 1/4
  - Common output 4
  - Segment output 25
- Main clock generating circuit .... 1 (connect to external ceramic resonator or on-chip oscillator)
- Sub clock generating circuit .... 1 (connect to external quartz-crystal oscillator)
- Power source voltage
  - In high-speed mode ($f(X_{IN}) \leq 8.0$ MHz) .... 4.0 to 5.5 V
  - In middle-speed mode (Mask ROM version: $f(X_{IN}) \leq 6.0$ MHz) .... 1.8 to 5.5 V
  - In middle-speed mode (One Time PROM version: $f(X_{IN}) \leq 6.0$ MHz) .... 2.2 to 5.5 V
  - In low-speed mode (Mask ROM version) .... 1.8 to 5.5 V
  - In low-speed mode (One Time PROM version) .... 2.2 to 5.5 V
- Power dissipation (Mask ROM version)
  - In high-speed mode (frequency divided by 2) .... Typ. 15 mW (V_{CC} = 5 V, $f(X_{IN})$ = 8 MHz , Ta = 25 °C)
  - In low-speed mode .... Typ. 18 µW (V_{CC} = 2.5 V, $f(X_{IN})$ = stop , $f(X_{CIN})$ = 32 kHz , Ta = 25 °C)
- Operating temperature range .... – 20 to 85°C

APPLICATIONS

Household appliances, consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Outline 64P6U-A/64P6Q-A

Fig. 1 Pin configuration of M38C1XMX-XXXFP/HP

FUNCTIONAL BLOCK DIAGRAM

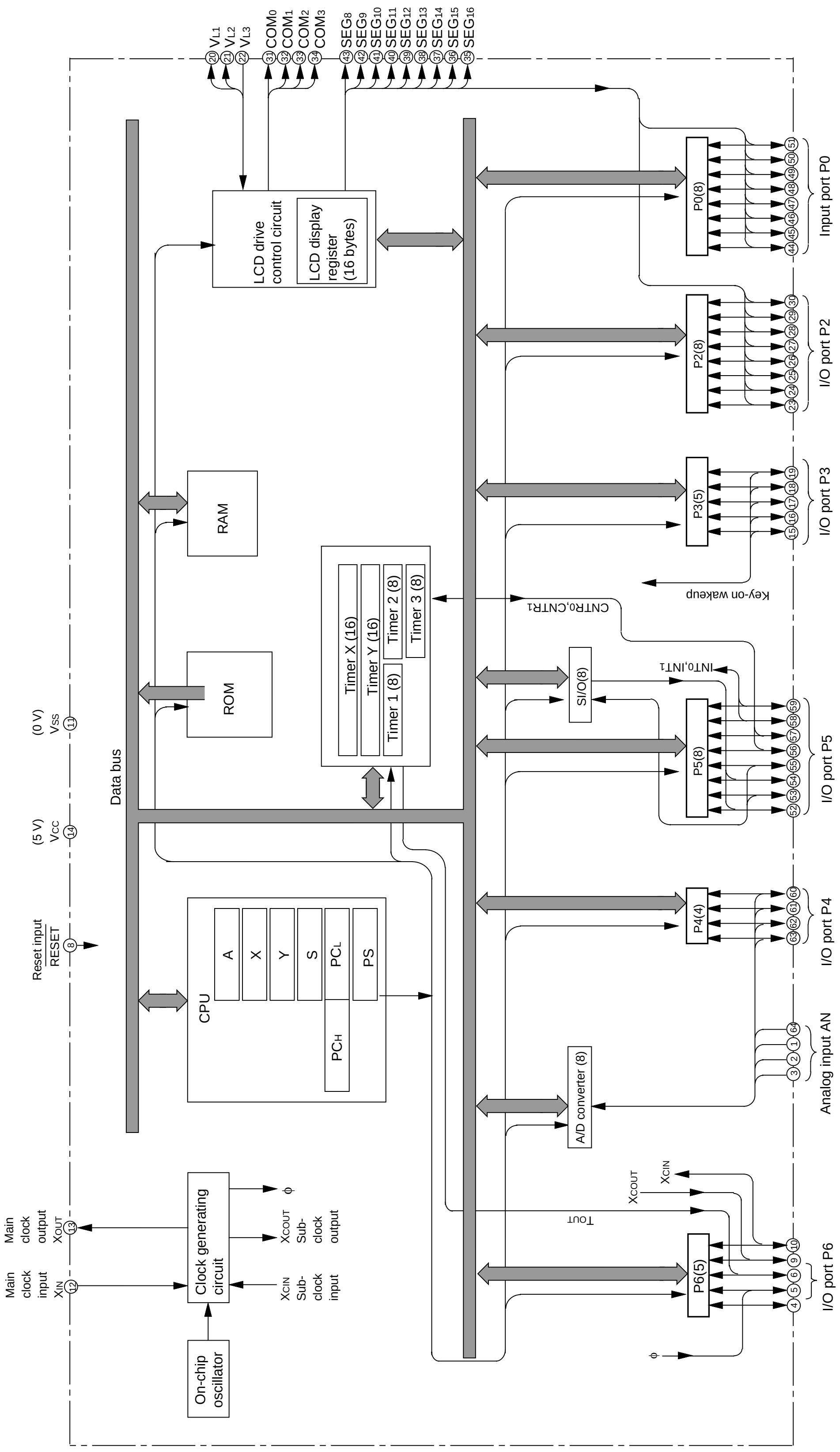


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function except a port function
VCC, VSS	Power source	• Apply voltage of power source to VCC, and 0 V to VSS. (As for VCC, refer to the recommended operating condition)	
CNVSS	CNVSS	• Connect to Vss.	
RESET	Reset input	• Reset input pin for active "L".	
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. A feedback resistor is built-in.	
XOUT	Clock output		
VL1–VL3	LCD power source	• Input 0 ≤ VL1 ≤ VL2 < VL3 voltage.	
COM0–COM3	Common output	• LCD common output pins.	
P00/SEG0–P07/SEG7	Input port P0	• 8-bit input port. • CMOS compatible input level. • 1, 2, 4 or 8-bit input and 8-bit pull-down can be programmed.	• LCD segment output pins
SEG8–/SEG16	Segment output pin	• LCD segment output pin.	
P20/SEG17–P27/SEG24	I/O port P2	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • 1-bit input/output and pull-down can be programmed.	• LCD segment output pins
P30(LED)/KW0–P34(LED)/KW4	I/O port P3	• 5-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • 1-bit input/output and pull-up can be programmed.	• Key input (key-on wake-up) interrupt input pins
AN0/ADKEY0–AN3/ADKEY3	Analog input	• Analog input pins for A/D converter. When these pins are used as ADKEY pins, the input voltage of ADKEY pin which is input "L" level is A/D converted automatically.	• ADKEY input pins
P44/AN4–P47/AN7	I/O port P4	• 4-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • 1-bit input/output and pull-up can be programmed.	• Analog input pins for A/D converter
P50/INT0, P51/INT1	I/O port P5	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • 1-bit input/output and pull-up can be programmed.	• Interrupt input pins
P52/CNTR0 P53/CNTR1			• Timer X, timer Y function pins
P54/SIN P55/SOUT P56/SCLK P57/SRDY			• Serial I/O function pins
P60/XCIN P61/XCOUT	I/O port P6	• 5-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • 1-bit input/output and pull-up can be programmed.	• Sub-clock generating circuit I/O pins (Oscillator is connected. External clock cannot be input directly.)
P62/TOUT			Timer 2 output pin
P63/ϕOUT			System clock ϕ output
P64			

PART NUMBERING

Product M38C1 **3** **M** **6** - **XXX** **FP**

Package type (FP)
FP : 64P6U-A package
HP : 64P6Q-A package

ROM number (XXX)
Omitted in One Time PROM version.

ROM/PROM size (6)
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes
9 : 36864 bytes
A : 40960 bytes
B : 45056 bytes
C : 49152 bytes
D : 53248 bytes
E : 57344 bytes
F : 61440 bytes

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

Memory type (M)
M: Mask ROM version
E: One Time PROM version

RAM size (3)
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes
8 : 1536 bytes
9 : 2048 bytes

Fig. 3 Part numbering

GROUP EXPANSION

Renesas plans to expand the 38C1 group as follows.

Memory Type

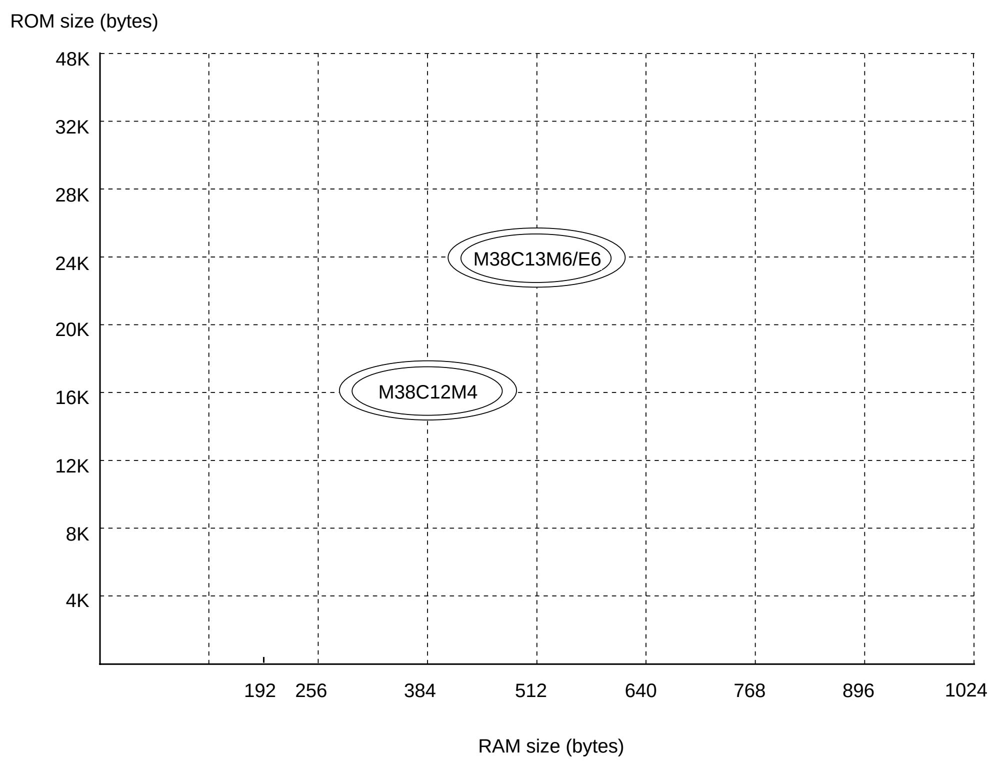
Support for Mask ROM version, One Time PROM version.

Memory Size

ROM/PROM size .... 16 K to 24 K bytes
RAM size .... 384 to 512 bytes

Packages

64P6Q-A .... 0.5 mm-pitch plastic molded QFP
64P6U-A .... 0.8 mm-pitch plastic molded QFP



Products under development or planning :the development schedule and specification may be revised without notice.

Fig. 4 Memory expansion plan

Currently products are listed below.

Table 2. List of products **As of June. 2004**

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38C12M4-XXXFP	16384 (16256)	384	64P6U-A	Mask ROM version
M38C12M4-XXXHP			64P6Q-A	
M38C13M6-XXXFP	24576 (24446)	512	64P6U-A	
M38C13M6-XXXHP			64P6Q-A	
M38C13E6FP			64P6U-A	One Time PROM version (shipped in blank)
M38C13E6HP			64P6Q-A	

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 38C1 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.
Machine-resident 740 family instructions are as follows:
The FST and SLW instruction cannot be used.
The STP, WIT, MUL, and DIV instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.
The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.
Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

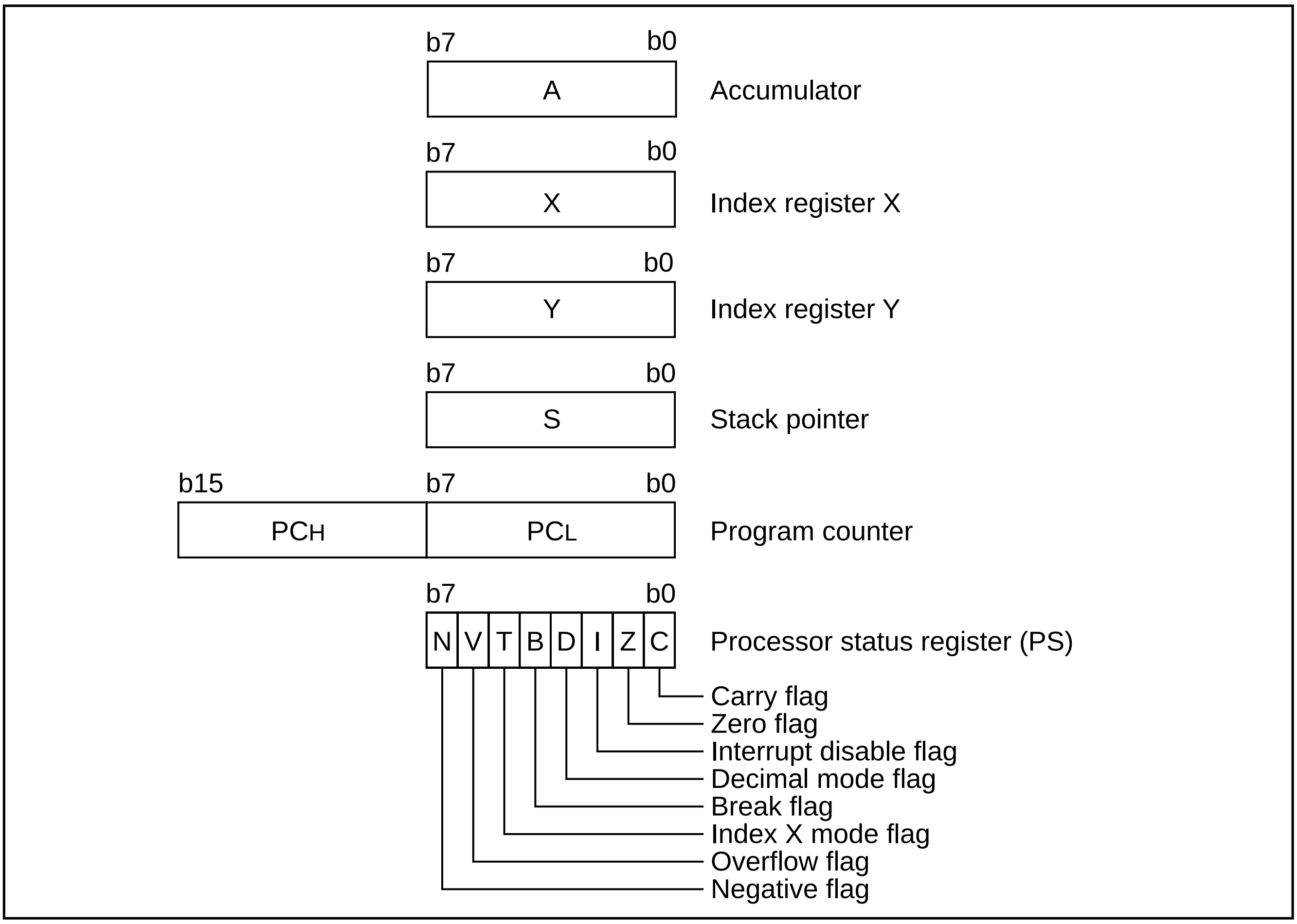


Fig. 5 740 Family CPU register structure

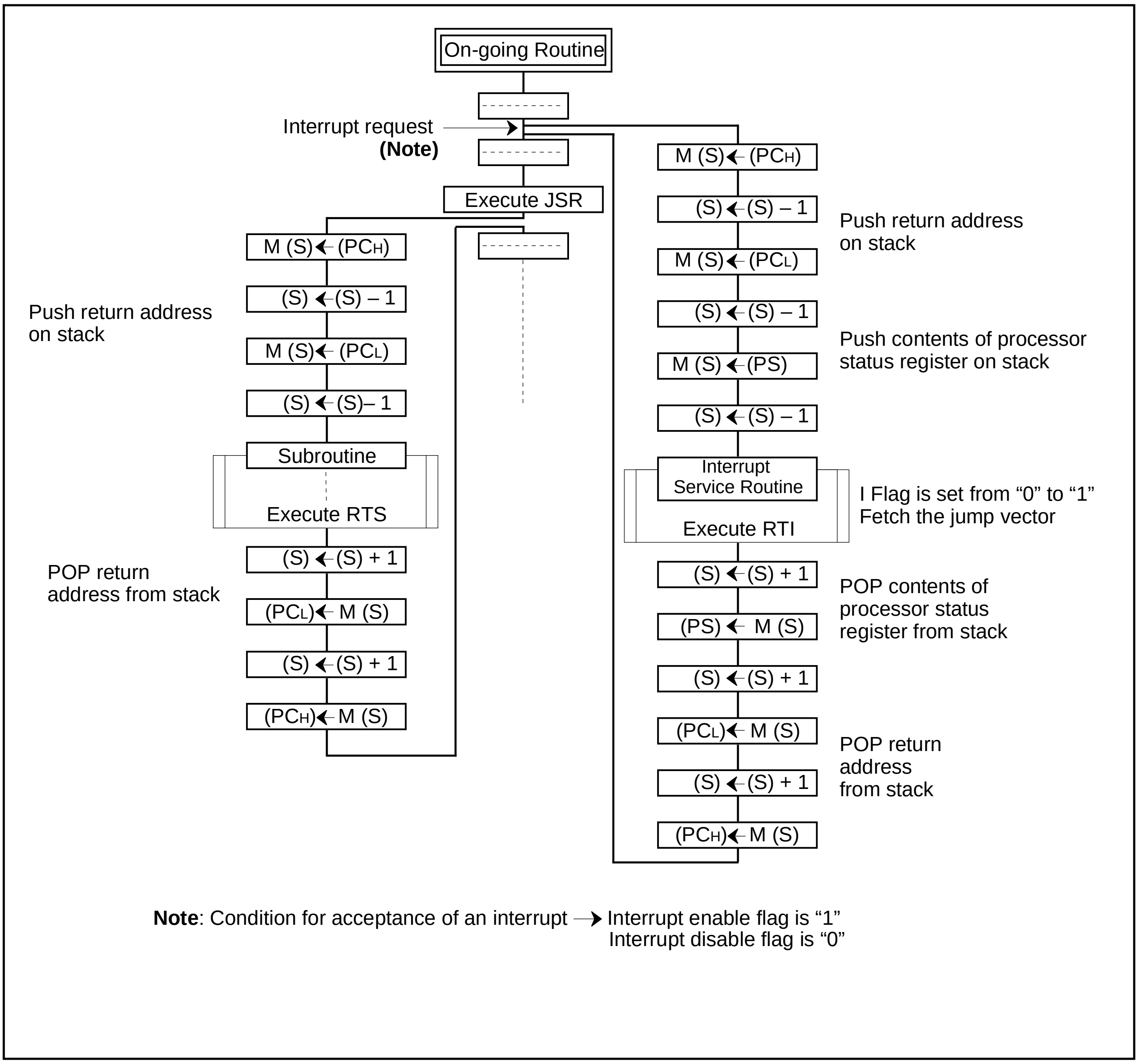


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)
  The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
- Bit 1: Zero flag (Z)
  The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.
- Bit 2: Interrupt disable flag (I)
  The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
  Interrupts are disabled when the I flag is “1”.
- Bit 3: Decimal mode flag (D)
  The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
  Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.
- Bit 4: Break flag (B)
  The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.
- Bit 5: Index X mode flag (T)
  When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.
- Bit 6: Overflow flag (V)
  The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.
- Bit 7: Negative flag (N)
  The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] $003B_{16}$

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address $003B_{16}$.

After system is released from reset, the on-chip oscillator mode is selected, and the XIN–XOUT oscillation and the XCIN–XCOUT oscillation are stopped.

When the low-, middle- or high-speed mode is used after the XIN–XOUT oscillation and the XCIN–XCOUT oscillation are enabled, wait in the on-chip oscillator mode until oscillation stabilizes, and then, switch the operation mode.

When the middle- and high-speed mode are not used (XIN-XOUT oscillation and external clock input are not performed), connect XIN to VCC through a resistor.

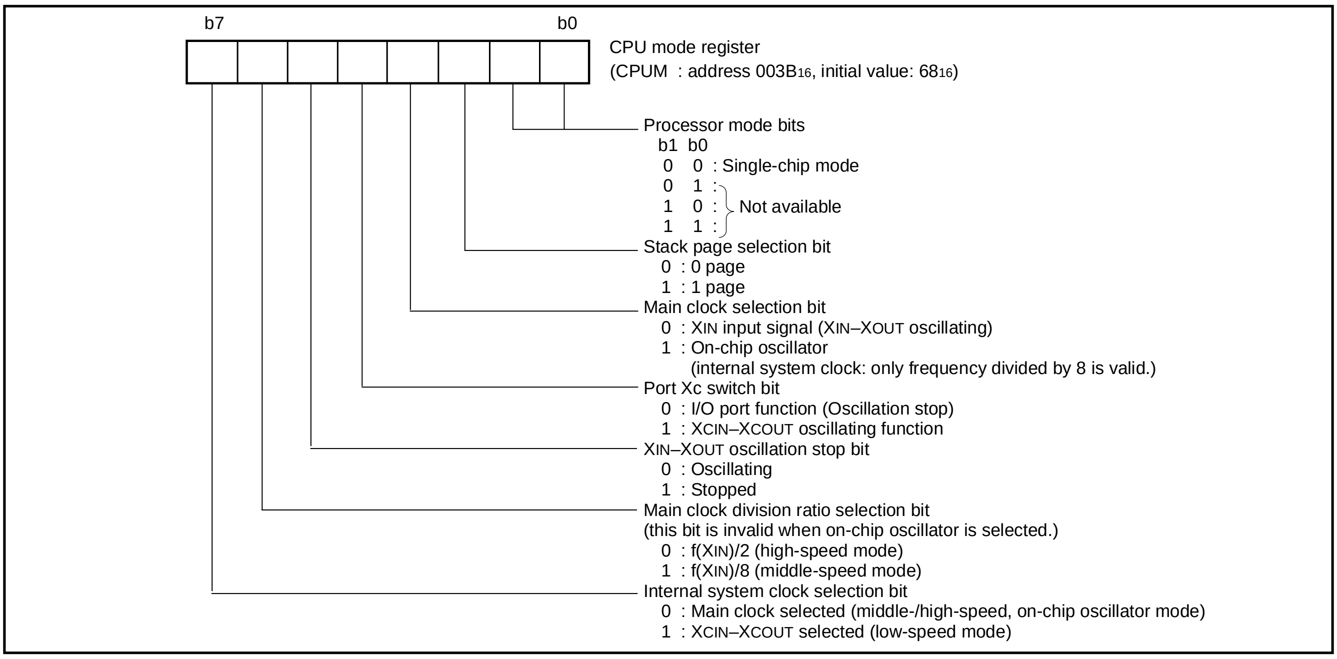


Fig. 7 Structure of CPU mode register

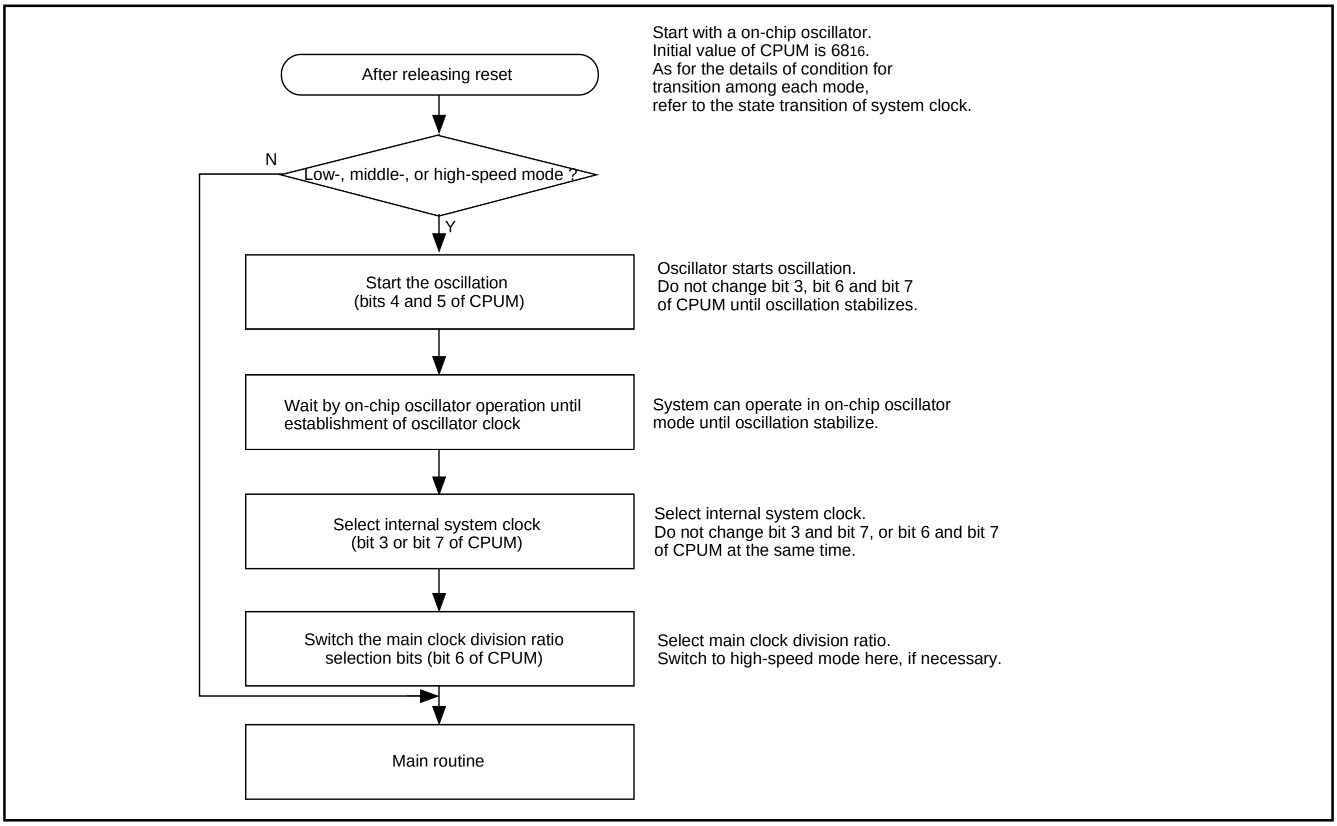


Fig. 8 Switching method of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}

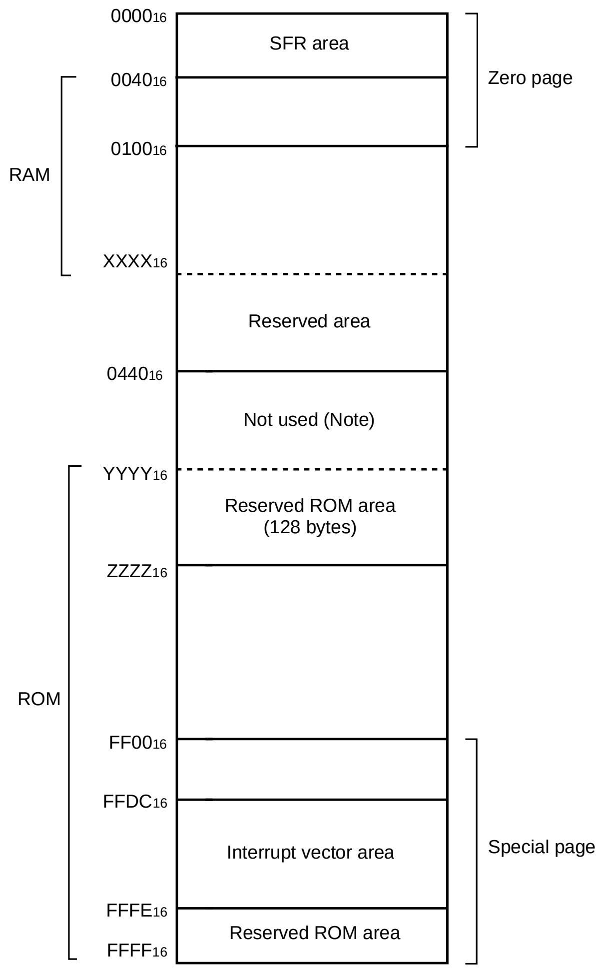


Fig. 9 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer X (low) (TXL)
0001_{16}		0021_{16}	Timer X (high) (TXH)
0002_{16}		0022_{16}	Timer Y (low) (TYL)
0003_{16}		0023_{16}	Timer Y (high) (TYH)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 1 (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 (T2)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 3 (T3)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer X mode register (TXM)
0008_{16}	Port P4, ADKEY pin selection (P4)	0028_{16}	Timer Y mode register (TYM)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 123 mode register (T123M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	ϕ output control register
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	
$000C_{16}$	Port P6 (P6)	$002C_{16}$	Temporary data register 1 (TD0)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	Temporary data register 2 (TD1)
$000E_{16}$		$002E_{16}$	Temporary data register 3 (TD2)
$000F_{16}$		$002F_{16}$	RRF register (RRF)
0010_{16}	LCD display register 0(LCD0)	0030_{16}	
0011_{16}	LCD display register 1(LCD1)	0031_{16}	
0012_{16}	LCD display register 2(LCD2)	0032_{16}	
0013_{16}	LCD display register 3(LCD3)	0033_{16}	PULL register
0014_{16}	LCD display register 4(LCD4)	0034_{16}	A/D control register (ADCON)
0015_{16}	LCD display register 5(LCD5)	0035_{16}	A/D conversion register (AD)
0016_{16}	LCD display register 6(LCD6)	0036_{16}	
0017_{16}	LCD display register 7(LCD7)	0037_{16}	
0018_{16}	LCD display register 8(LCD8)	0038_{16}	Segment output enable register (SEG)
0019_{16}	LCD display register 9(LCD9)	0039_{16}	LCD mode register (LM)
$001A_{16}$	LCD display register 10(LCD10)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	LCD display register 11(LCD11)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	LCD display register 12(LCD12)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$	Serial I/O control register (SIOCON)	$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$	Serial I/O register (SIO)	$003F_{16}$	Interrupt control register 2(ICON2)

Fig. 10 Memory map of special function register (SFR)

I/O PORTS

Direction Registers (Ports P2–P6)

The I/O ports (P2–P6) have direction registers which determine the input/output direction of each individual pin.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Port P0

Port P0 is an input port.

$P0_0$/SEG_0-$P0_7$/SEG_7 pins are also used as segment output pins. These pins can be used as segment output pins by setting segment output enable bits.

Pull-up/Pull-down Control

By setting the PULL register (address 0033_{16}), I/O ports can control pull-up/pull-down (pins also used as segment output pin: pull-down, other pins: pull-up). Pull-up/pull-down of pins are performed by setting the PULL register to “1”.

However, the contents of PULL register does not affect ports programmed as the output ports.

Input port P0 and I/O port P2 are pulled-down in the initial state.

Also, the pull-down setting is invalid for pins set to segment output with the segment output enable register (address 0038_{16}).

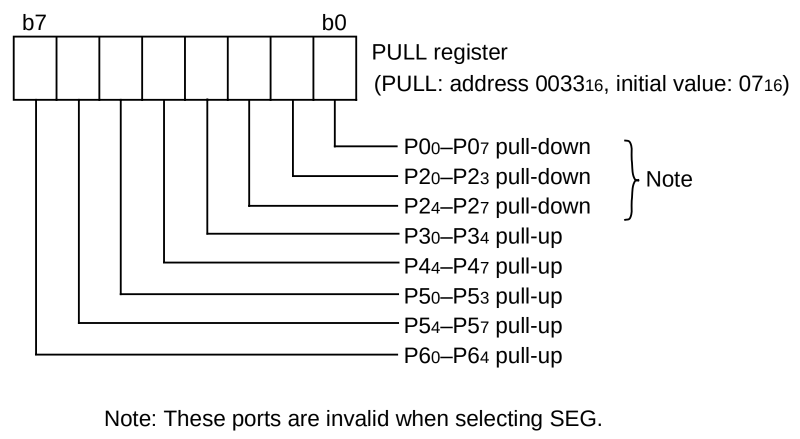


Fig. 11 Structure of PULL register

Table 5 List of I/O port function

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Fig. No.
COM$_0$–COM$_3$	Common	Output	LCD common output		LCD mode register	(16)
P0$_0$/SEG$_0$–P0$_7$/SEG$_7$	Input Port P0	Input, individual bits	CMOS compatible input level	LCD segment output	PULL register Segment output enable register LCD0–LCD3	(1)
SEG$_8$–/SEG$_{16}$	Segment	Output	LCD segment output		LCD mode register LCD4–LCD8	(17)
P2$_0$/SEG$_{17}$–P2$_7$/SEG$_{24}$	I/O Port P2	Input/output individual bits	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register Segment output enable register LCD8–LCD12	(2)
P3$_0$(LED)/KW$_0$–P3$_4$(LED)/KW$_4$	I/O Port P3	Input/output individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register Interrupt control register	(3)
AN$_0$/ADKEY$_0$–AN$_3$/ADKEY$_3$	A/D conversion input	Input	Analog input	ADKEY input	A/D control register P4 data latch (ADKEY selected)	(15)
P4$_4$/AN$_4$–P4$_7$/AN$_7$	I/O Port P4	Input/output individual bits	CMOS 3-state output CMOS compatible input level	A/D conversion input	PULL register A/D control register	(4)
P5$_0$/INT$_0$, P5$_1$/INT$_1$	I/O Port P5	Input/output individual bits	CMOS 3-state output CMOS compatible input level	Interrupt input	PULL register Interrupt edge selection register	(3)
P5$_2$/CNTR$_0$				Timer X function input/output	PULL register Timer X mode register	(5)
P5$_3$/CNTR$_1$				Timer Y function input	PULL register Timer Y mode register	(6)
P5$_4$/SIN				Serial I/O function output	PULL register Serial I/O control register	(7)
P5$_5$/SOUT						(8)
P5$_6$/SCLK						(9)
P5$_7$/SRDY						(10)
P6$_0$/XCIN	I/O port P6	Input/output individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit input/output	PULL register CPU mode register	(11)
P6$_1$/XCOUT						(12)
P6$_2$/TOUT				Timer 2 output	PULL register Timer X mode register	(13)
P6$_3$/ϕOUT				ϕ clock output	PULL register ϕ output control register	(14)
P6$_4$					PULL register	(18)

Notes 1: For details of how to use double function ports as function I/O ports,refer to the applicable sections.
2: When an input level is at an intermediate potential,a current will flow from VCC to VSS through the input-stage gate. Especially, power source current may increase during execution of the STP and WIT instructions. Fix the unused input pins to “H” or “L” through a resistor.

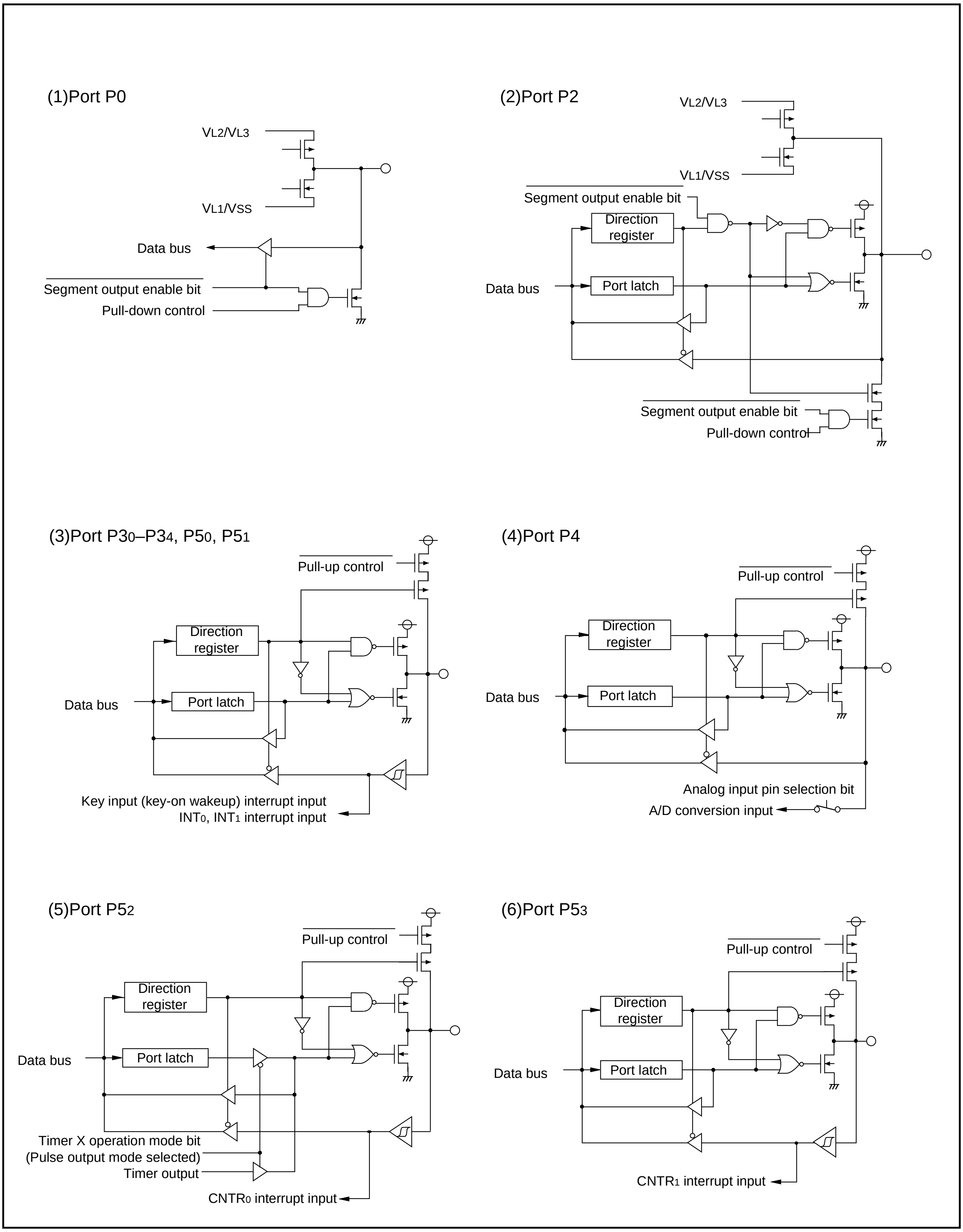
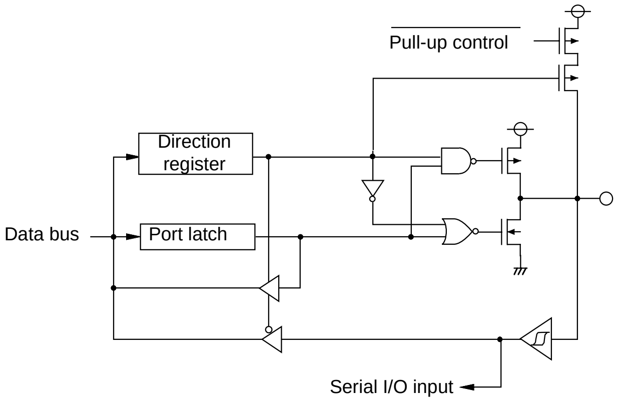
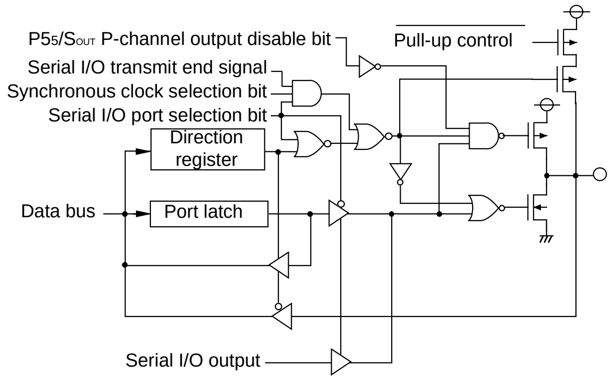


Fig. 12 Port block diagram (1)

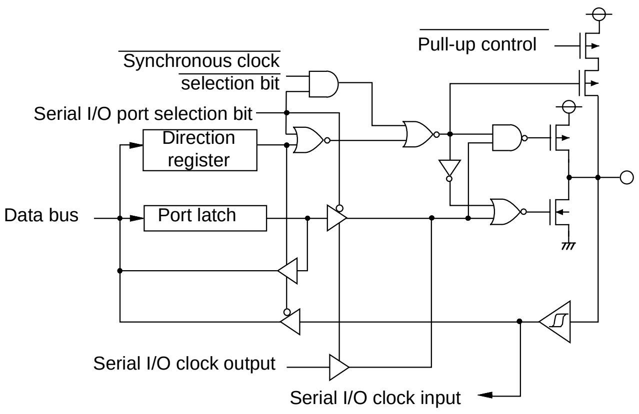
(7)Port P5$_4$



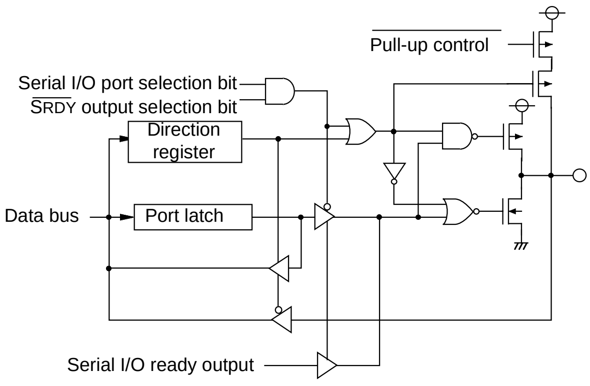
(8)Port P5$_5$



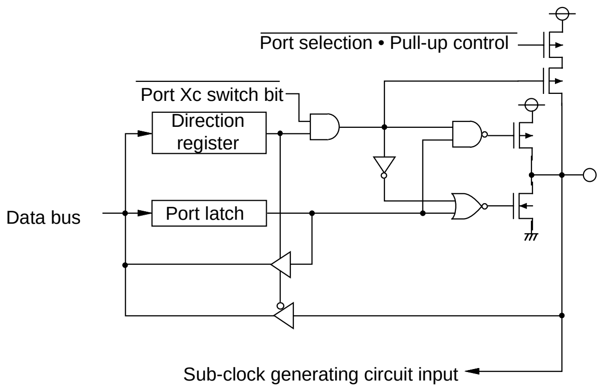
(9)Port P5$_6$



(10)Port P5$_7$



(11)Port P6$_0$



(12)Port P6$_1$

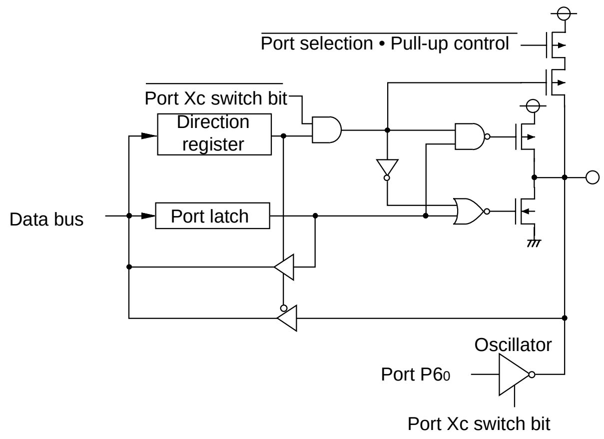
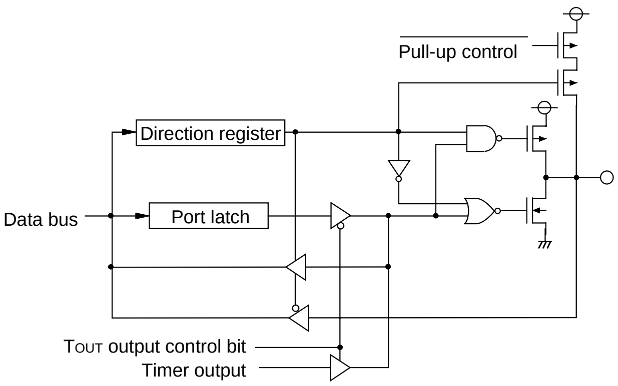
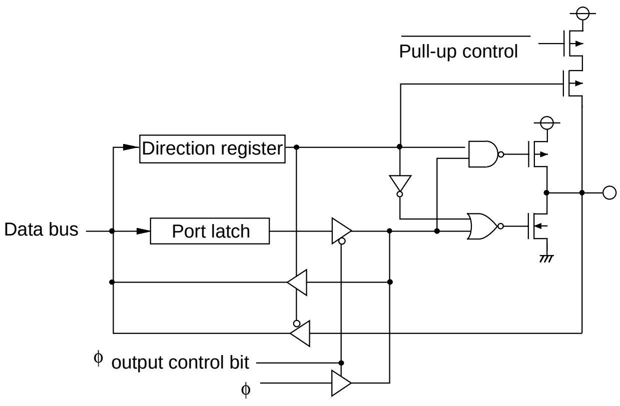


Fig. 13 Port block diagram (2)

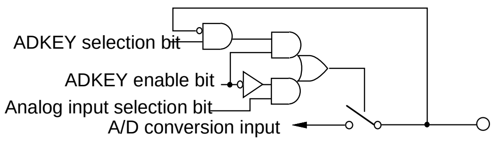
(13)Port $P6_2$



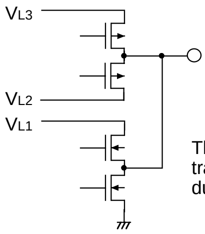
(14)Port $P6_3$



(15)AN_0/$ADKEY_0$–AN_3/$ADKEY_3$

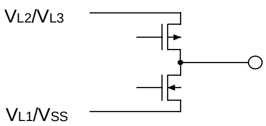


(16)COM_0–COM_3



The gate input signal of each transistor is controlled by the LCD duty ratio and the bias value.

(17)SEG_8–SEG_{16}



The voltage applied to the sources of P-channel and N-channel transistors is the controlled voltage by the bias value.

(18)Port $P6_4$

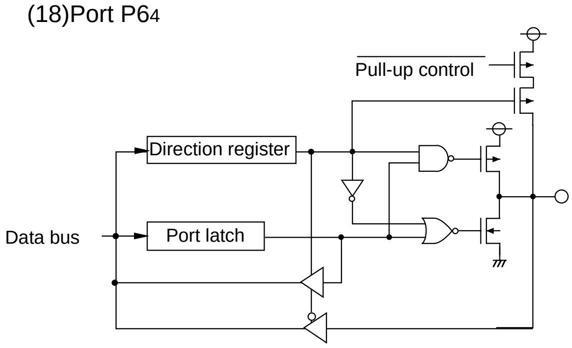


Fig. 14 Port block diagram (3)

INTERRUPTS

Interrupts occur by thirteen sources: five external, seven internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".
Interrupt enable bits can be set or cleared by software.
Interrupt request bits can be cleared by software, but cannot be set by software.
The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.
When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:
1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■ Notes on Interrupts

When the active edge of an external interrupt (INT_0 , INT_1, $CNTR_0$ or $CNTR_1$) is set or an interrupt source where several interrupt source is assigned to the same vector address is switched, the corresponding interrupt request bit may also be set. Therefore, take following sequence:
(1) Disable the interrupt.
(2) Set the interrupt edge selection register (Timer X control register for CNTR0, Timer Y mode register for $CNTR_1$).
(3) Clear the set interrupt request bit to "0."
(4) Enable the interrupt.

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Timer X	4	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	5	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 1	6	$FFEF_{16}$	$FFEE_{16}$	At timer 1 underflow	
Timer 3	7	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
$CNTR_0$	8	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	9	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer 2	10	$FFE7_{16}$	$FFE6_{16}$	At timer 2 underflow	
Serial I/O	11	$FFE3_{16}$	$FFE2_{16}$	At completion of serial I/O data transmission or reception	
Key input (Key-on wake-up)	12	$FFE1_{16}$	$FFE0_{16}$	At falling of conjunction of input level for port P3 (at input mode)	External interrupt (valid at falling)
A/D conversion	13	$FFDF_{16}$	$FFDE_{16}$	At completion of A/D conversion	Valid when A/D interrupt is selected
BRK instruction	14	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

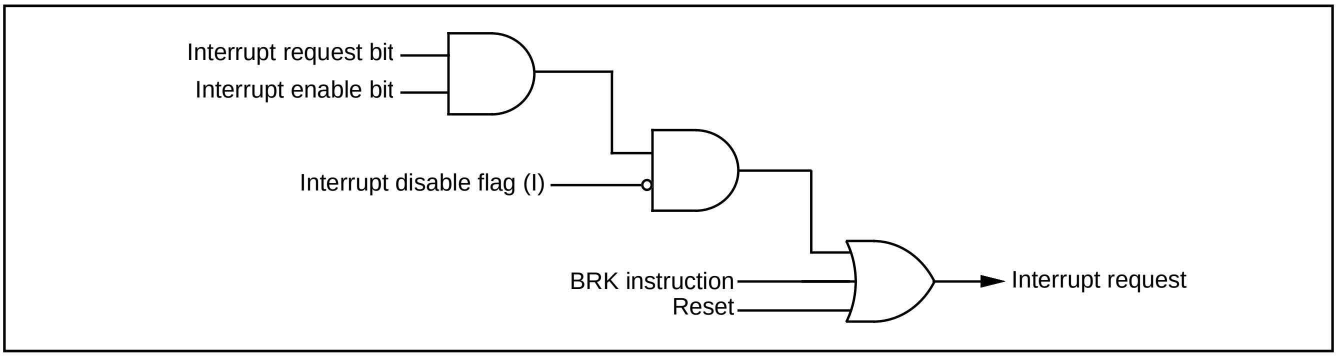


Fig. 15 Interrupt control

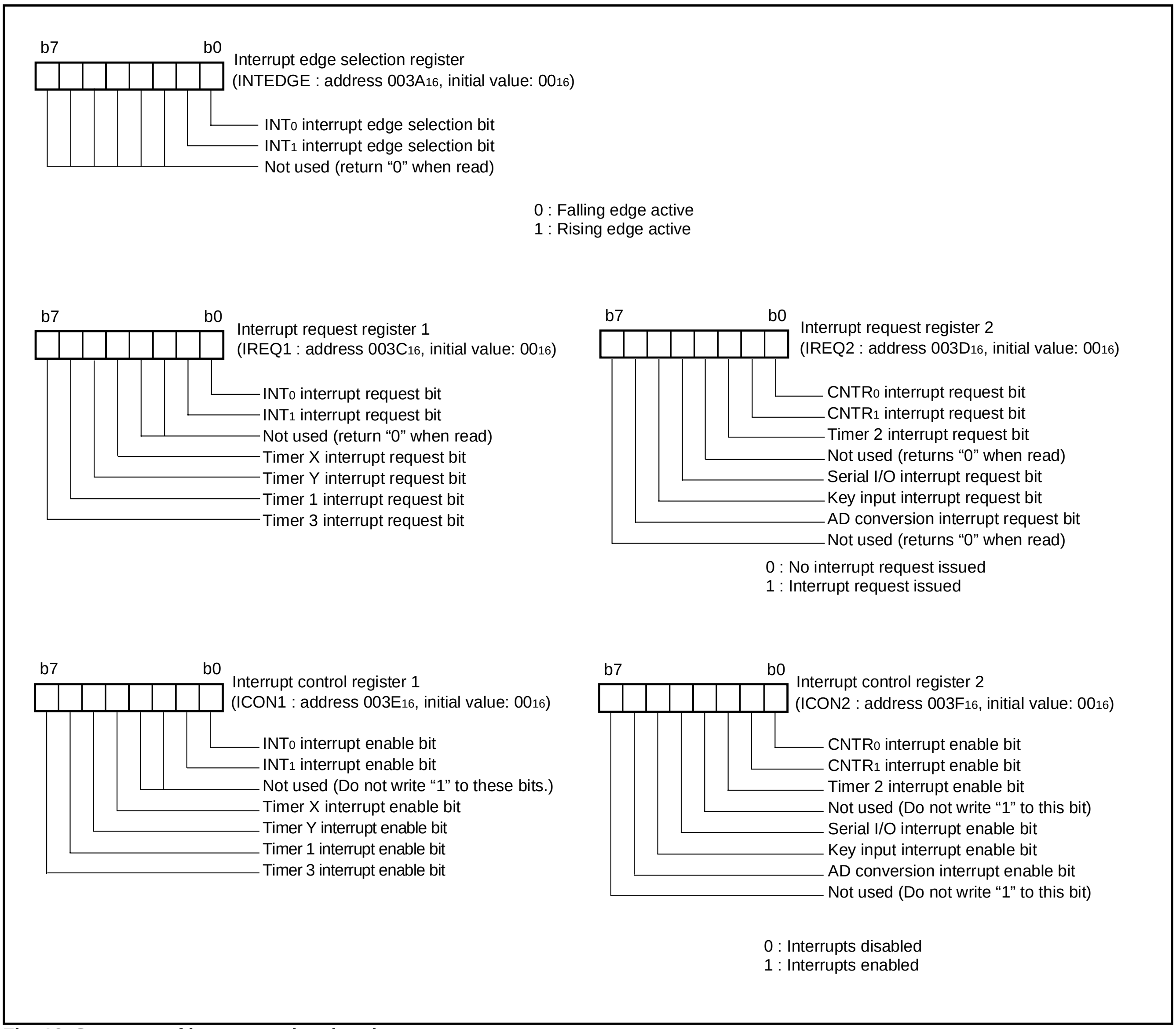


Fig. 16 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

A Key-on wake up interrupt request is generated by applying "L" level voltage to any pin of port P3 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 17, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports $P3_0$–$P3_3$.

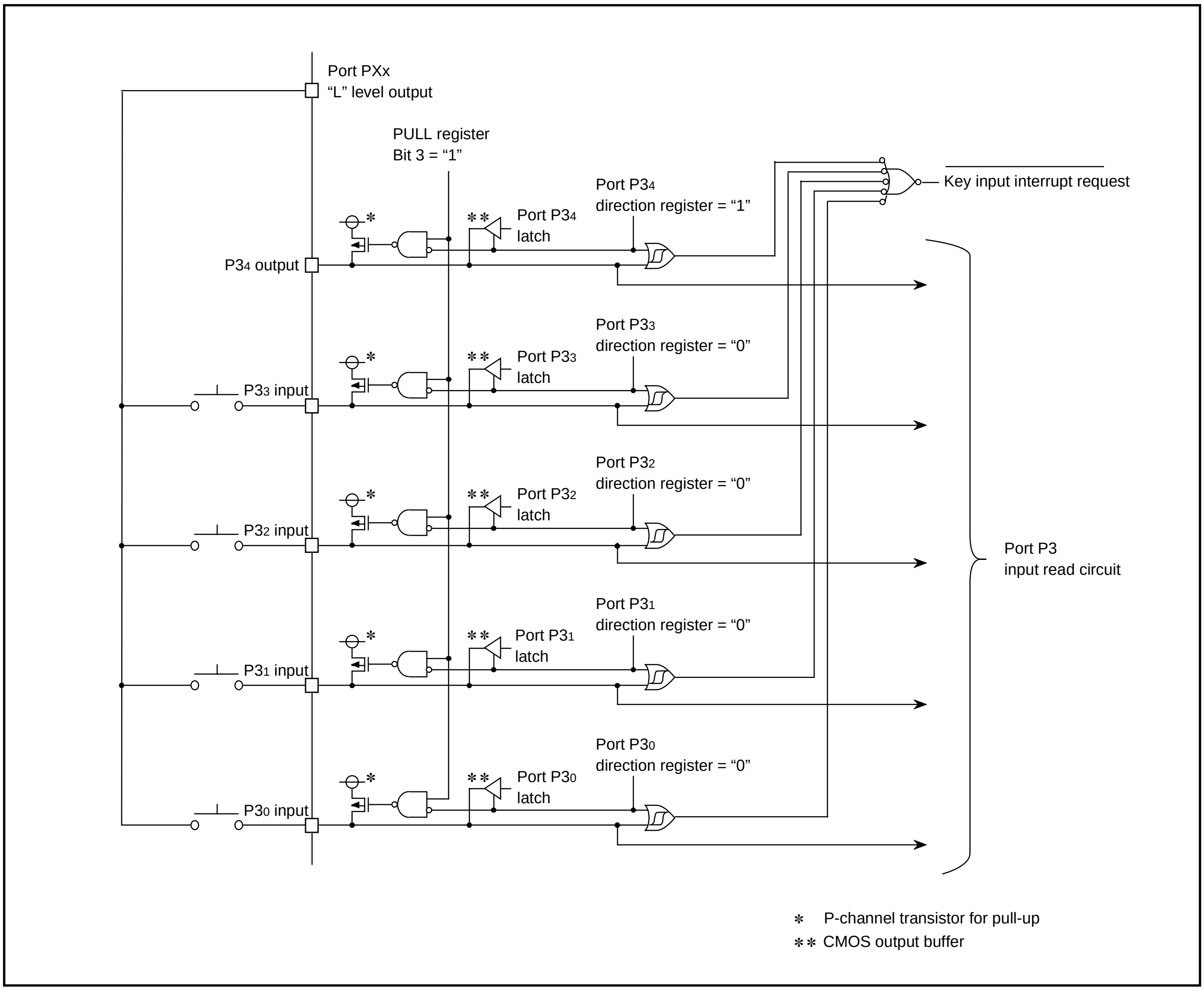
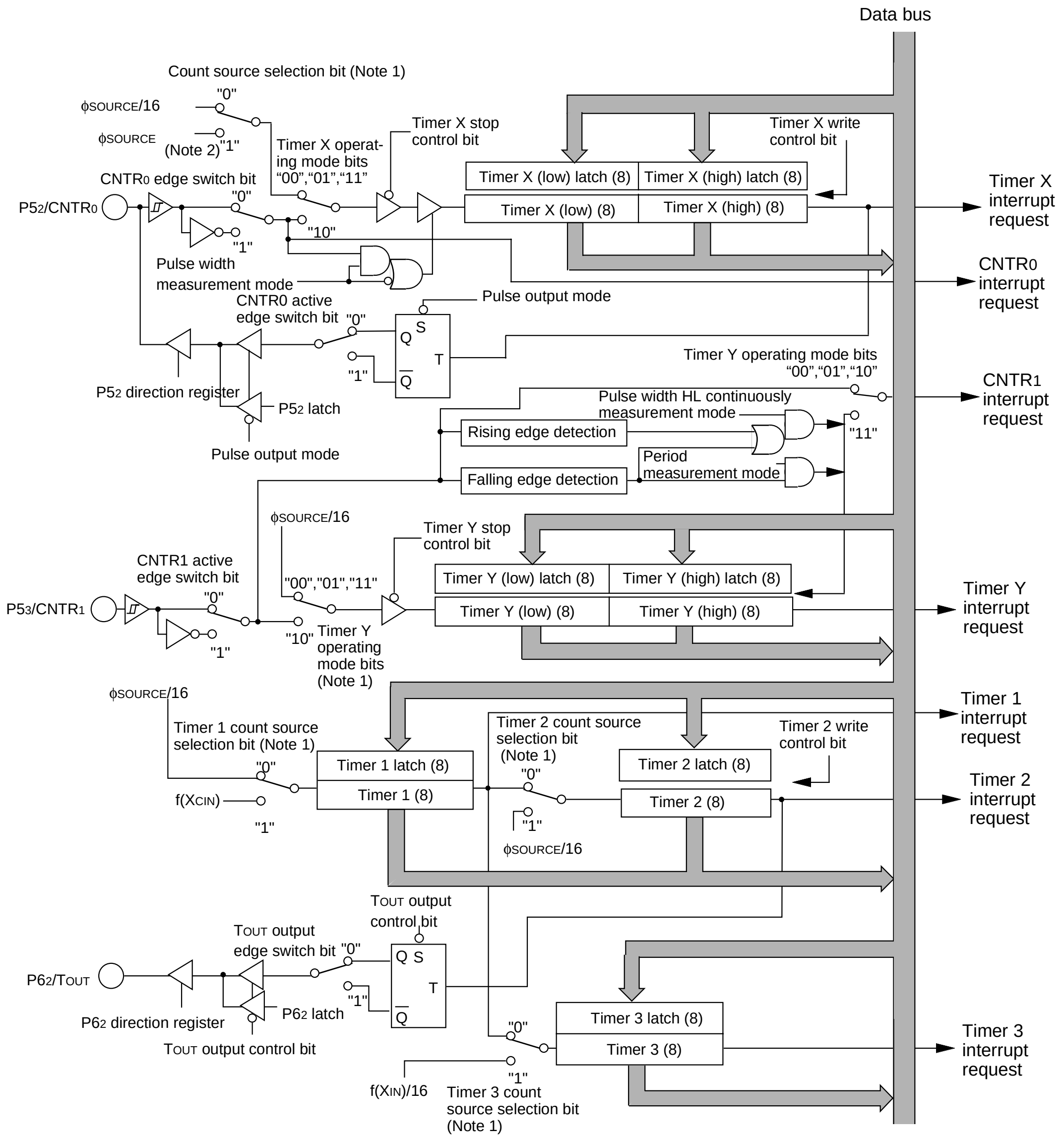


Fig. 17 Connection example when using key input control register, key input interrupt and port P3 block diagram

TIMERS

The 38C1 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.
All timers are down count timers. When the timer reaches “0”, an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to “1”.

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.



ϕSOURCE: represents the supply source of internal clock ϕ. It is the oscillation frequency of XIN input in the middle- and high-speed mode, on-chip oscillator in the on-chip oscillator mode, and sub-clock in the low-speed mode.

Notes 1: Internal clock in the low-speed mode is the sub-clock oscillation/2.
Internal clock in the on-chip oscillator mode is the internal on-chip oscillator oscillation/8.
Except CNTR input, timer 1 and timer 3 count sources, the clock except system clock cannot be used as the count source.

2: ϕSOURCE can be selected as the timer X count source only in the pulse output mode.
Write “0” to the count source selection bit except in the pulse output mode.

Fig. 18 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer mode

The timer counts the followings;

- f(X$_{IN}$) (input frequency to X$_{IN}$ pin) divided by 16 in middle-, or high-speed mode
- f(X$_{CIN}$) (sub-clock oscillation frequency) divided by 16 in low-speed mode
- f(XR$_{OSC}$) (on-chip oscillator oscillation frequency) divided by 16 in on-chip oscillator mode

(2) Pulse output mode

Each time the timer underflows, a signal output from the CNTR$_0$ pin is inverted and f(X$_{IN}$), f(R$_{OSC}$) or f(X$_{CIN}$) can be selected for the count source. Except for them, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P5$_2$ direction register to output mode.

(3) Event counter mode

The timer counts signals input through the CNTR$_0$ pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P5$_2$ direction register to input mode.

(4) Pulse width measurement mode

The count source is f(X$_{IN}$)/16 in the middle-, or high-speed mode, f(R$_{OSC}$)/16 in on-chip oscillator mode, and f(X$_{CIN}$)/16 in the low-speed mode. If CNTR$_0$ active edge switch bit is "0", the timer counts while the input signal of CNTR$_0$ pin is at "H". If it is "1", the timer counts while the input signal of CNTR$_0$ pin is at "L". When using a timer in this mode, set the corresponding port P5$_2$ direction register to input mode.

●Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
If the value is written in latch only, when the value is written in latch at the timer underflow, the value is loaded in the timer X and the latch at the same time. Also, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

■Note on CNTR$_0$ interrupt active edge selection

CNTR$_0$ interrupt active edge depends on the CNTR$_0$ active edge switch bit.

■Note on count source selection bit

Except the pulse output mode, write "0" to the count source selection bit.
When the timer X count source selection bit is set to "1", as for the recommended operating condition of the main clock input frequency f(X$_{IN}$), the rating value at the high-speed mode is applied.

■Note on interrupt in pulse output mode

When the count source selection bit is "1" in the pulse output mode, the timing when the timer X interrupt request occurs may be early or lately for one instruction cycle.

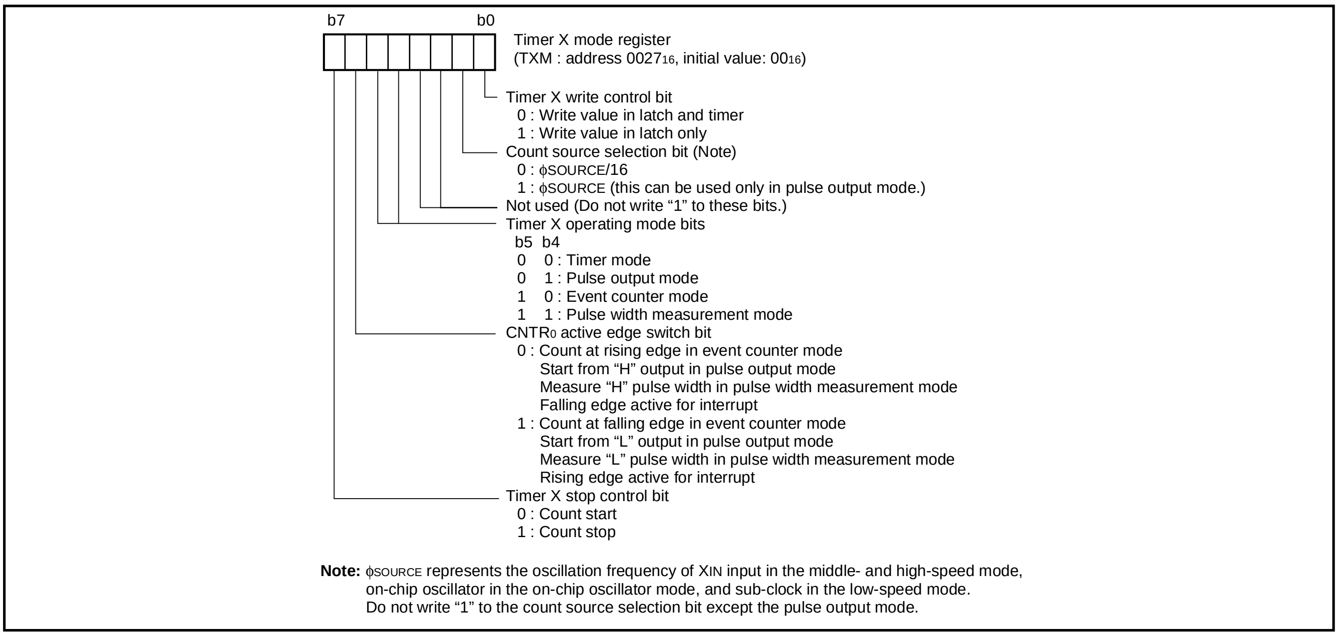


Fig. 19 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer mode

The timer counts the followings;

- f(X$_{IN}$)/16 in middle-, or high-speed mode
- f(X$_{CIN}$)/16 in low-speed mode
- f(XR$_{OSC}$) divided by 16 in on-chip oscillator mode

(2) Period measurement mode

CNTR$_1$ interrupt request is generated at rising/falling edge of CNTR$_1$ pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR$_1$ pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR$_1$ pin input signal is found by CNTR$_1$ interrupt. When using a timer in this mode, set the corresponding port P5$_3$ direction register to input mode.

(3) Event counter mode

The timer counts signals input through the CNTR$_1$ pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P5$_3$ direction register to input mode.

(4) Pulse width HL continuously measurement mode

CNTR$_1$ interrupt request is generated at both rising and falling edges of CNTR$_1$ pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P5$_3$ direction register to input mode.

■Note on CNTR$_1$ interrupt active edge selection

CNTR$_1$ interrupt active edge depends on the CNTR$_1$ active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR$_1$ interrupt request is generated at both rising and falling edges of CNTR$_1$ pin input signal regardless of the setting of CNTR$_1$ active edge switch bit.

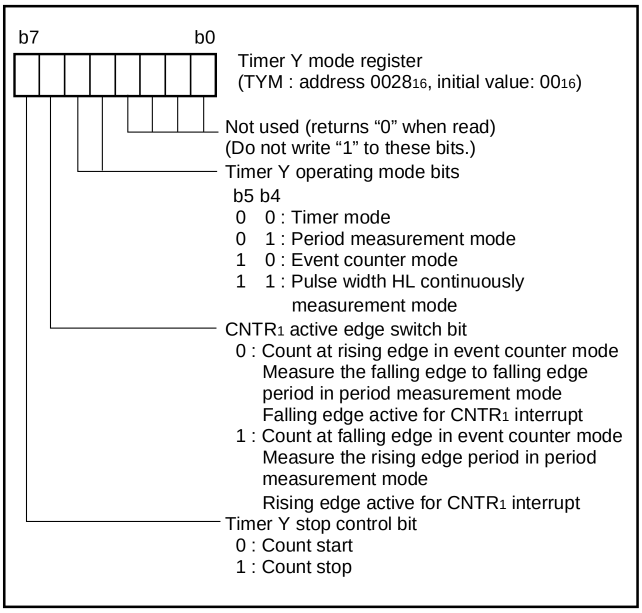


Fig. 20 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

●Timer 2 Write Control

If the timer 2 write control bit is “0”, when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is “1”, when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

●Timer 2 Output Control

When the timer 2 (T_{OUT}) is output enabled, an inversion signal from pin T_{OUT} is output each time timer 2 underflows.

In this case, set the port $P6_2$ shared with the port T_{OUT} to the output mode.

■Note on Timer 1 to Timer 3

When the count source of timers 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

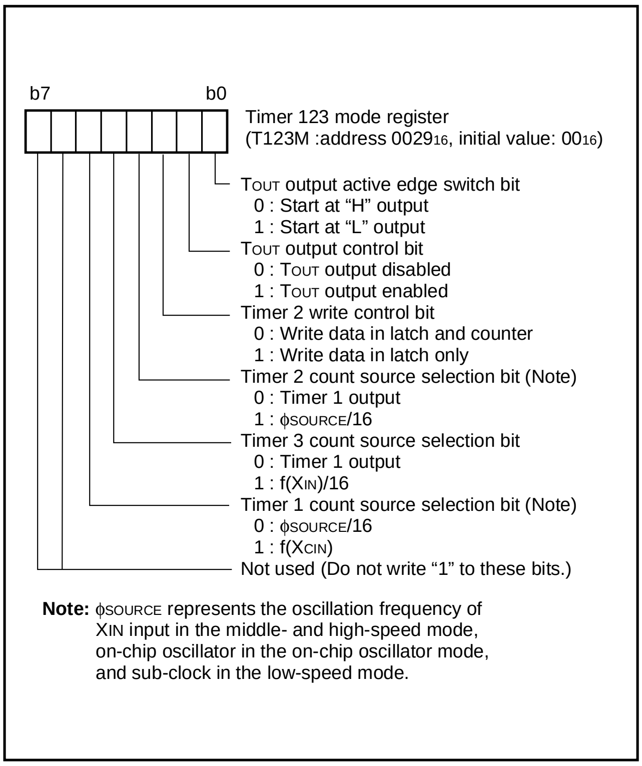


Fig. 21 Structure of timer 123 mode register

Serial I/O

The serial I/O function can be used only for clock synchronous serial I/O.
For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O register.

[Serial I/O Control Register (SIOCON)] 001D16

The serial I/O control register contains 8 bits which control various serial I/O functions.

■ Notes on Serial I/O
Write data to the serial I/O register only when the SCLK pin is “H”.

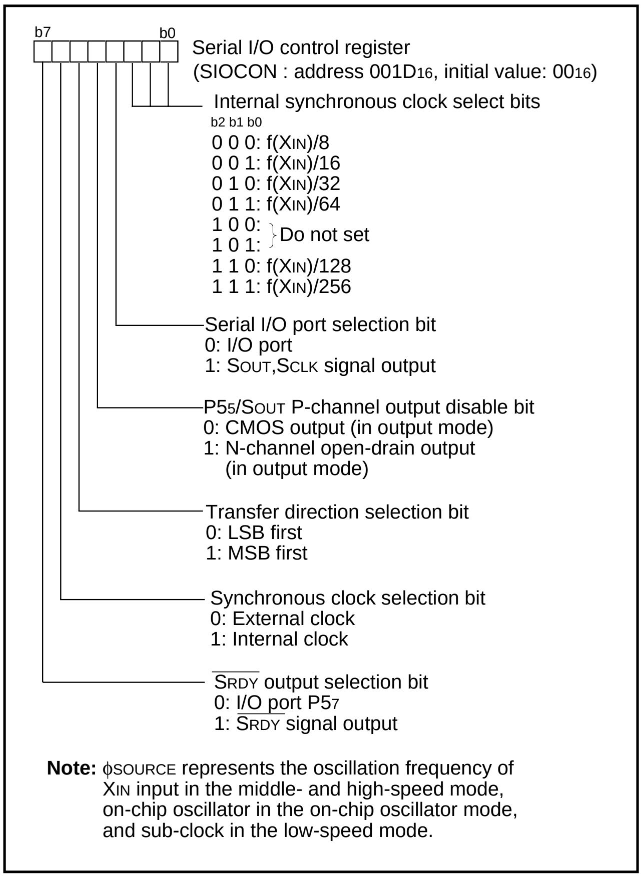


Fig. 22 Structure of serial I/O control register

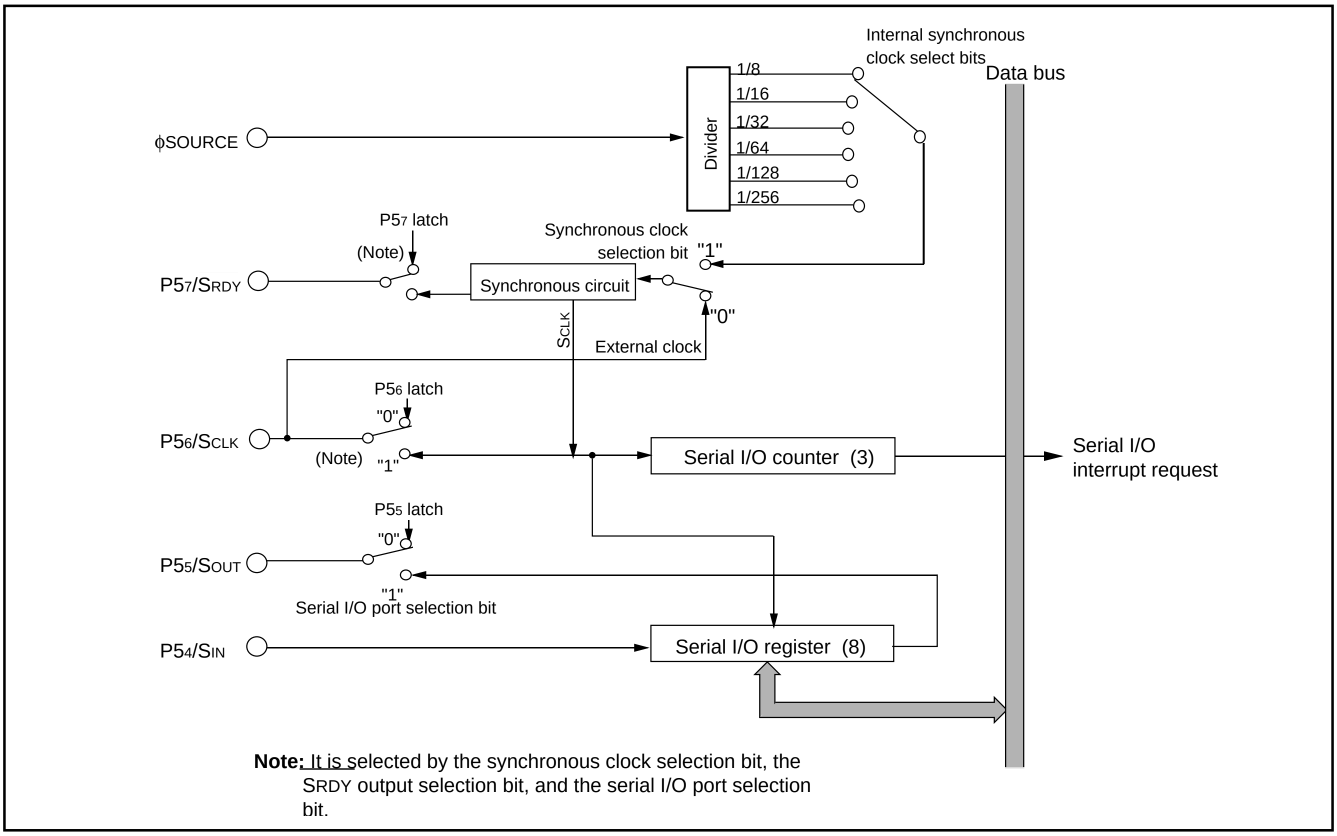
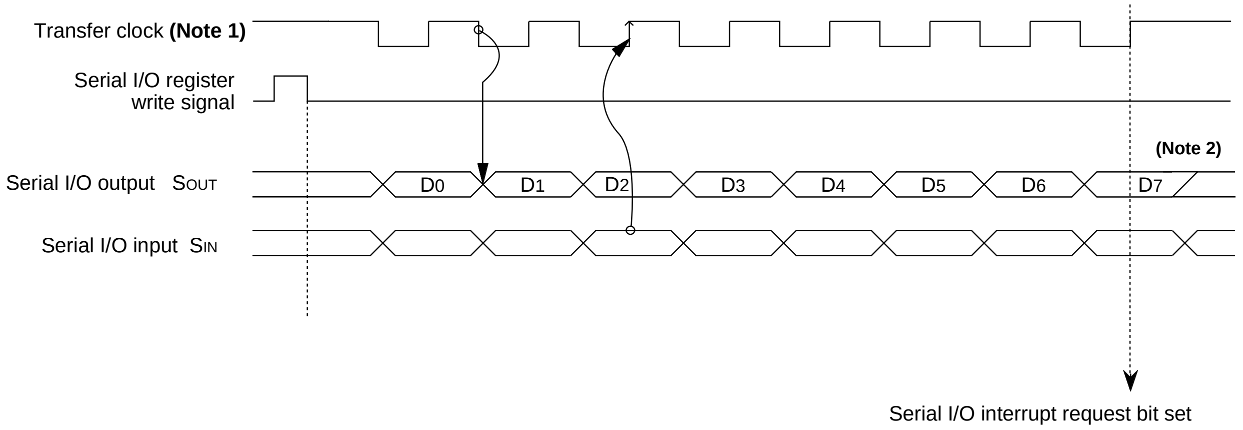


Fig. 23 Block diagram of serial I/O function

RENESAS



Notes 1: When the internal clock is selected as the transfer clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O control register.
2: When the internal clock is selected as the transfer clock, the SOUT pin goes to high impedance after transfer completion. When the external clock is selected as the transfer clock, a content of the serial I/O shift register is continued to shift during inputting a transfer clock. The SOUT pin does not go to high impedance after transfer completion.

Fig. 24 Timing of serial I/O function

A/D CONVERTER

The functional blocks of the A/D converter are described below.

● A/D Converter

The conversion method of this A/D converter is the 8-bit resolution successive comparison method. This A/D converter has the ADKEY function for A/D conversion of “L” level analog input to ADKEY pin automatically.

[A/D Conversion Register (AD)] 0035_{16}

The A/D conversion register is a read-only register that contains the result of an A/D conversion. When reading this register during an A/D conversion, the previous conversion result is read.
After power on or system is released from reset, the value is undefined.

[A/D Control Register (ADCON)] 0034_{16}

The A/D control register controls the A/D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A/D conversion. The value of this bit remains at “0” during an A/D conversion, then changes to “1” when the A/D conversion is completed. Writing “0” to this bit starts the A/D conversion. Bit 4 enables the ADKEY function. Writing “1” to this bit enables the ADKEY function. When this function is set to be valid, the analog input pin selection bits are invalid. Also, when the bit 4 is “1”, do not write “0” to bit 3 by program.

Resistor ladder

The resistor ladder divides the voltage between V_{CC} and V_{SS} by 256, and outputs the comparison voltages to the comparator.

Channel Selector

The channel selector selects one of the input ports AN_7–AN_0.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A/D conversion register. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to “1”.
The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough.
Accordingly, set $f(X_{IN})$ to at least 500kHz during A/D conversion in the middle- or high-speed mode.
Also, do not execute the STP and WIT instructions during the A/D conversion.
In the low-speed mode, since the A/D conversion is executed by the built-in self-oscillation circuit, the minimum value of $f(X_{IN})$ frequency is not limited.

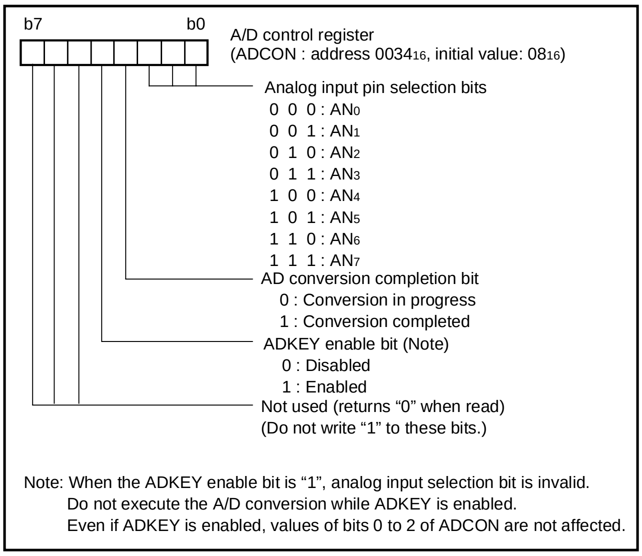


Fig. 25 Structure of A/D control register

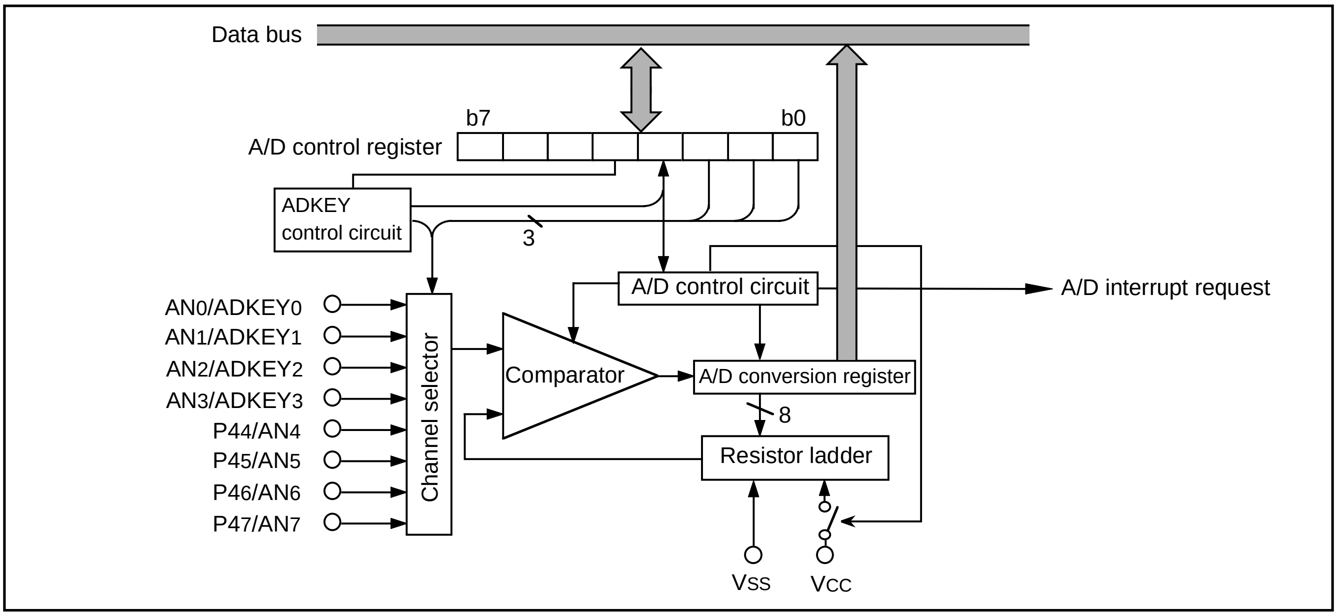


Fig. 26 A/D converter block diagram

ADKEY Control Circuit

The ADKEY function is the function for A/D conversion of the “L” level analog input voltage input to the ADKEY pin automatically. This function can be used also in the state of STP and WIT.

• ADKEY Selection

Two or more ADKEY pins can be selected by the low-order 4 bits of P4 data register.
If “L” level input to an ADKEY pin is detected, other bits are set to “0” and only the corresponding ADKEY selection bit is set to “1”. As a result, the pin with “L” level input can be recognized.

• ADKEY Enable

The ADKEY function is enabled by writing “1” to the ADKEY enable bit. Surely, in order to enable ADKEY functin, set “1” to the ADKEY enable bit, after selecting the ADKEY pin.
ADKEY becomes disabled automatically after the A/D conversion end by the ADKEY function. When the ADKEY enable bit of the A/D control register is “1”, the analog input pin selection bits become invalid. Please do not write “0” in the AD conversion completion bit by the program during ADKEY enabled state.

[ADKEY Control Circuit]

The pins which performs A/D conversion is selected with the ranking of ADKEY0, ADKEY1, ADKEY2, and ADKEY3 when there is an “L” level input simultaneously to two or more valid ADKEY pins.
In order to obtain a more exact conversion result, by the A/D conversion with ADKEY, execute the following;
① set the input to the ADKEY pin into a steep falling waveform,
② stabilize the input voltage within 8 clock cycle (1 µs at $f(X_{IN})$ = 8MHz) after the input voltage is under V_{IL}, and
③ maintain the input voltage until the completion of the A/D conversion.

The threshold voltage with an actual ADKEY pin is the voltage between V_{IH}-V_{IL}.
In order not to make ADKEY operation perform superfluously in a noise etc., in the state of the waiting for an input, set the voltage of an ADKEY pin to V_{IH} ($0.9V_{CC}$) or more.
When the following operations are performed, the A/D conversion operation cannot be guaranteed.
• When the CPU mode register is operated during A/D conversion operation,
• When the AD conversion control register is operated during A/D conversion operation,
• When STP or WIT instructin is executed during A/D conversion operation,
• When the ADKEY pin selection bit is operated during A/D conversion operation at selecting ADKEY function, and
• Return operation by reset, STOP or WIT under A/D conversion operation at selecting ADKEY function is performed.

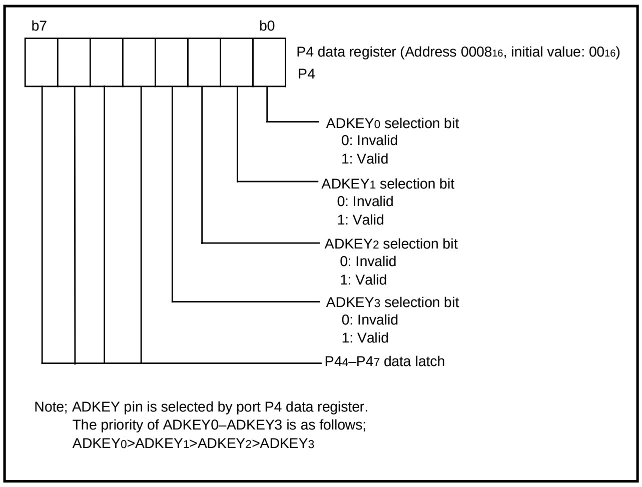


Fig. 27 Structure of ADKEY pin selection bits

Definition of A/D converter accuracy

The A/D conversion accuracy is defined below (refer to Figure 28).

• Relative accuracy

① Zero transition voltage (V_{0T})

This means an analog input voltage when the actual A/D conversion output data changes from "0" to "1."

② Full-scale transition voltage (V_{FST})

This means an analog input voltage when the actual A/D conversion output data changes from "255" to "254."

③ Linearity error

This means a deviation from the line between V_{0T} and V_{FST} of a converted value between V_{0T} and V_{FST}.

④ Differential non-linearity error

This means a deviation from the input potential difference required to change a converter value between V_{0T} and V_{FST} by 1 LSB at the relative accuracy.

• Absolute accuracy

This means a deviation from the ideal characteristics between 0 to V_{REF} (V_{CC} in 38C1 Group) of actual A/D conversion characteristics.

V_n: Analog input voltage when the output data changes from "n" to "n+1" (n = 0 to 254)

• 1LSB at relative accuracy → $\frac{V_{FST}-V_{0T}}{254}$ (V)

• 1LSB at absolute accuracy → $\frac{V_{REF}*}{256}$ (V)

* V_{REF} = V_{CC} in the 38C1 Group.

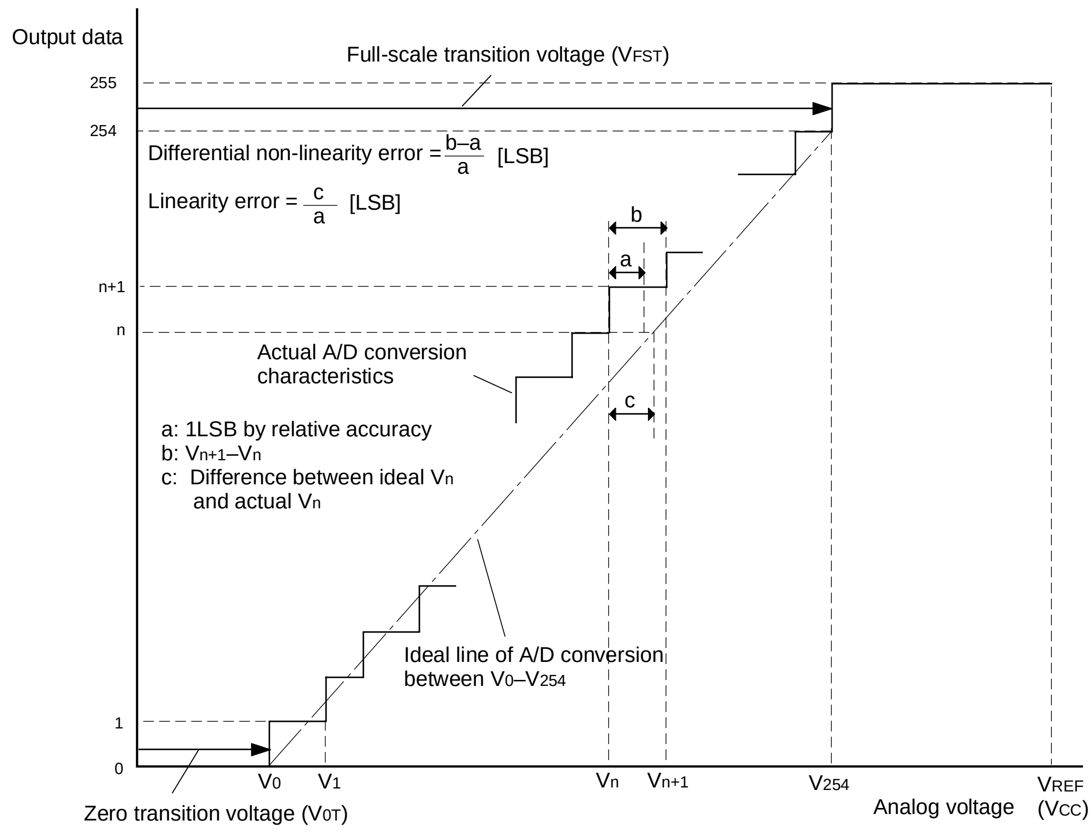


Fig. 28 Definition of A/D conversion accuracy

LCD DRIVE CONTROL CIRCUIT

The 38C1 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

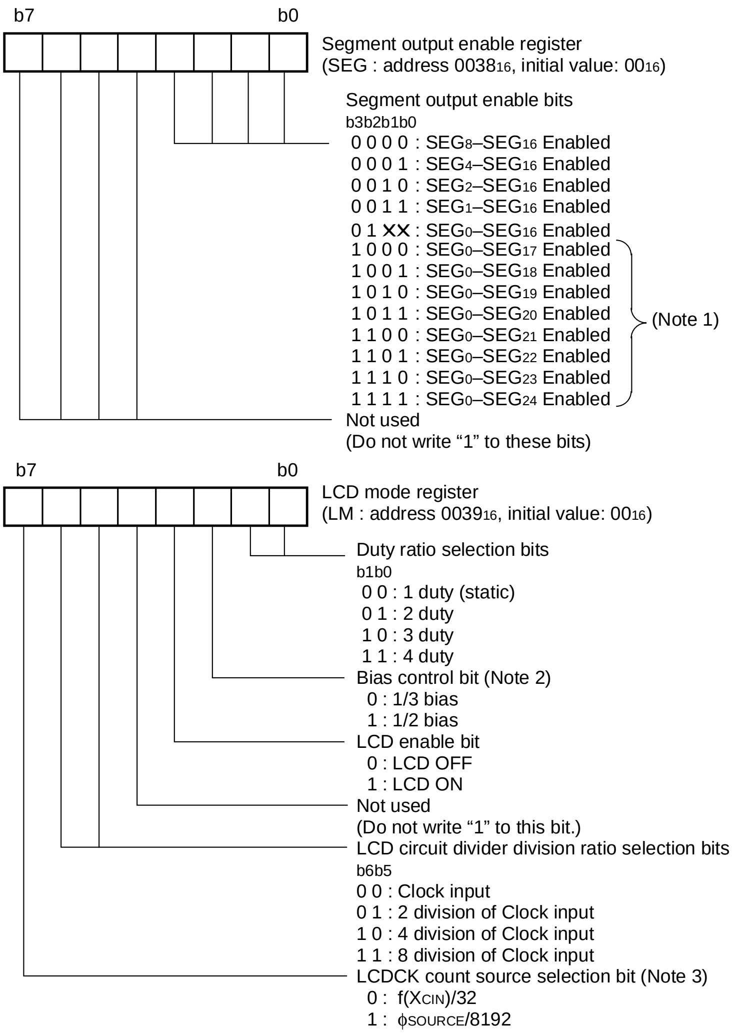
- LCD display register
- Segment output enable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 25 segment output pins and 4 common output pins can be used.

Up to 100 pixels can be controlled for LCD display. When the LCD enable bit is set to “1” after data is set in the LCD mode register, the segment output enable register and the LCD display register, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 7. Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
1	25 dots or 8 segment LCD 3 digits
2	50 dots or 8 segment LCD 6 digits
3	75 dots or 8 segment LCD 9 digits
4	100 dots or 8 segment LCD 12 digits



Notes 1: Set the direction register of the port which is also used as the segment output enabled pin to “1”.
2: When “1 duty” is selected by the duty ratio selection bit, set the bias control bit to “1”.
3: LCDCK is a clock for a LCD timing controller.
ϕ_{SOURCE} represents the oscillation frequency of X_{IN} input in the middle- and high-speed mode, on-chip oscillator in the on-chip oscillator mode, and sub-clock in the low-speed mode.

Fig. 29 Structure of segment output enable register and LCD mode register

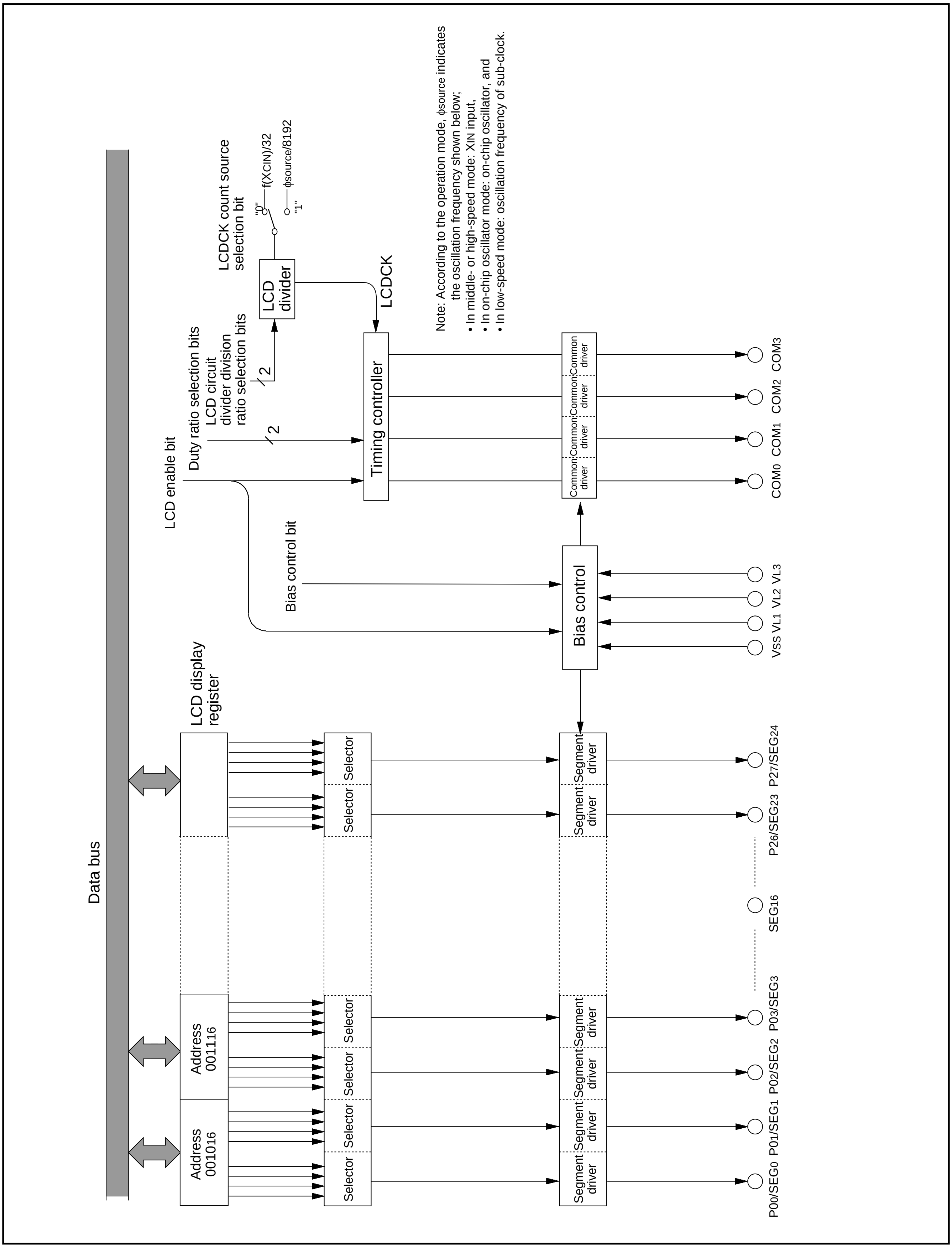


Fig. 30 Block diagram of LCD controller/driver

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage shown in Table 8 according to the bias value.
Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio.
Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).
When the LCD enable bit is “0”, the output of COM_0–COM_3 is “L” level.

Table 8. Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$
1/1 bias (static)	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{SS}$

Note : V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Table 9. Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits		Common pins used
	Bit 1	Bit 0	
1	0	0	COM_0 (Note 1)
2	0	1	COM_0, COM_1 (Note 2)
3	1	0	COM_0–COM_2 (Note 3)
4	1	1	COM_0–COM_3

Notes 1: Set COM_1, COM_2 and COM_3 to be open.
2: Set COM_2 and COM_3 to be open.
3: Set COM_3 to be open.

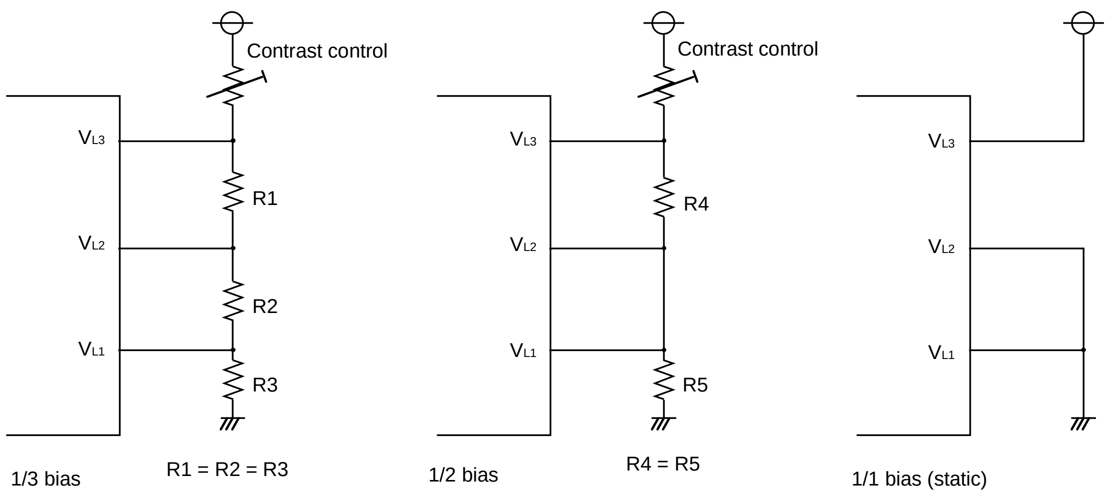


Fig. 31 Example of circuit at each bias

LCD Display register

Address 0010_{16} to $001C_{16}$ is the LCD display register. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK)=\frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency}=\frac{f(LCDCK)}{\text{duty ratio}}$$

Address \ Bits	7	6	5	4	3	2	1	0
0010_{16}	SEG_1				SEG_0			
0011_{16}	SEG_3				SEG_2			
0012_{16}	SEG_5				SEG_4			
0013_{16}	SEG_7				SEG_6			
0014_{16}	SEG_9				SEG_8			
0015_{16}	SEG_{11}				SEG_{10}			
0016_{16}	SEG_{13}				SEG_{12}			
0017_{16}	SEG_{15}				SEG_{14}			
0018_{16}	SEG_{17}				SEG_{16}			
0019_{16}	SEG_{19}				SEG_{18}			
$001A_{16}$	SEG_{21}				SEG_{20}			
$001B_{16}$	SEG_{23}				SEG_{22}			
$001C_{16}$	–				SEG_{24}			
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Fig. 32 LCD display register map

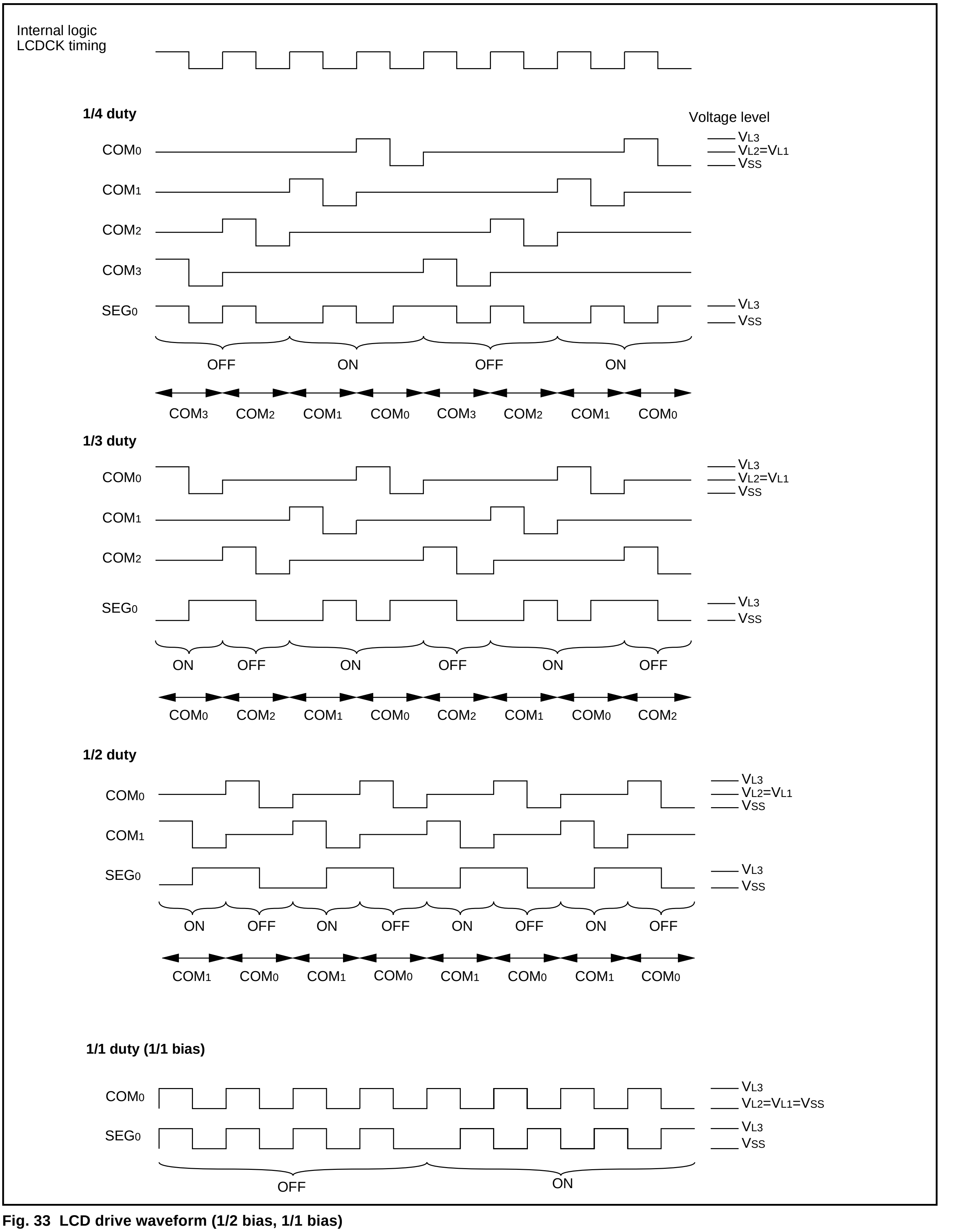


Fig. 33 LCD drive waveform (1/2 bias, 1/1 bias)

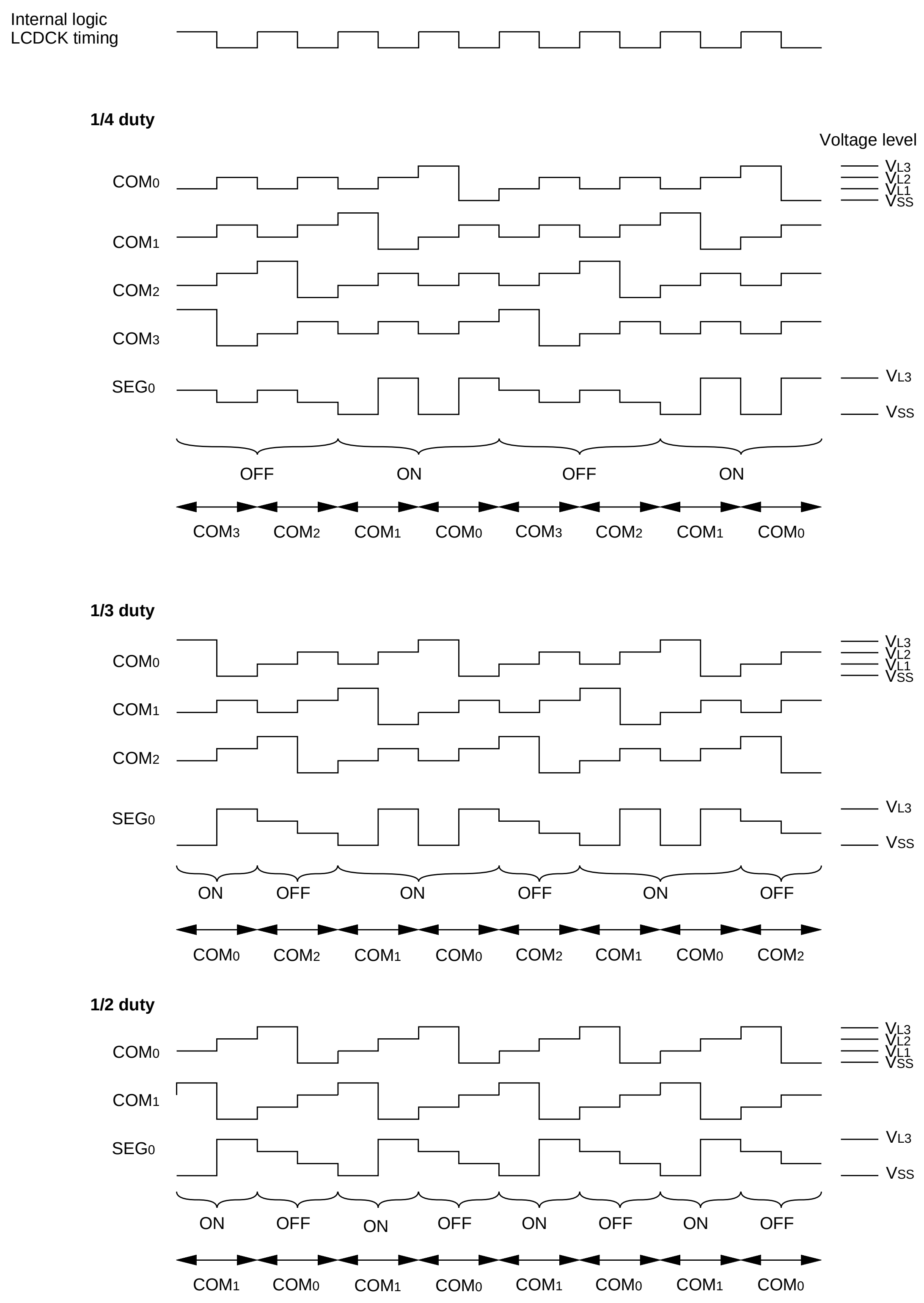


Fig. 34 LCD drive waveform (1/3 bias)

OTHER FUNCTION REGISTERS

● φ clock output function

The internal clock φ can be output from port $P6_3$ by setting the φ output control register.

At φ clock output, set “1” to the bit 3 of the port P6 direction register.

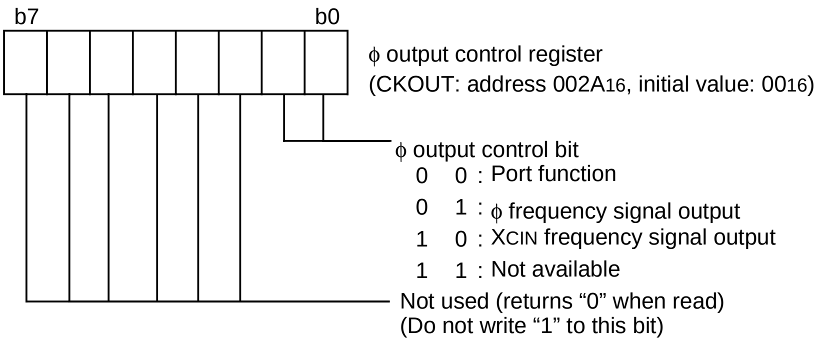


Fig. 35 Structure of clock output control register

● Temporary data register

The temporary data register (addresses $002C_{16}$ to $002E_{16}$) is the 8-bit register and does not have the control function. It can be used to store data temporarily. It is initialized after reset.

● RRF register

The RRF register (address $002F_{16}$) is the 8-bit register and does not have the control function.

As for the value written in this register, high-order 4 bits and low-order 4 bits interchange.

It is initialized after reset.

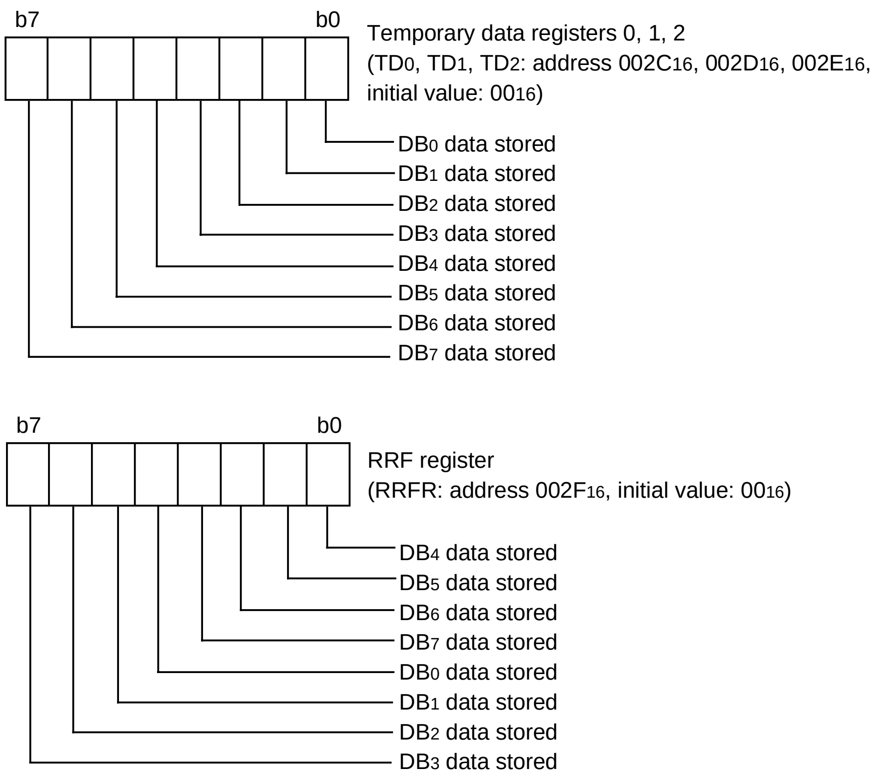


Fig. 36 Structure of temporary data register, RRF register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between V_{CC}(min.) and 5.5 V), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.2 V_{CC} for V_{CC} of V_{CC} (min.).

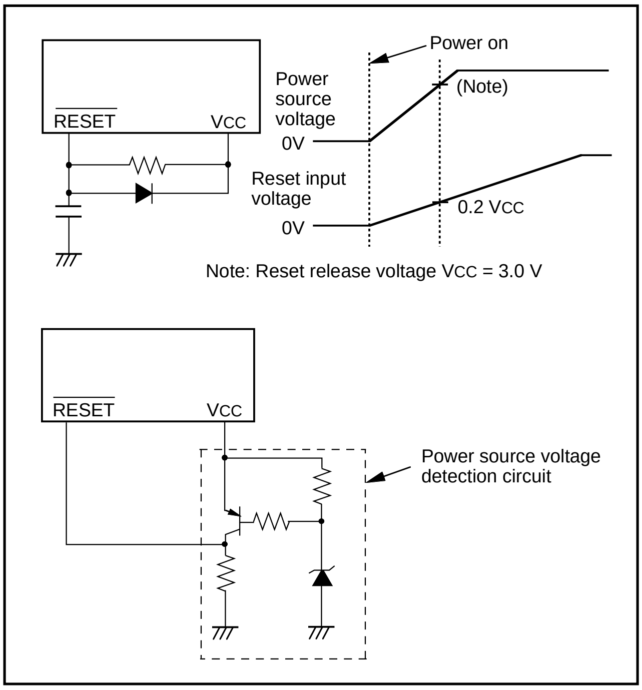


Fig. 37 Example of reset circuit

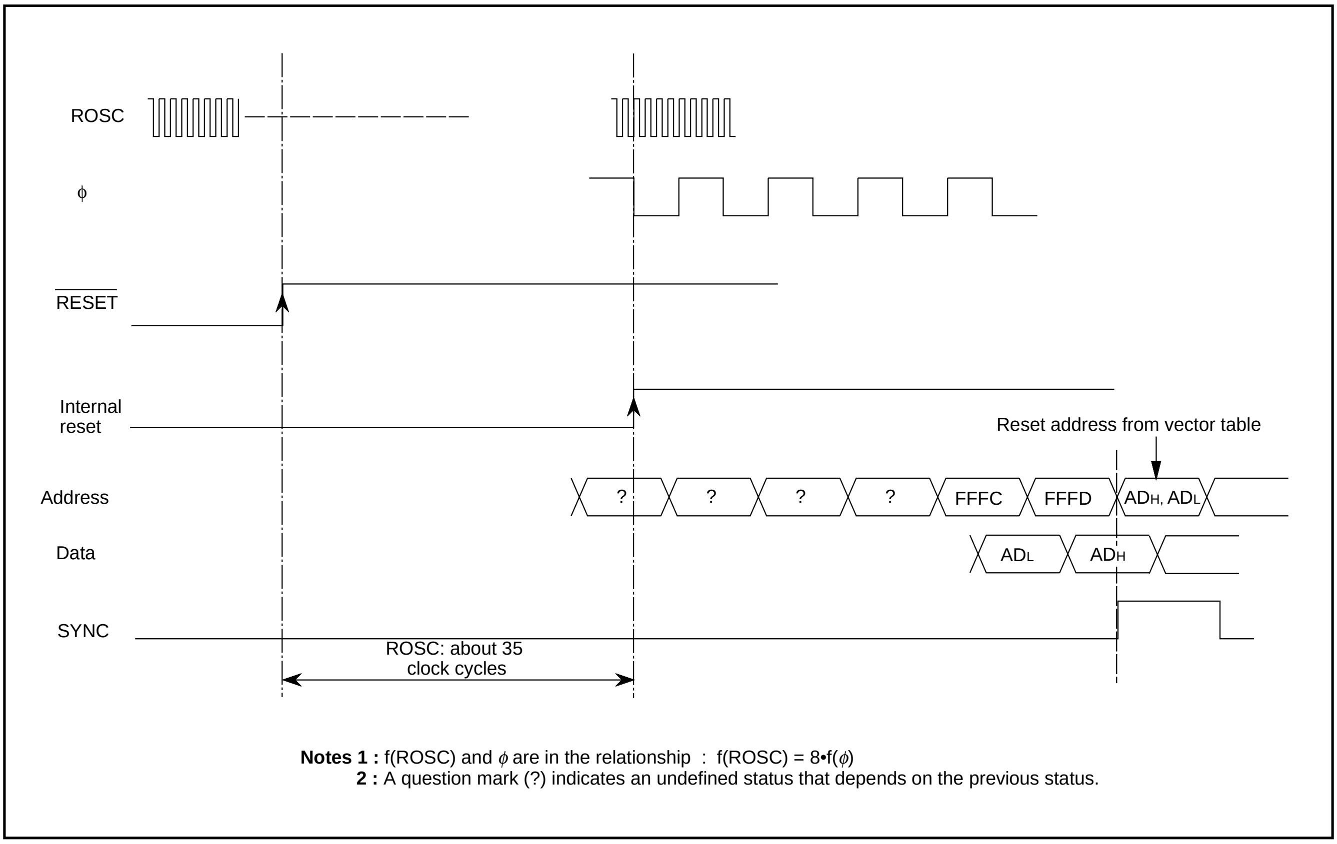


Fig. 38 Reset Sequence

		Address	Register contents
(1)	Port P2 direction register	0005_{16}	00_{16}
(2)	Port P3 direction register	0007_{16}	00_{16}
(3)	Port P4 direction register	0009_{16}	00_{16}
(4)	Port P5 direction register	$000B_{16}$	00_{16}
(5)	Port P6 direction register	$000D_{16}$	00_{16}
(6)	Serial I/O control register	$001D_{16}$	00_{16}
(7)	Timer X (low)	0020_{16}	FF_{16}
(8)	Timer X (high)	0021_{16}	FF_{16}
(9)	Timer Y (low)	0022_{16}	FF_{16}
(10)	Timer Y (high)	0023_{16}	FF_{16}
(11)	Timer 1	0024_{16}	10_{16}
(12)	Timer 2	0025_{16}	FF_{16}
(13)	Timer 3	0026_{16}	FF_{16}
(14)	Timer X mode register	0027_{16}	00_{16}
(15)	Timer Y mode register	0028_{16}	00_{16}
(16)	Timer 123 mode register	0029_{16}	00_{16}
(17)	ϕ output control register	$002A_{16}$	00_{16}
(18)	Temporary data register 0	$002C_{16}$	00_{16}
(19)	Temporary data register 1	$002D_{16}$	00_{16}
(20)	Temporary data register 2	$002E_{16}$	00_{16}
(21)	RRF register	$002F_{16}$	00_{16}
(22)	PULL register	0033_{16}	07_{16}
(23)	A/D control register	0034_{16}	08_{16}
(24)	Segment output enable register	0038_{16}	00_{16}
(25)	LCD mode register	0039_{16}	00_{16}
(26)	Interrupt edge selection register	$003A_{16}$	00_{16}
(27)	CPU mode register	$003B_{16}$	68_{16}
(28)	Interrupt request register 1	$003C_{16}$	00_{16}
(29)	Interrupt request register 2	$003D_{16}$	00_{16}
(30)	Interrupt control register 1	$003E_{16}$	00_{16}
(31)	Interrupt control register 2	$003F_{16}$	00_{16}
(32)	Processor status register	(PS)	X X X X X 1 X X
(33)	Program counter	(PC_H)	Contents of address $FFFD_{16}$
		(PC_L)	Contents of address $FFFC_{16}$

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.

X : Undefined

Fig. 39 Internal state of microcomputer immediately after reset

CLOCK GENERATING CIRCUIT

The oscillation circuit of 38C1 group can be formed by connecting an oscillator, capacitor and resistor between XIN and XOUT (XCIN and XCOUT). To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The clocks that are externally generated cannot be directly input to XCIN. Use the circuit constants in accordance with the oscillator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, a 10 MΩ external feed-back resistor is needed between XCIN and XCOUT.
Immediately after reset is released, only the on-chip oscillator starts oscillating, XIN -XOUT oscillation stops oscillating, and XCIN and XCOUT pins function as I/O ports.

Operation mode
(1) On-chip oscillator mode

The internal clock φ is the on-chip oscillator oscillation divided by 8.

(2) Middle-speed mode

The internal clock φ is the frequency of XIN divided by 8.

(3) High-speed mode

The internal clock φ is half the frequency of XIN.

(4) Low-speed mode

The internal clock φ is half the frequency of XCIN.

After reset release and when system returns from the stop mode, the on-chip oscillator mode is selected.
Refer to the clock state transition diagram for the setting of transition to each mode.
The XIN–XOUT oscillation is controlled by the bit 5 of CPUM, and the sub-clock oscillation is controlled by the bit 4 of CPUM. When the mode is switched to the on-chip oscillator mode, set the bit 3 of CPUM to "1".
In the on-chip oscillator mode, the oscillation by the oscillator can be stopped. In the low-speed mode, the power consumption can be reduced by stopping the XIN–XOUT oscillation.
When the mode is switched from the on-chip oscillator mode to the low-speed mode, the on-chip oscillator is stopped.
Set enough time for oscillation to stabilize by programming to restart the stopped oscillation and switch the operation mode. Also, set enough time for oscillation to stabilize by programming to switch the timer count source .

Note: If you switch the mode between on-chip oscillator mode, middle/high-speed mode and low-speed mode, stabilize both XIN and XCIN oscillations. Especially be careful immediately after power-on and at returning from stop mode. Refer to the clock state transition diagram for the setting of transition to each mode. Set the frequency in the condition that f(XIN) > 3•f(XCIN).
When the middle- and high-speed mode are not used (XIN-XOUT oscillation and external clock input are not performed), connect XIN to VCC through a resistor.

Oscillation Control
(1) Stop mode

Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. If the STP instruction is executed, the internal clock φ stops at an "H" level, and main clock, on-chip oscillator and sub-clock oscillators stop.
In this time, "10_{16}" is set to timer 1 and the on-chip oscillator is connected forcibly for the system clock and the timer 1 count source. Also, the bits of the timer 123 mode register except bit 4 are cleared to "0".
When an external interrupt is received, the clock oscillated before stop mode and the on-chip oscillator start oscillating.
However, bit 3 of CPUM is set to "1" forcibly and system returns to the on-chip oscillator mode.
Tthe internal clock φ is supplied to the CPU after timer 1 underflows. However, when the system clock is switched from the on-chip oscillator to main clock and sub-clock, generate the wait time enough for oscillation stabilizing by program.

(2) Wait mode

If the WIT instruction is executed, only the internal clock φ stops at an "H" level. The states of main clock, on-chip oscillator and sub-clock are the same as the state before the executing the WIT instruction and the oscillation does not stop. Since the internal clock φ restarts when an interrupt is received, the instruction is executed immediately.

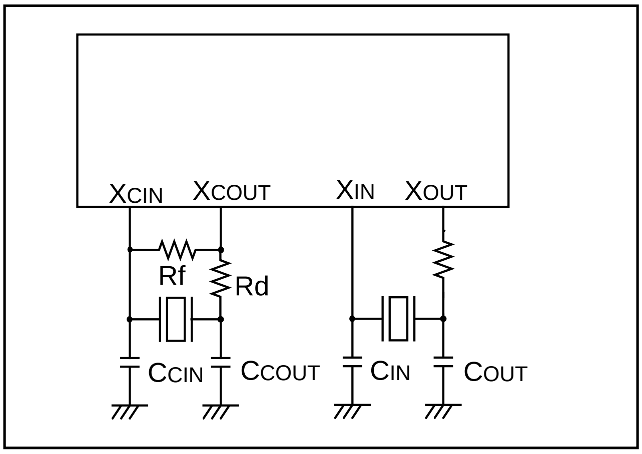


Fig. 40 Oscillator circuit example

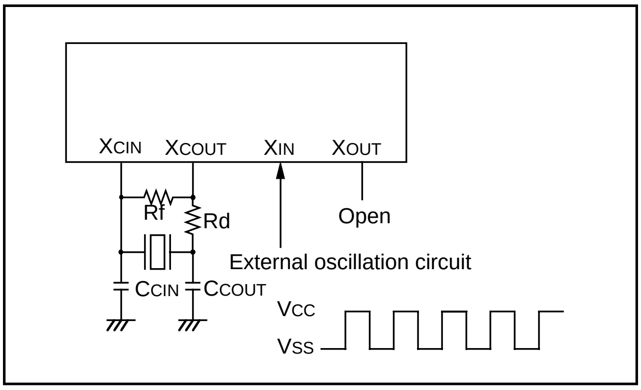
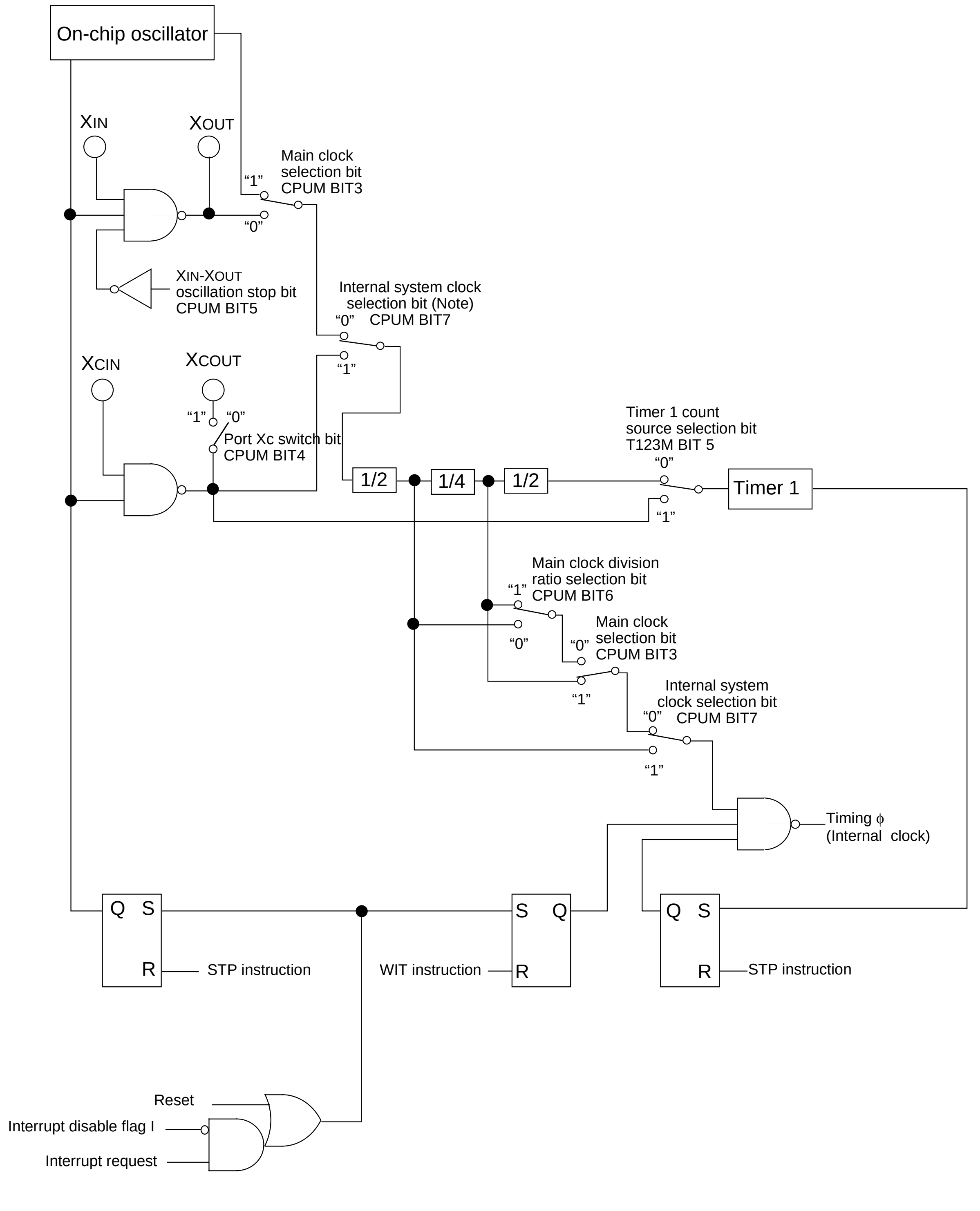
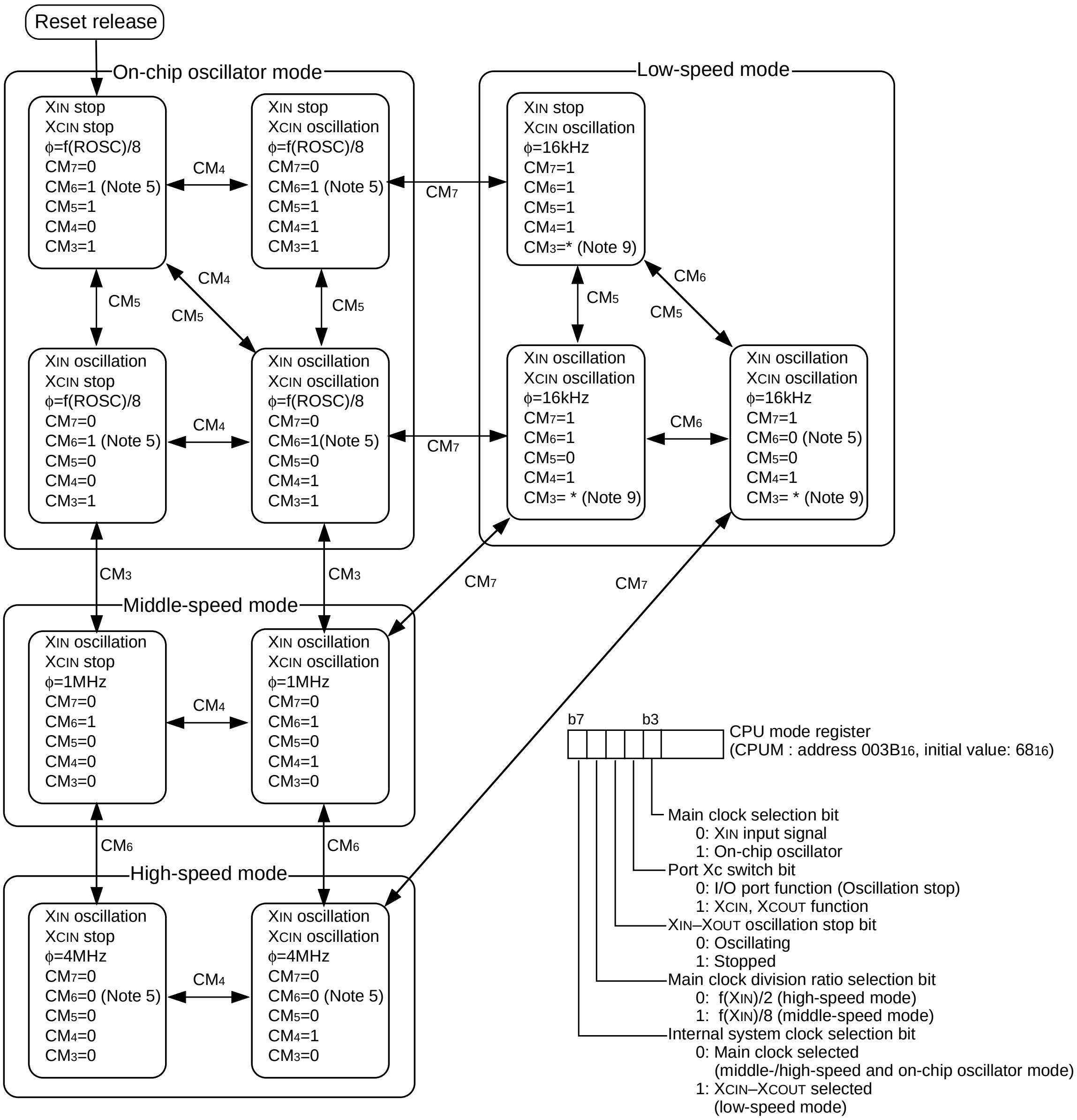


Fig. 41 External clock input circuit



Note: When Xc oscillation is selected for internal system clock, set the port Xc switch bit to "1".

Fig. 42 Clock generating circuit block diagram



Notes 1: Switch the mode by the arrows shown between the mode blocks.
The all modes can be switched to the stop mode or the wait mode.

2: Timer and LCD operate in the wait mode. System is returned to the source mode when the wait mode is ended.

3: CM4, CM5 and CM6 are retained in the stop mode. System is returned to the on-chip oscillator mode (CM3=1, CM7=0).

4: When the stop mode is ended, set the oscillation stabilizing wait time in the on-chip oscillator mode.

5: When the stop mode is ended, set the initial value to CM6 (CM6=1).

6: Execute the transition after the oscillation used in the destination mode is stabilized.

7: When system goes to on-chip oscillator mode, the oscillation stabilizing wait time is not needed.

8: Do not go to the high-speed mode from the on-chip oscillator mode.

9: Write the proper values for destination mode beforehand.

10: The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin.
f(ROSC) indicates the oscillation frequency of on-chip oscillator.

Fig. 43 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n + 1).

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to “1”.
In serial I/O, the SOUT pin goes to high impedance state after transmission is completed.

A/D Converter

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough.
Accordingly, set f(XIN) to at least 500kHz during A/D conversion in the middle- or high-speed mode.
Also, do not execute the STP or WIT instruction during an A/D conversion.
In the low-speed mode, since the A/D conversion is executed by the built-in self-oscillation circuit, the minimum value of f(XIN) frequency is not limited.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the XIN frequency.

NOTES ON USE

VL3 pin

When LCD drive control circuit is not used, connect VL3 to VCC.

Countermeasures against noise

(1) Shortest wiring length

① Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the Vss pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the RESET pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the RESET pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

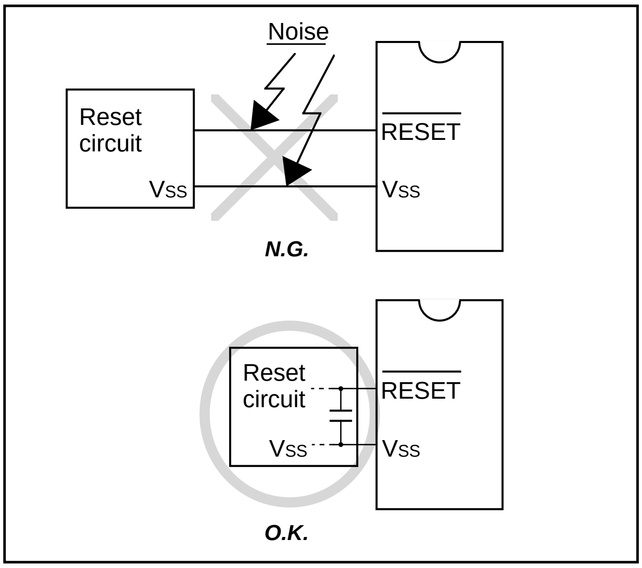


Fig. 44 Wiring for the RESET pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

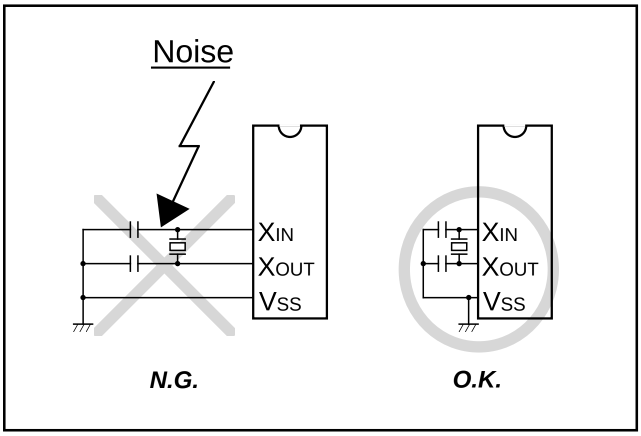


Fig. 45 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 µF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

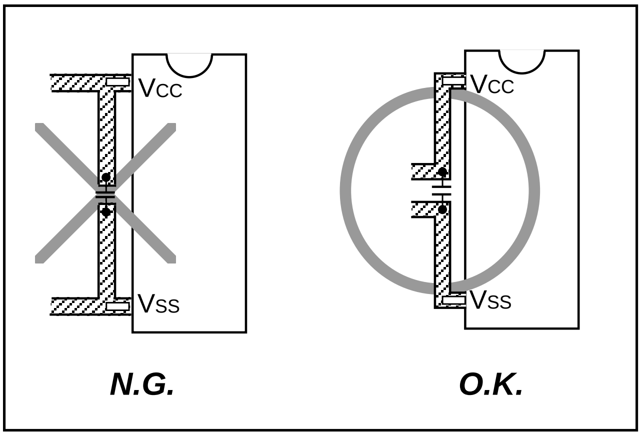


Fig. 46 Bypass capacitor across the Vss line and the Vcc line

(3) Oscillator concerns
In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of voltage or/and temperature is wide.
Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines
Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason
In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently
Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason
Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

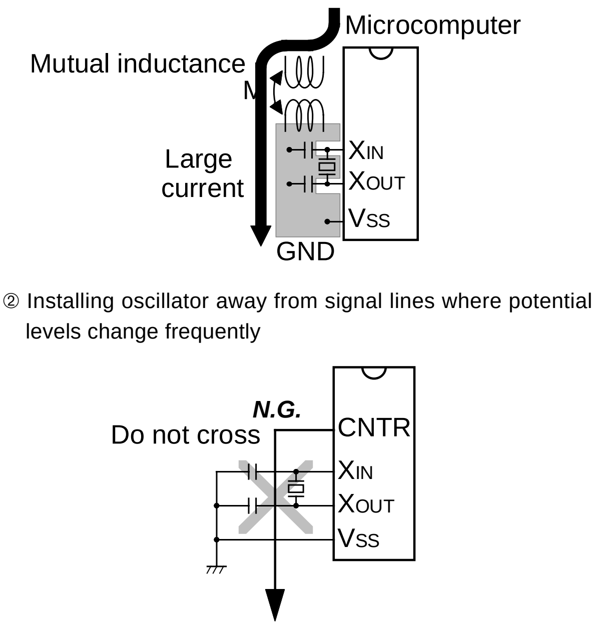


Fig. 47 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input
The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory type and size
When Mask ROM and PROM version and memory size differ in one group, actual values such as an electrical characteristics, A/D conversion accuracy, and the amount of -proof of noise incorrect operation may differ from the ideal values.
When these products are used switching, perform system evaluation for each product of every after confirming product specification.

(6) Wiring to VPP pin of One Time PROM version
Connect an approximately 5 kΩ resistor to the VPP pin the shortest possible in series and also to the VSS pin.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason
The VPP pin of the One Time PROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for writing flow into the built-in PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

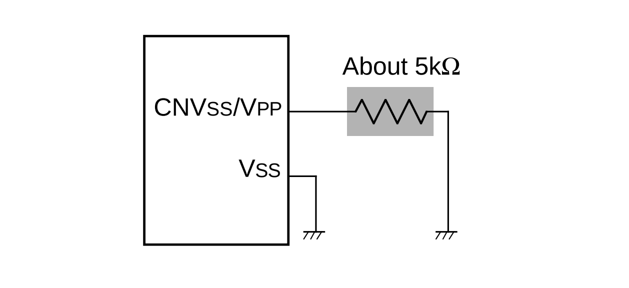


Fig. 48 Wiring for the VPP pin of One Time PROM

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form✻
2. Mark Specification Form✻
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk

✻For the mask ROM confirmation and the mark specifications, refer to the "Renesas Technology" Homepage (http://www.renesas.com/en/rom/).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version (M38C13E6FP/HP) can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 10. Programming adapter

Package	Name of Programming Adapter
M38C13E6FP	PCA7438F-64A
M38C13E6HP	PCA7438H-64A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 49 is recommended to verify programming.

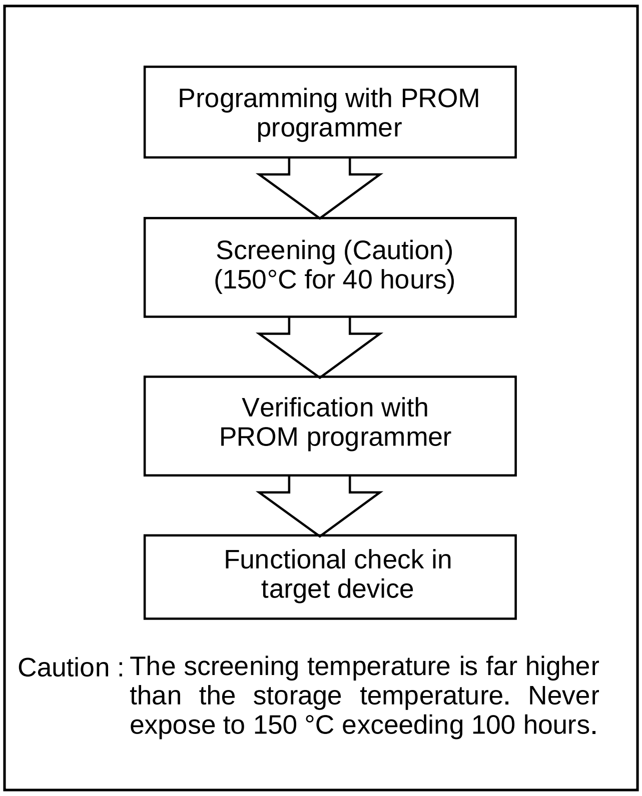


Fig. 49 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 11 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on Vss. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage P0₀–P0₇, P2₀–P2₇, P3₀–P3₄, P4₄–P4₇, P5₀–P5₇, P6₀–P6₄		–0.3 to V_{CC}+0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 6.5	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC}+0.3	V
V_I	Input voltage AN_0–AN_3		–0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS} (Mask ROM version)		–0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS} (One Time PROM version)		–0.3 to 13	V
V_O	Output voltage $P2_0$–$P2_7$	At output port	–0.3 to V_{CC}+0.3	V
		At segment output	–0.3 to V_{L3}+0.3	V
V_O	Output voltage $P3_0$–$P3_4$, $P4_4$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_4$		–0.3 to V_{CC}+0.3	V
V_O	Output voltage SEG_0–SEG_{24}		–0.3 to V_{L3}+0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Recommended Operating Conditions

Table 12 Recommended operating conditions

(Vcc = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter				Limits Min.	Typ.	Max.	Unit
V_{CC}	Power source voltage (**Note 1**)		High-speed mode	$f(X_{IN}) \leq 8$ MHz	4.0	5.0	5.5	V
				$f(X_{IN}) \leq 6$ MHz	3.0	5.0	5.5	V
		Mask ROM version	High-speed mode	$f(X_{IN}) \leq 4$ MHz	2.0	5.0	5.5	V
			Middle-speed mode	$f(X_{IN}) \leq 8$ MHz	2.0	5.0	5.5	V
				$f(X_{IN}) \leq 6$ MHz	1.8	5.0	5.5	V
			Low-speed, on-chip oscillator operation mode		1.8	5.0	5.5	V
		One Time PROM version	High-speed mode	$f(X_{IN}) \leq 4$ MHz	2.5	5.0	5.5	V
			Middle-speed mode	$f(X_{IN}) \leq 8$ MHz	2.5	5.0	5.5	V
				$f(X_{IN}) \leq 6$ MHz	2.2	5.0	5.5	V
			Low-speed, on-chip oscillator operation mode		2.2	5.0	5.5	V
		When oscillation starts (**Note 2**)	Mask ROM version		2.2	5.0	5.5	V
			One Time PROM version		2.5	5.0	5.5	V
V_{SS}	Power source voltage					0		V
CNV_{SS}						0	$0.2V_{CC}$	V
VL3	LCD power source voltage				2.5			V
V_{IA}	Analog input voltage	AN_0–AN_7			V_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P4_4$–$P4_7$, $P5_5$, $P5_7$, $P6_2$–$P6_4$			$0.7V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$P6_0$, $P6_1$ (CM_4=0)			$0.7V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$P3_0$–$P3_4$, $P5_0$–$P5_4$, $P5_6$			$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$			$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}			$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P4_4$–$P4_7$, $P5_5$, $P5_7$, $P6_2$–$P6_4$			0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage	$P6_0$, $P6_1$ (CM_4=0)			0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage	$P3_0$–$P3_4$, $P5_0$–$P5_4$, $P5_6$			0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	$\overline{RESET}$			0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	X_{IN}			0		$0.2V_{CC}$	V

Notes 1: When the A/D converter is used, refer to the recommended operating condition for A/D conversion.
2: Oscillation start voltage and oscillation start time depend on the oscillator, the circuit constant and temperature.
Especially, be careful that an oscillation start of the high-frequency oscillator may be difficult at low-voltage.
Until the oscillation is stabilized, wait in the on-chip oscillator mode.

Table 13 Recommended operating conditions

(Vcc = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current **(Note 1)** P20–P27, P30–P34			–40	mA
ΣIOH(peak)	"H" total peak output current **(Note 1)** P44–P47, P50–P57, P60–P64			–60	mA
ΣIOL(peak)	"L" total peak output current **(Note 1)** P20–P27, P30–P34			80	mA
ΣIOL(peak)	"L" total peak output current **(Note 1)** P44–P47, P50–P57, P60–P64			60	mA
ΣIOH(avg)	"H" total average output current **(Note 1)** P20–P27, P30–P34			–20	mA
ΣIOH(avg)	"H" total average output current **(Note 1)** P44–P47, P50–P57, P60–P64			–30	mA
ΣIOL(avg)	"L" total average output current **(Note 1)** P20–P27, P30–P34			40	mA
ΣIOL(avg)	"L" total average output current **(Note 1)** P44–P47, P50–P57, P60–P64			30	mA
IOH(peak)	"H" peak output current **(Note 2)** P20–P27			–2	mA
IOH(peak)	"H" peak output current **(Note 2)** P30–P34			–5	mA
IOH(peak)	"H" peak output current **(Note 2)** P44–P47, P50–P57, P60–P64			–5	mA
IOL(peak)	"L" peak output current **(Note 2)** P20–P27			5	mA
IOL(peak)	"L" peak output current **(Note 2)** P30–P34			30	mA
IOL(peak)	"L" peak output current **(Note 2)** P44–P47, P50–P57, P60–P64			10	mA
IOH(avg)	"H" average output current **(Note 3)** P20–P27			–1.0	mA
IOH(avg)	"H" average output current **(Note 3)** P30–P34			–2.5	mA
IOH(avg)	"H" average output current **(Note 3)** P44–P47, P50–P57, P60–P64			–2.5	mA
IOL(avg)	"L" average output current **(Note 3)** P20–P27			2.5	mA
IOL(avg)	"L" average output current **(Note 3)** P30–P34			15	mA
IOL(avg)	"L" average output current **(Note 3)** P44–P47, P50–P57, P60–P64			5	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is average value measured over 100 ms.

Table 14 Recommended operating conditions

(Vcc = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Timer X and Timer Y Input frequency (duty cycle 50%)	(4.0 V ≤ VCC ≤ 5.5 V)			4.0	MHz
		(Mask ROM version: 2.0V ≤ VCC ≤ 4.0 V) (One Time PROM version: 3.0 V ≤ VCC ≤ 4.0 V)			VCC	MHz MHz
		(Mask ROM version: VCC ≤ 2.0 V)			5×VCC–8	MHz
		(One Time PROM version: 2.5 V ≤ VCC ≤ 3.0 V)			2×VCC–3	MHz
		(One Time PROM version: VCC ≤ 2.5 V)			$\frac{10\times V_{CC}-19}{3}$	MHz
f(XIN)	Main clock input frequency (duty cycle 50%) (**Note 1**)	High-speed mode (4.0 V < VCC ≤ 5.5 V)			8.0	MHz
		High-speed mode (Mask ROM version: 2.0V ≤ VCC ≤ 4.0 V) (One Time PROM version: 3.0 V ≤ VCC ≤ 4.0 V)			2×VCC	MHz
		High-speed mode (One Time PROM version: 2.5 V ≤ VCC ≤ 3.0 V)			4×VCC–6	MHz
		Middle-speed mode (**Note 3**) (**Note 4**) (Mask ROM version: 2.0 V ≤ VCC ≤ 5.5 V) (One Time PROM version: 2.5 V ≤ VCC ≤ 5.5 V)			8.0	MHz
		Middle-speed mode (**Note 3**) (**Note 4**)			6.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (**Note 2**) (**Note 4**) (duty cycle 50%)			32.768	80	kHz

Notes 1: When the A/D converter is used, refer to the recommended operating condition for A/D conversion.
2: When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.
3: When the timer X count source selection bit is set to “1”, as for the recommended operating condition of the main clock input frequency f(XIN), the rating value at the high-speed mode is applied.
4: Oscillation start voltage and oscillation start time depend on the oscillator, the circuit constant and temperature.
Especially, be careful that an oscillation start of the high-frequency oscillator may be difficult at low-voltage.
Until the oscillation is stabilized, wait in the on-chip oscillator mode.

Electrical Characteristics

Table 15 Electrical characteristics

(Vcc = 4.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	“H” output voltage P20–P27	I_{OH} = –1.0 mA	V_{CC}–2.0			V
		I_{OH} = –0.2 mA, V_{CC} = 1.8 to 5.5 V (Note)	V_{CC}–0.8			V
V_{OH}	“H” output voltage P30–P34, P44–P47, P50–P57, P60–P64	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.5 mA, V_{CC} = 1.8 to 5.5 V (Note)	V_{CC}–0.8			V
V_{OL}	“L” output voltage P20–P27	I_{OL} = 2.5 mA			2.0	V
		I_{OL} = 0.5 mA, V_{CC} = 1.8 to 5.5 V (Note)			0.8	V
V_{OL}	“L” output voltage P44–P47, P50–P57, P60–P64	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1 mA, V_{CC} = 1.8 to 5.5 V (Note)			0.8	V
V_{OL}	“L” output voltage P30–P34	I_{OL} = 15 mA			2.0	V
		I_{OL} = 3 mA, V_{CC} = 1.8 to 5.5 V (Note)			0.8	V
V_{T+}–V_{T-}	Hysteresis INT0, INT1, CNTR0, CNTR1, P30–P34			0.5		V
V_{T+}–V_{T-}	Hysteresis SCLK, SIN			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	“H” input current P30–P34, P44–P47, P50–P57, P60–P64	V_I = V_{CC}			5.0	µA
I_{IH}	“H” input current P00–P07, P20–P27	V_I = V_{SS}, Pull-down “OFF”			5.0	µA
		V_{CC} = 5.0 V, V_I = V_{CC}, Pull-down “ON”	60	120	240	µA
		V_{CC} = 3.0 V, V_I = V_{CC}, Pull-down “ON”	25	50	100	µA
I_{IH}	“H” input current $\overline{RESET}$, AN0–AN3	V_I = V_{CC}			5.0	µA
I_{IH}	“H” input current XIN	V_I = V_{CC}		4.0		µA
I_{IL}	“L” input current P00–P07, P20–P27	V_I = V_{SS}			–5.0	µA
I_{IL}	“L” input current P30–P34, P44–P47, P50–P57, P60–P64	V_I = V_{SS}, Pull-up “OFF”			–5.0	µA
		V_{CC} = 5.0 V, V_I = V_{SS}, Pull-up “ON”	–60	–120	–240	µA
		V_{CC} = 3.0 V, V_I = V_{SS}, Pull-up “ON”	–25	–50	–100	µA
I_{IL}	“L” input current $\overline{RESET}$, CNVSS, AN0–AN3	V_I = V_{SS}			–5.0	µA
I_{IL}	“L” input current XIN	V_I = V_{SS}		–4.0		µA
V_{RAM}	RAM hold voltage (Mask ROM version)	At clock stop	1.8		5.5	V
	RAM hold voltage (One Time PROM version)	At clock stop	2.2		5.5	V
R_{OSC}	On-chip oscillator oscillation frequency	V_{CC} = 5.0 V, Ta = 25 °C	2500	5000	7500	kHz

Note: One Time PROM version: 2.2 to 5.5 V.

Table 16 Electrical characteristics

(V_{CC} = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = –20 to 85°C, f(X_{CIN}) = 32.768 kHz, output transistors “OFF”, AD converter stopped, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	Power source current	High-speed mode	V_{CC} = 5 V Mask ROM version	f(X_{IN}) = 8 MHz		3.0	6.0	mA
				f(X_{IN}) = 8 MHz (in WIT state)		0.8	1.6	mA
				f(X_{IN}) = 4 MHz		1.5	3.0	mA
			V_{CC} = 5 V One Time PROM version	f(X_{IN}) = 8 MHz		4.7	9.4	mA
				f(X_{IN}) = 8 MHz (in WIT state)		0.9	1.8	mA
				f(X_{IN}) = 4 MHz		2.5	5.0	mA
			V_{CC} = 2.5 V Mask ROM version	f(X_{IN}) = 4 MHz		0.6	1.2	mA
				f(X_{IN}) = 4 MHz (in WIT state)		0.3	0.6	mA
				f(X_{IN}) = 2 MHz		0.4	0.8	mA
			V_{CC} = 2.5 V One Time PROM version	f(X_{IN}) = 4 MHz		0.9	1.8	mA
				f(X_{IN}) = 4 MHz (in WIT state)		0.3	0.6	mA
				f(X_{IN}) = 2 MHz		0.6	1.2	mA
		Middle-speed mode	V_{CC} = 5 V Mask ROM version	f(X_{IN}) = 8 MHz		1.2	2.4	mA
				f(X_{IN}) = 8 MHz (in WIT state)		0.8	1.6	mA
				f(X_{IN}) = 4 MHz		0.8	1.6	mA
			V_{CC} = 5 V One Time PROM version	f(X_{IN}) = 8 MHz		1.8	3.6	mA
				f(X_{IN}) = 8 MHz (in WIT state)		0.9	1.8	mA
				f(X_{IN}) = 4 MHz		1.0	2.0	mA
			V_{CC} = 2.5 V Mask ROM version	f(X_{IN}) = 8 MHz		0.5	1.0	mA
				f(X_{IN}) = 8 MHz (in WIT state)		0.3	0.6	mA
				f(X_{IN}) = 4 MHz		0.3	0.6	mA
			V_{CC} = 2.5 V One Time PROM version	f(X_{IN}) = 8 MHz		0.7	1.4	mA
				f(X_{IN}) = 8 MHz (in WIT state)		0.4	0.8	mA
				f(X_{IN}) = 4 MHz		0.4	0.8	mA
		Low-speed mode	V_{CC} = 5 V Mask ROM version	f(X_{IN}) = stop		13	26	µA
				WIT instruction executed		5.5	11	µA
			V_{CC} = 5 V One Time PROM version	f(X_{IN}) = stop		19	38	µA
				WIT instruction executed		6.5	13	µA
			V_{CC} = 2.5 V Mask ROM version	f(X_{IN}) = stop		7.0	14	µA
				WIT instruction executed		3.5	7.0	µA
			V_{CC} = 2.5 V One Time PROM version	f(X_{IN}) = stop		10	20	µA
				WIT instruction executed		3.5	7	µA
		On-chip oscillator mode f(X_{CIN}) = stop		V_{CC} = 5 V		600	1200	µA
				V_{CC} = 2.5 V		90	270	µA
				V_{CC} = 2.5 V (in WIT state)		30	90	µA
		All oscillations stop (STP instruction executed)		Ta = 25 °C		0.1	1.0	µA
				Ta = 85 °C			10	µA
		Current increased when AD converter is operating		f(X_{IN}) = 8 MHz, V_{CC} = 5 V at middle-, high-speed mode		0.5		mA
				f(X_{IN}) = stop, V_{CC} = 5 V at on-chip oscillator operation mode		0.5		mA
				f(X_{IN}) = stop, V_{CC} = 5 V at low-speed mode		0.4		mA

A/D Converter Characteristics

Table 17 A/D converter recommended operating condition

(V_{CC} = 2.0 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{DD}	Power source voltage	Mask ROM version		2.0	5.0	5.5	V
		One Time PROM version		2.2	5.0	5.5	V
V_{IH}	"H" input voltage $ADKEY_0$–$ADKEY_3$			$0.9V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $ADKEY_0$–$ADKEY_3$			0		$0.7V_{CC} \times -0.5$	V
$f(X_{IN})$	AD converter control clock (low-speed mode and on-chip oscillator mode excluded)	Mask ROM version	$V_{CC} \le 2.2$ V			$20 \times V_{CC}-38$	MHz
			$2.2 < V_{CC} \le 2.5$ V			$\frac{20 \times V_{CC}-26}{3}$	
		One Time PROM version	$V_{CC} \le 2.5$ V			$\frac{40 \times V_{CC}-82}{3}$	MHz
			$2.5 < V_{CC} \le 2.7$ V			$10 \times V_{CC}-19$	
		Mask ROM version	$2.5 < V_{CC} \le 5.5$ V			8.0	MHz
		One Time PROM version	$2.7 < V_{CC} \le 5.5$ V				

Table 18 A/D converter characteristics

(V_{CC} = 2.0 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution				8	BIT
LIN	Linearity error	Ta = 25 °C, $2.5 \le V_{CC} \le 5.5$ V			±1	LSB
DIF	Differential non-linearity error	Ta = 25 °C, $2.5 \le V_{CC} \le 5.5$ V			±0.9	LSB
V0T	Zero transition voltage	V_{CC} = 5.12 V, Ta = 25 °C	0	20	50	mV
		V_{CC} = 2.56 V, Ta = 25 °C	0	10	25	mV
VFST	Full-scale transition voltage	V_{CC} = 5.12 V, Ta = 25 °C	5070	5100	5120	mV
		V_{CC} = 2.56 V, Ta = 25 °C	2535	2550	2560	mV
ABS	Absolute accuracy (quantification error excluded)	$2.2 < V_{CC} \le 5.5$ V ($2.7 < V_{CC} \le 5.5$ V for One Time PROM version), $f(X_{IN}) \le 8.0$ MHz, or low-speed or on-chip oscillator mode			±2	LSB
		$2.2 < V_{CC} \le 2.5$ V ($2.5 < V_{CC} \le 2.7$ V for One Time PROM version), $f(X_{IN}) \le 2.0$ MHz, or low-speed or on-chip oscillator mode			±2	LSB
		$2.2 \le V_{CC} < 2.3$ V for One Time PROM version Low-speed or on-chip oscillator mode excluded			±5	LSB
		Condition except above			±3	LSB
T_{conv}	Conversion time (**Note**)		106		109	$t_c(\phi AD)$
I_{IA}	Analog input current				±5	µA

Note: The operation clock is X_{IN} in the middle- or high-speed mode, or the on-chip oscillator in the other modes.
When the A/D conversion is executed in the middle- or high-speed mode, set $f(X_{IN}) \ge 500$ kHz.
$t_c(\phi AD)$: One cycle of control clock for A/D converter. X_{IN} input is used in the middel- or high-speed mode, and on-chip oscillator is used in the low- or on-chip oscillator mode for the control clock.

Timing Requirements And Switching Characteristics

Table 19 Timing requirements 1

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w}(\overline{RESET})$	Reset input “L” pulse width	2			µs
$t_{c}(X_{IN})$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH}(X_{IN})$	Main clock input “H” pulse width	50			ns
$t_{wL}(X_{IN})$	Main clock input “L” pulse width	50			ns
$t_{c}(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH}(INT)$	INT_0, INT_1 input “H” pulse width	80			ns
$t_{wL}(INT)$	INT_0, INT_1 input “L” pulse width	80			ns
$t_{c}(S_{CLK})$	Serial I/O clock input cycle time	1000			ns
$t_{wH}(S_{CLK})$	Serial I/O clock input “H” pulse width	400			ns
$t_{wL}(S_{CLK})$	Serial I/O clock input “L” pulse width	400			ns
$t_{su}(S_{IN}\text{-}S_{CLK})$	Serial I/O input setup time	200			ns
$t_{h}(S_{CLK}\text{-}S_{IN})$	Serial I/O input hold time	200			ns

Table 20 Timing requirements 2

(Vcc =1.8 to 4.0 V (2.2 to 4.0 V for One Time PROM version), Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{w}(\overline{RESET})$	Reset input “L” pulse width		2			µs
$t_{c}(X_{IN})$	Main clock input cycle time (X_{IN} input)	2.0 V (One Time PROM version: 2.5 V) ≤ V_{CC} ≤ 4.0 V	125			ns
		V_{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	166			ns
$t_{wH}(X_{IN})$	Main clock input “H” pulse width	2.0 V (One Time PROM version: 2.5 V) ≤ V_{CC} ≤ 4.0 V	50			ns
		V_{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	70			ns
$t_{wL}(X_{IN})$	Main clock input “L” pulse width	2.0 V (One Time PROM version: 2.5 V) ≤ V_{CC} ≤ 4.0 V	50			ns
		V_{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	70			ns
$t_{c}(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	2.0 V (One Time PROM version: 2.5 V) ≤ V_{CC} ≤ 4.0 V	$1000/V_{CC}$			ns
		V_{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	$1000/(5 \times V_{CC}-8)$			ns
$t_{wH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width		$t_{c}(CNTR)/2-20$			ns
$t_{wL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width		$t_{c}(CNTR)/2-20$			ns
$t_{wH}(INT)$	INT_0, INT_1 input “H” pulse width		230			ns
$t_{wL}(INT)$	INT_0, INT_1 input “L” pulse width		230			ns
$t_{c}(S_{CLK})$	Serial I/O clock input cycle time		2000			ns
$t_{wH}(S_{CLK})$	Serial I/O clock input “H” pulse width		950			ns
$t_{wL}(S_{CLK})$	Serial I/O clock input “L” pulse width		950			ns
$t_{su}(RxD\text{-}S_{CLK})$	Serial I/O input setup time		400			ns
$t_{h}(S_{CLK}\text{-}RxD)$	Serial I/O input hold time		200			ns

Table 21 Switching characteristics 1

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{WH}(SCLK)	Serial I/O clock output "H" pulse width	t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O clock output "L" pulse width	t_C(SCLK)/2–30			ns
t_d(SCLK-SOUT)	Serial I/O output delay time **(Note 1)**			140	ns
t_V(SCLK-SOUT)	Serial I/O output valid time **(Note 1)**	–30			ns
t_r(SCLK)	Serial I/O clock output rising time			30	ns
t_f(SCLK)	Serial I/O clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time P2~0~–P2~7~			200	ns
	CMOS output rising time P3~0~–P3~4~, P4~4~–P4~7~, P5~0~–P5~7~, P6~0~–P6~4~ **(Note 2)**		25	40	ns
t_f(CMOS)	CMOS output falling time **(Note 2)**		25	40	ns

Notes 1: When the P5~5~/SOUT P-channel output disable bit of the serial I/O control register (bit 4 of address 001D~16~) is "0."
2: The XOUT, XCOUT pins are excluded.

Table 22 Switching characteristics 2

(Vcc = 1.8 to 4.0 V (2.2 to 4.0 V for One Time PROM version), Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{WH}(SCLK)	Serial I/O clock output "H" pulse width	t_C(SCLK)/2–80			ns
t_{WL}(SCLK)	Serial I/O clock output "L" pulse width	t_C(SCLK)/2–80			ns
t_d(SCLK-SOUT)	Serial I/O output delay time **(Note 1)**			350	ns
t_V(SCLK-SOUT)	Serial I/O output valid time **(Note 1)**	–30			ns
t_r(SCLK)	Serial I/O clock output rising time			80	ns
t_f(SCLK)	Serial I/O clock output falling time			80	ns
t_r(CMOS)	CMOS output rising time P2~0~–P2~7~			400	ns
	CMOS output rising time P3~0~–P3~4~, P4~4~–P4~7~, P5~0~–P5~7~, P6~0~–P6~4~ **(Note 2)**		60	120	ns
t_f(CMOS)	CMOS output falling time **(Note 2)**		60	120	ns

Notes 1: When the P5~5~/SOUT P-channel output disable bit of the serial I/O control register (bit 4 of address 001D~16~) is "0."
2: The XOUT, XCOUT pins are excluded.

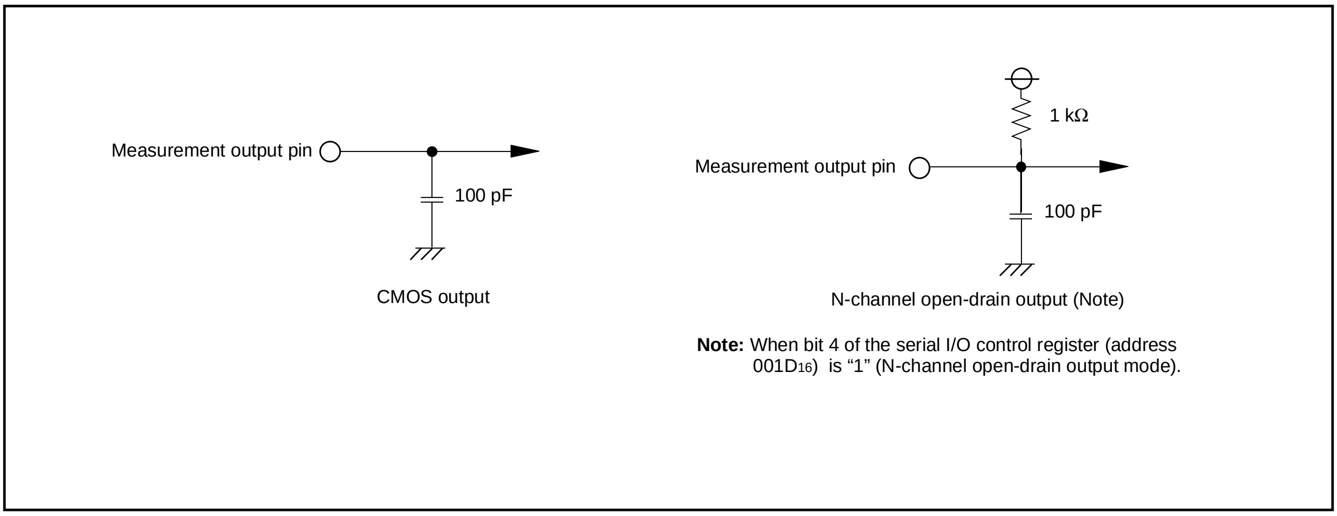


Fig. 50 Circuit for measuring output switching characteristics

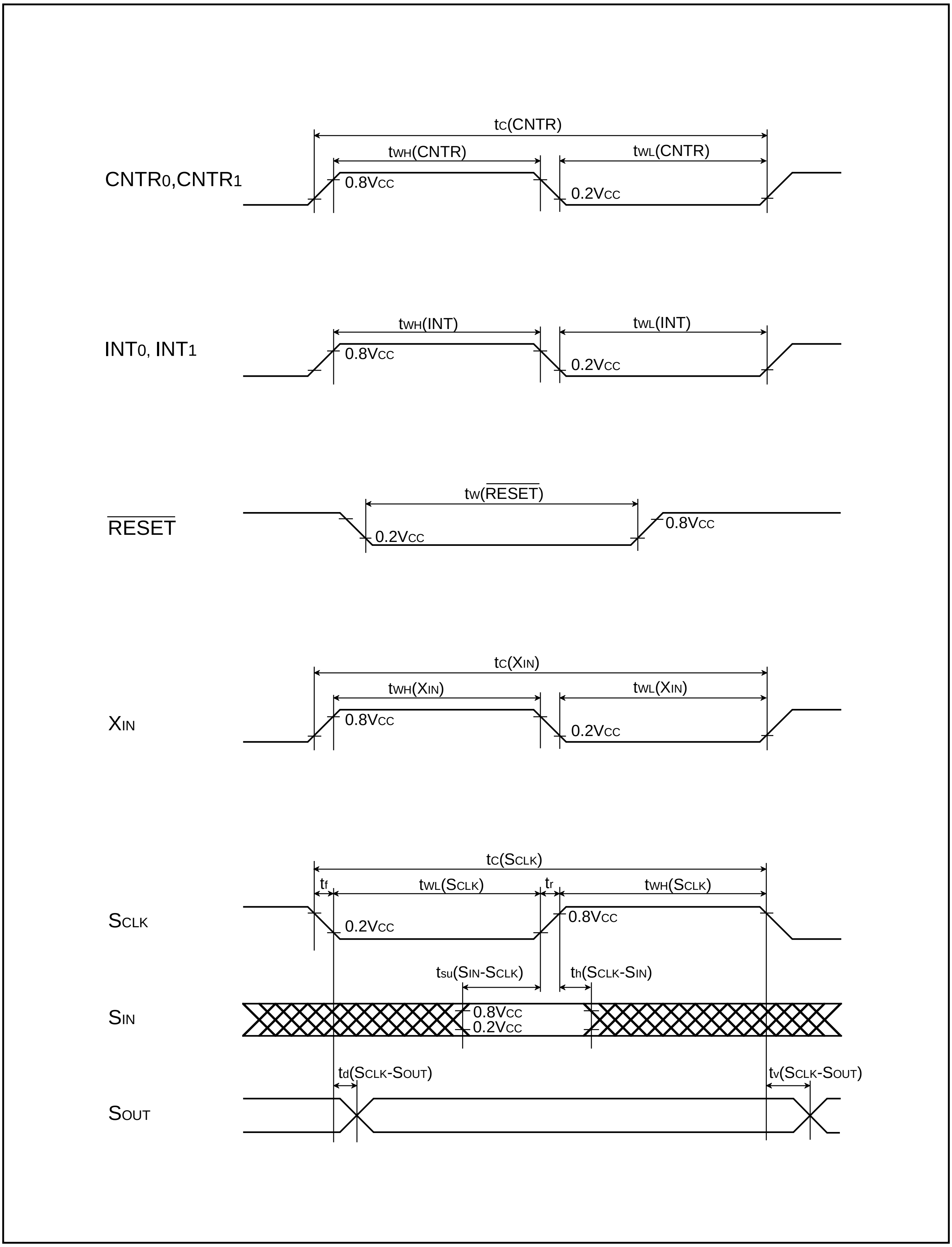


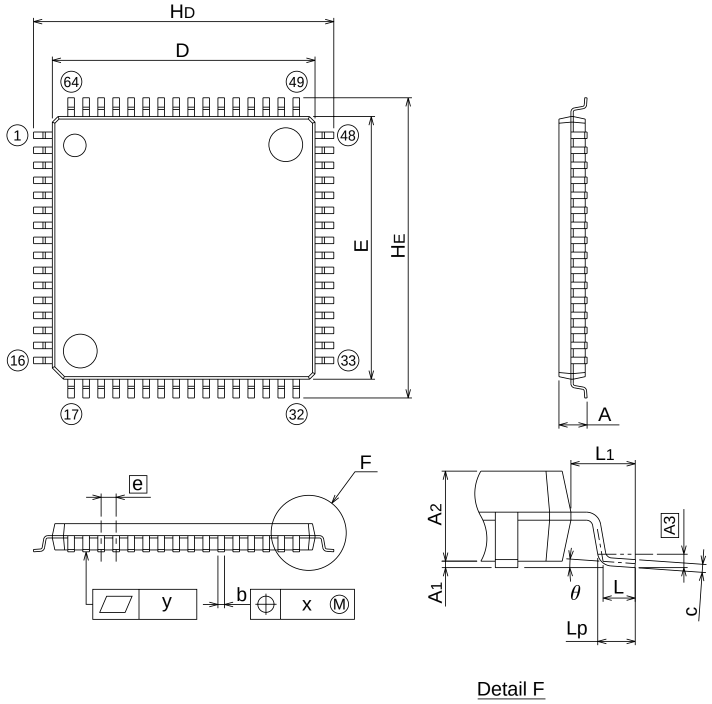
Fig. 51 Timing chart

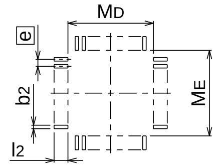
PACKAGE OUTLINE

64P6U-A

Plastic 64pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1414-0.8	–		Cu Alloy





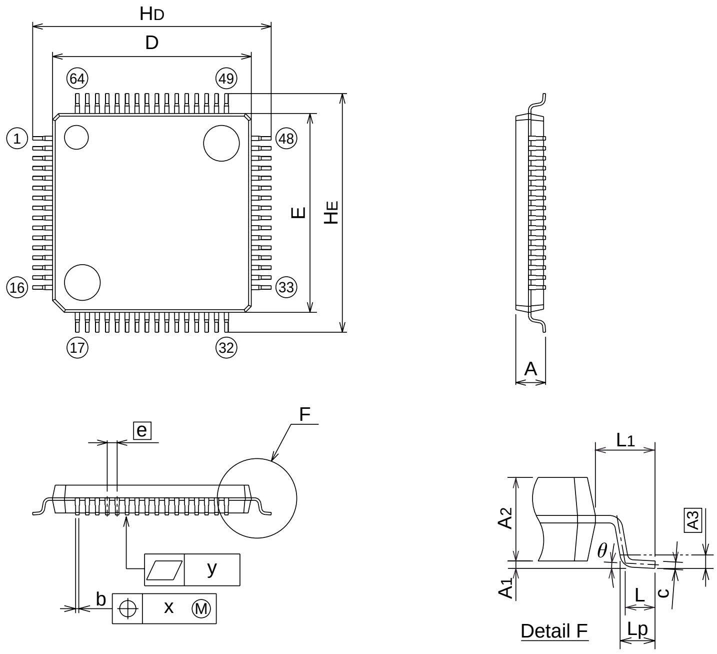
Recommended Mount Pad

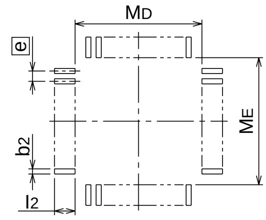
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.8	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	0.95	–	–
MD	–	14.4	–
ME	–	14.4	–

64P6Q-A

Plastic 64pin 10X10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.50	–	–	Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	–	0.5	–
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	1.0	–	–
MD	–	10.4	–
ME	–	10.4	–

REVISION HISTORY	38C1 GROUP DATA SHEET

Rev.	Date	Description: Page	Description: Summary
1.0	01/16/02		First Edition
2.0	03/28/02	1	FEATURES; • Interrupts and • Power dissipation revised.
		4	PIN DESCRIPTION; V_{L1}–V_{L3} $0 \leq V_{L1} \leq V_{L2} \leq V_{L3} \rightarrow 0 \leq V_{L1} \leq V_{L2} < V_{L3}$
		6	Table 2; Date revised. Jan. → Mar.
		10	Fig. 7; Bits 3 and 6 Description added.
		12	Fig. 10; Address 0007_{16} Port P3 direction register (P3D) Address 0008_{16} “ADKEY pin selection” added.
		14	Table 5; Note 2 revised.
		18	INTERRUPTS; fourteen sources → thirteen sources, eight internal → seven internal
		20	Fig. 17; PULL register A Bit 2 = “1” → PULL register Bit 3 = “1”
		27	● A/D Converter description added.
		28	ADKEY Control Circuit; Description revised all.
			Fig. 27; Figure title and note “pin” added.
		32	Common Pin and Duty Ratio Control; Description added.
			Table 9; Note revised.
		36	Fig. 35; Bits 0 and 1 Functional description revised.
			● RRF register; Description revised.
		41	Fig. 43; Low-speed mode CM_3 = 1 → CM_3 = * (Note 9)
		44	(3) line 5; voltage and temperature → voltage or/and temperature
		47 to 54	ELECTRICAL CHARACTERISTICS ; Most contents revised.
		47	Table 12; V_{CC} revised, VL3 and Notes added.
		49	Table 14; Note revised.
		51	Table 16; Most contents revised.
		52	Table 17; Added.
			Table 18; Most contents revised.
		53	Table 20; “(2.2 to 4.0 V for One Time PROM version)” added.
		54	Table 22; “(2.2 to 4.0 V for One Time PROM version)” added.
		56	PACKAGE OUTLINE revised.
2.1	05/09/02	6	Fig. 4 and Table 2; Revised.
		10	**[CPU Mode Register (CPUM)];** Description revised.
		16	Fig. 13; Revised.
		22	● Timer X, ■ Note on count source selection bit; Description revised.
		25	Fig. 23; Note revised.
		39	Clock generating circuit; Note revised.
		47	Table 12; “H” input voltage ADKEY0–ADKEY3, “L” input voltage ADKEY0–ADKEY3 eliminated.
		49	Table 14; Note 3 added.
		52	Table 17; “H” input voltage ADKEY0–ADKEY3, “L” input voltage ADKEY0–ADKEY3 added.

REVISION HISTORY	38C1 GROUP DATA SHEET

Rev.	Date	Description: Page	Description: Summary
2.2	Nov. 07, 2003	25	■ Notes on Serial I/O added.
		27	[A/D Control Register (ADCON)] 0034_{16}
			Also, when the bit 4 is "1", do not write "0" to bit 3 by program.
		28	Please do not write "0" in the AD conversion completion bit
			5th item;
			• Return operation by reset, STOP or WIT under A/D conversion operation at selecting ADKEY function is performed.
		46	Table 11 Absolute Maximum Ratings
			V_I Input voltage CNV_{SS} (Mask ROM version) → –0.3 to V_{CC}+0.3
		47	V_{CC} when oscillation starts revised.
			Note 2 revised.
		49	Table 14 Recommended operating conditions;
			$f(CNTR_0)$, $f(CNTR_1)$ and $f(X_{IN})$ revised.
			Note 4 added.
		51	Table 16 Electrical characteristics revised.
		52	Table 17 A/D characteristics recommended operating condition; $f(X_{IN})$ revised.
			Table 18 A/D converter characteristics; ABS revised.
		54	Table 21, 22 Switching characteristics; tr(CMOS) revised.
2.30	Dec. 24, 2003	6	Fig.4 "Under development" eliminated.
		13	Description about Port P0 added.
		14	I/O Format of $P0_0/SEG_0$–$P0_7/SEG_7$ revised.
		38	● Oscillation Control (1) Stop mode; Description revised.
			Fig.40 a resistor is added to X_{OUT} pin nd Fig. title revised.
		45	DATA REQUIRED FOR MASK ORDERS: URL revised.
2..40	Jun. 14, 2004	All pages	Words standardized: On-chip oscillator, A/D converter

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

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Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
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7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
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Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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