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April 1988 Revised September 2000

74F280

9-Bit Parity Generator/Checker

General Description

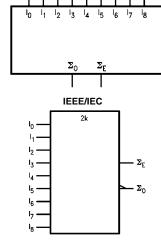
The F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output

Ordering Code:

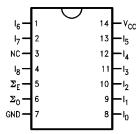
Order Number	Package Number	Package Description
74F280SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F280SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F280PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

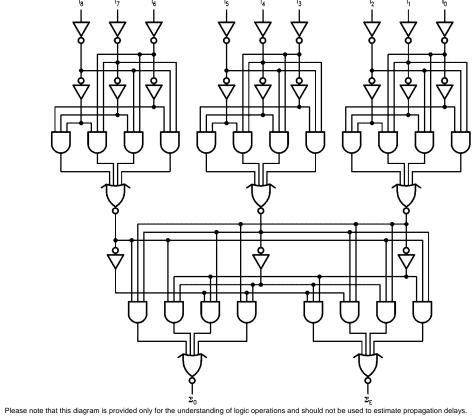
Pin Names	Description	U.L.	Input I _{IH} /I _{IL}		
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
I ₀ –I ₈	Data Inputs	1.0/1.0	20 μA/-0.6 mA		
Σ_{O}	Odd Parity Output	50/33.3	−1 mA/20 mA		
Σ_{E}	Even Parity Output	50/33.3	−1 mA/20 mA		

Truth Table

Number of	Outputs				
HIGH Inputs I ₀ –I ₈	∑ Even	Σ Odd			
0, 2, 4, 6, 8	Н	L			
1, 3, 5, 7, 9	L	Н			

H = HIGH Voltage Level L = LOW Voltage Level

Logic Diagram



Absolute Maximum Ratings(Note 1)

-65°C to +150°C

Ambient Temperature under Bias -55°C to +125°C

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

Storage Temperature

 $\begin{array}{ll} \text{Standard Output} & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & -0.5 \text{V to +5.5V} \end{array}$

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min) 4000V

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

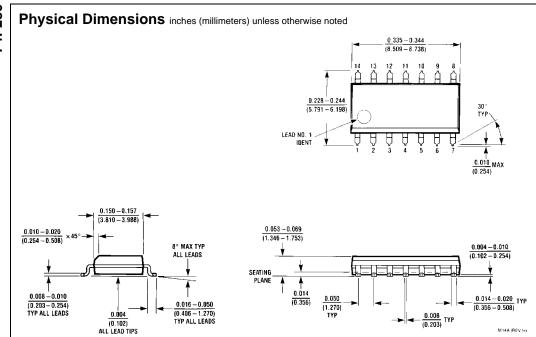
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

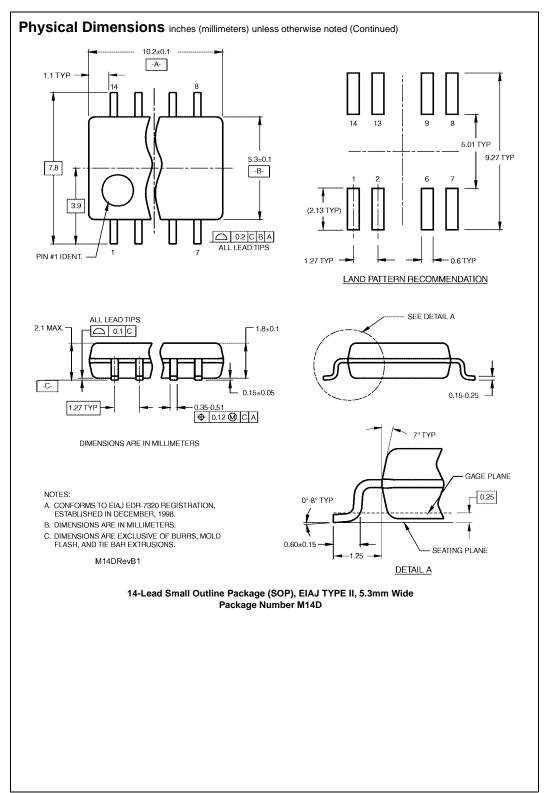
Symbol	pol Parameter		Min	Тур	Max	Units	V _{cc}	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA	
	Voltage	5% V _{CC}	2.7					$I_{OH} = -1 \text{ mA}$	
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA	
I _{IH}	Input HIGH Current				5.0	μА	Max	V _{IN} = 2.7V	
I _{BVI}	Input HIGH Current Breakdown Test				7.0	μА	Max	V _{IN} = 7.0V	
I _{CEX}	Output HIGH Leakage Current				50	μА	Max	V _{OUT} = V _{CC}	
V _{ID}	Input Leakage Test		4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded	
I _{OD}	Output Leakage Circuit Current				3.75	μА	0.0	V _{IOD} = 150 mV All Other Pins Grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V	
los	Output Short-Circuit Curren	t	-60		-150	mA	Max	V _{OUT} = 0V	
I _{CCH}	Power Supply Current			25	38	mA	Max	V _O = HIGH	

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$ $C_{L} = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0V$ $C_L = 50$ pF		Units
		Min	Тур	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	6.5	10.0	15.0	6.5	20.0	6.5	16.0	ns
t _{PHL}	I_n to Σ_E	6.5	11.0	16.0	6.5	21.0	6.5	17.0	
t _{PLH}	Propagation Delay	6.0	10.0	15.0	5.0	20.0	6.0	16.0	200
t _{PHL}	I_n to Σ_O	6.5	11.0	16.0	6.5	21.0	6.5	17.0	ns



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 14 13 12 11 10 9 8 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320(7.620 - 8.128) 0.145 - 0.200 0.060 (1.524) 4° TYP Optional (1.651) (3.683 - 5.080)95°±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 0.020 (0.508)0.125 - 0.150 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112)-MIN 0.014 - 0.023 $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ $0.325 ^{\,+\,0.040}_{\,-\,0.015}$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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 $8.255 + 1.016 \\ -0.381$

N14A (REV.F)

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