



Product Specification

XBLW UC2843

Current Mode Pulse-width Controller

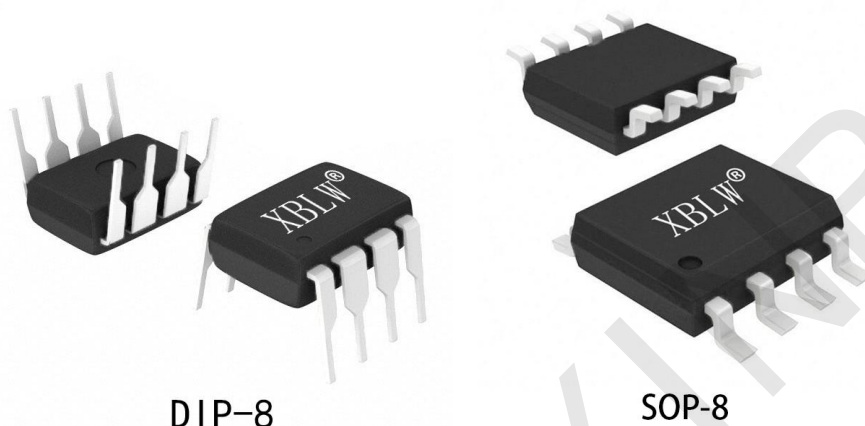
WEB | www.xinboleic.com



Descriptions

The UC2843 is a high-performance fixed frequency current mode controller. They are designed specifically for offline converters and DC-DC converter applications, providing designers with low-cost solutions with minimal external components. These integrated circuits have fine tuned oscillators with precise duty cycle control, temperature compensated reference power supplies, high gain error amplifiers, current detection comparators, and high current totem pole outputs that are highly suitable for driving power MOSFETs. It also includes protection functions, including input and undervoltage locking, cycle by cycle current limiting, programmable output dead time, and latches for single pulse metering.

This device is available in SOP-8 package and DIP-8 package.



Feature

- Stable internal bandgap reference voltage source
- Enhanced load response characteristics
- Pulse by pulse current limitation
- Automatic negative feedback compensation circuit
- High current totem pole output (driving current up to 1A)
- Undervoltage lockout circuit
- Low Startup and Operating Current (< 0.13mA)
- The working frequency can reach 500kHz

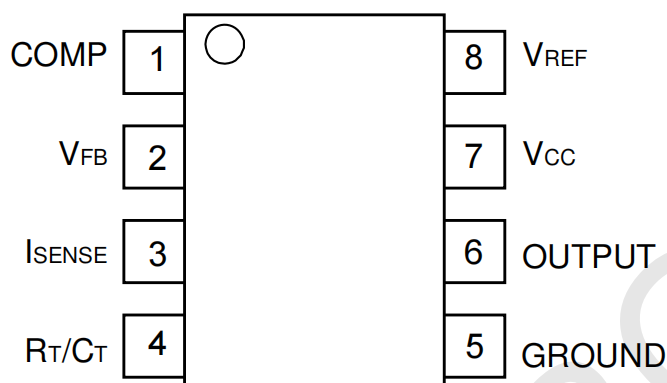
Applications

- Switching regulators of any polarity
- Transformer-coupled DC-DC converters

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW UC2843AN	DIP-8	UC2843AN	Tube	2000pcs/Box
XBLW UC2843BDTR	SOP-8	UC2843B	Tape	2500pcs/Reel

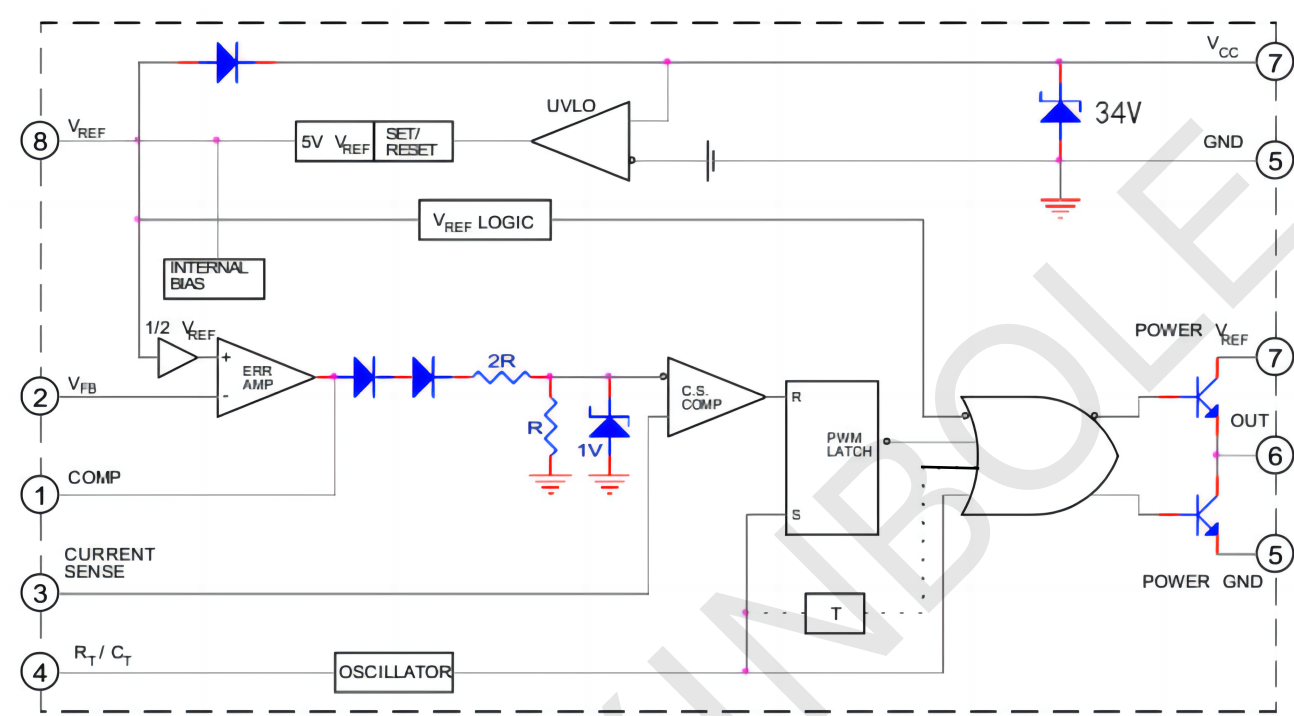
Pins Description



(Top view)

No.	Name	Symbol	Description
1	Compensation	COMP	Error amplifier compensation pin. Connect external compensation components to this pin to modify the error amplifier output.
2	Voltage Feedback	V _{FB}	Inverting input to the internal error amplifier. VFB is used to control the power converter voltage-feedback loop for stability
3	Current Sense	I _{SENSE}	Primary-side current sense pin. Connect to current sensing resistor. The PWM uses this signal to terminate the OUTPUT switch conduction.
4	Oscillator	R _T / C _T	Connect timing resistor, RRT, to VREF and timing capacitor, CCT, to GROUND from this pin to set the switching frequency and maximum output ratio. Maximum frequency can up to 500kHz .
5	Ground	GND	Ground
6	Output	OUTPUT	OUTPUT is the gate drive for the external MOSFET. Peak currents of up to 1 A are sourced and sunk by this pin.
7	Power Supply	V _{CC}	provides power to the device.
8	Reference Voltage	V _{REF}	VREF is used to provide charging current to the oscillator timing capacitor through the timing resistor.

Simplified Block Diagram



Absolute Maximum Ratings

($T_{amb} = 25^\circ\text{C}$, unless otherwise noted)

Rating	Symbol	Value		Unit
		Min.	Max.	
Power voltage	V_{CC}		30	V
Output Current	I_o	-1	1	A
Output Energy	W		5	μJ
Error Amp Output Sink Current	I_o		10	mA
Current Sense and Voltage Feedback Inputs	V_{in}	-0.3	6.3	V
Operating Junction Temperature	T_j		150	$^\circ\text{C}$
Power Dissipation	P_D		1	W
Operating Ambient Temperature	T_{amb}	-40	85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55	150	$^\circ\text{C}$

Electrical Characteristics

($V_{CC}=15V$ *Note 1, $R_T=10k\Omega$, $C_T=3.3nF$, $T_{amb}=-40^{\circ}C\sim 85^{\circ}C$, unless otherwise noted)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Reference Section						
Reference Output Voltage	V_{REF}	$T_j=25^{\circ}C, I_{REF}=1mA$	4.9	5.00	5.1	V
Line Regulation rate	Reg_{line}	$12V \leq V_{CC} \leq 25V$		6	20	mV
Load Regulation	Reg_{load}	$1mA \leq I_{REF} \leq 20mA$		6	25	mV
Output Short Circuit Current	I_{sc}	$T_{amb}=25^{\circ}C$	-30	-80	-180	mA
Oscillator Section						
Frequency	f_{osc}	$T_j=25^{\circ}C$	47	52	57	kHz
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	$12V \leq V_{CC} \leq 25V$		0.2	1	%
Oscillator Voltage Swing	$V_{(OSC)}$	PIN 4 peak to peak		1.6		Vpp
Error Amplifier Section (EA)						
Input Bias Current	I_{BIAS}	$V_{FB}=5.0V$		-0.1	-2	μA
Voltage Feedback Input	$V_{in(EA)}$	$V_{FB}=V_{comp}$	2.42	2.50	2.58	V
Open Loop Voltage Gain	G_{VO}	$2V \leq V_o \leq 4V$	60	90		dB
Power Supply Rejection Ratio	PSRR	$12V \leq V_{CC} \leq 25V$	60	70		dB
Output Current – Sink	I_{SINK}	$V_{FB}=2.7V, V_{COMP}=1.1V$	2	6.5		mA
Output Current – Source	I_{SOURCE}	$V_{FB}=2.3V, V_{COMP}=5V$	-0.5	-0.9		mA
Output Voltage Swing (High State)	V_{OH}	$V_{FB}=2.3V, R_L=15k\Omega$ to GND	5	6.4		V
Output Voltage Swing (Low State)	V_{OL}	$V_{FB}=2.7V, R_L=15k\Omega$ to P in 8		0.87	1.1	V

Electrical Characteristics

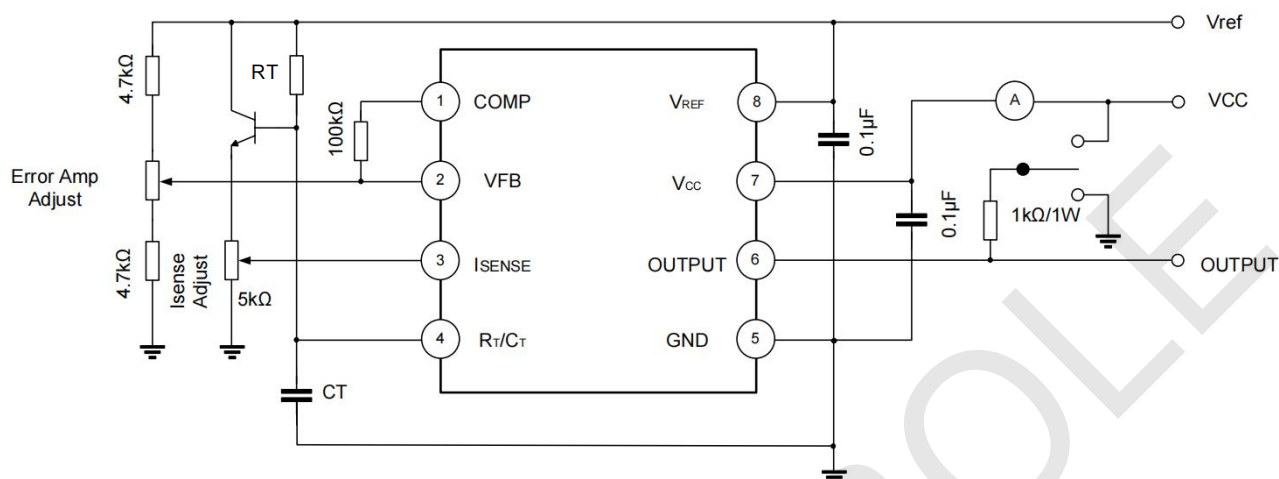
($V_{CC}=15V, R_T=10k\Omega$, $C_T=3.3nF, T_{amb}=0^\circ C \sim 70^\circ C$, unless otherwise noted)

Current Sense Section						
Current Sense Input Voltage Gain	G_V	*Note 2 and *Note 3	2.85	3	3.15	V/V
Maximum Current Sense Input Threshold	$V_{I(MAX)}$	$V_{COMP}=5V$ *Note 2	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$12V \leq V_{CC} \leq 25V$ *Note 2	-	70	-	dB
Input Bias Current	I_{BIAS}		-	-2	-10	μA
Output Section						
Output Voltage Low State	V_{OL}	$I_{SINK}=20mA$	-	0.1	0.4	V
		$I_{SINK}=200mA$	-	1.5	2.2	V
Output Voltage High State	V_{OH}	$I_{SOURCE}=20mA$	13	13.5	-	V
		$I_{SOURCE}=200mA$	12	13.0	-	V
Output Voltage Rise Time	t_r	$C_L=1nF$	-	50	150	ns
Output Voltage Fall Time	t_f	$C_L=1nF$	-	50	150	ns
Undervoltage Lockout Section						
Startup Threshold	$V_{TH(ST)}$		7.8	8.3	9.0	V
Minimum Operating Voltage After Turn-On	$V_{OPR(MIN)}$		7.0	7.6	8.2	V
PWM Section						
Duty Cycle Maximum	$DC (MAX)$		90	94	-	%
Duty Cycle Minimum	$DC (MIN)$		-	-	0	%
Total Device						
Power Supply Current (Startup)	I_{ST}		-	0.13	0.5	mA
Power Supply Current(Operating)	$I_{CC(OPR)}$	$V_{SENSE}=V_{FB}=0V$	-	11	17	mA
Power Supply Zener Voltage	V_Z	$I_{CC}=25mA$	-	34	-	V

Note:

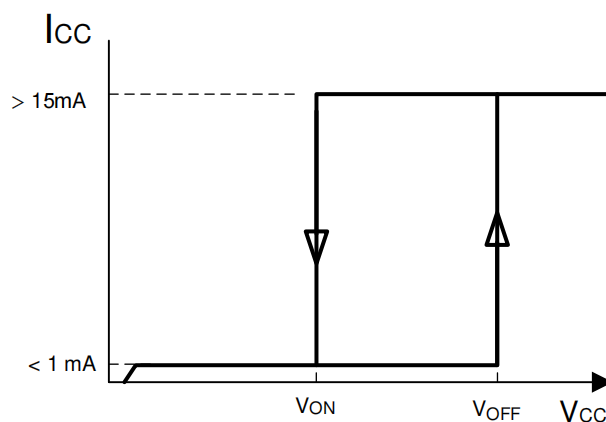
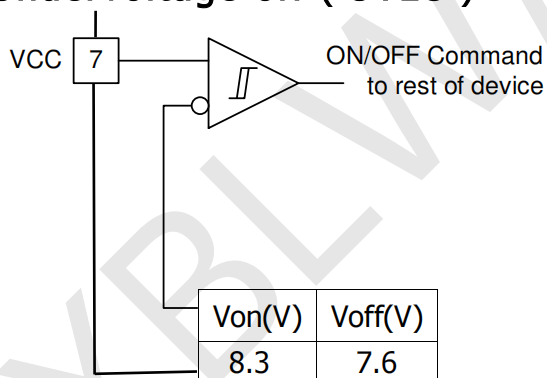
1. Adjust V_{CC} to 15V after circuit startup
2. Parameters measured at the latch transition point
3. Gain is defined as $AV=\Delta V_{comp}/\Delta V_{sense}$; $0 \leq V_{sense} \leq 0.8V$

Basic Test Circuit Diagram



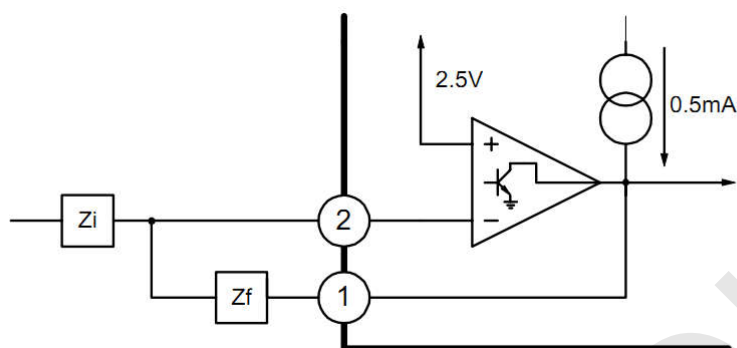
Grounding techniques should be carefully considered when there are high peak currents associated with capacitive loads. The timing and bypass capacitors must be installed next to the PIN5 and single-point grounded. Transistors and 5k Ω potentiometers are used to sample waveforms and send waveforms with adjustable slopes to PIN3.

Undervoltage off (UVLO)



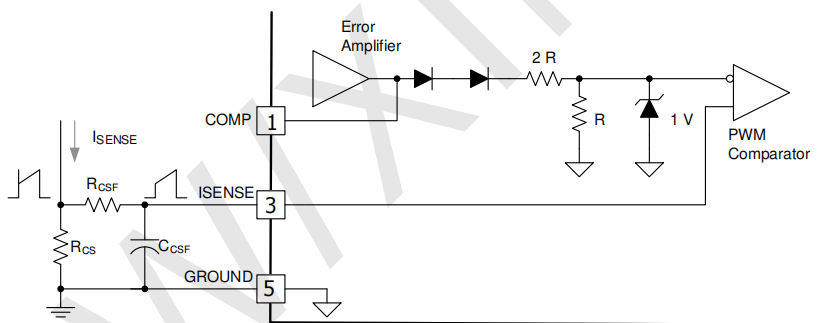
The output driver is placed in a high impedance state when entering an undervoltage shutdown. The sixth pin must be grounded with a leakage resistance to prevent leakage current from pushing the power switch

Error amplifier connection



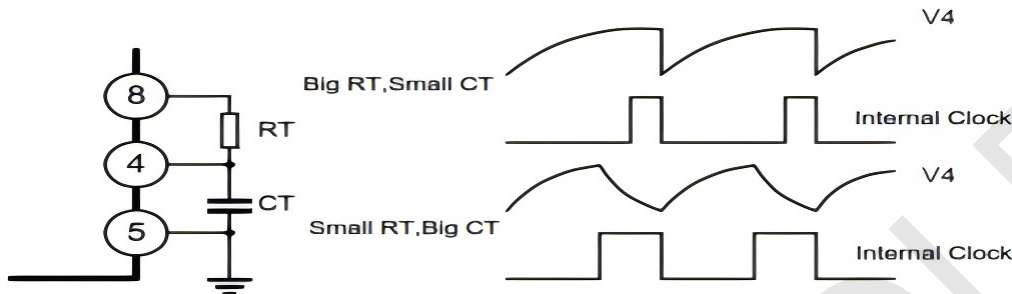
Error amplifier can push-pull output 0.5 ma current

Current detection circuit



Peak current (I_S) is defined as: $I_{S(MAX)} \approx 1.0 \text{ V}/R_S$ requires a small RC filter network to suppress the transient response of the switch.

Oscillator waveform and maximum duty cycle, period



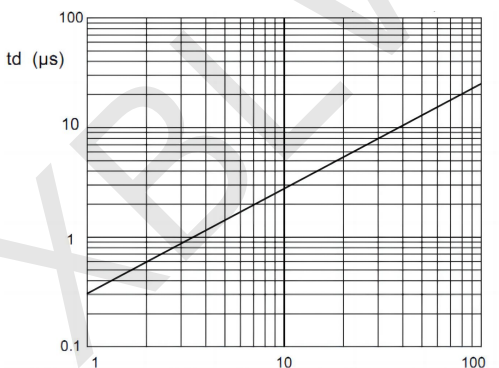
The oscillating time capacitor C_T is charged by V_{REF} via R_T and discharged by an internal current source. The internal clock signal drives the output to a low level during discharge. The oscillation period and the maximum duty cycle can be determined by selecting R_T and C_T simultaneously. The time of charge and discharge is determined by the following formula:

$$t_c \approx 0.55 R_T * C_T$$

$$t_d \approx R_T * C_T * \ln\left(\frac{0.063 R_T - 2.7}{0.063 R_T - 4}\right)$$

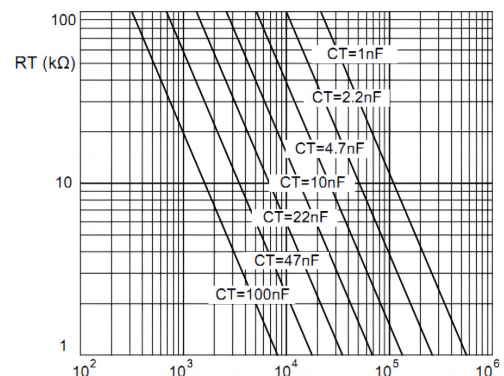
$$\text{The frequency is: } f = (t_c + t_d)^{-1}$$

$$\text{When: } R_T > 5K\Omega, \quad f \approx \frac{1.8}{R_T * C_T}$$



Electrical time capacitance (nF)

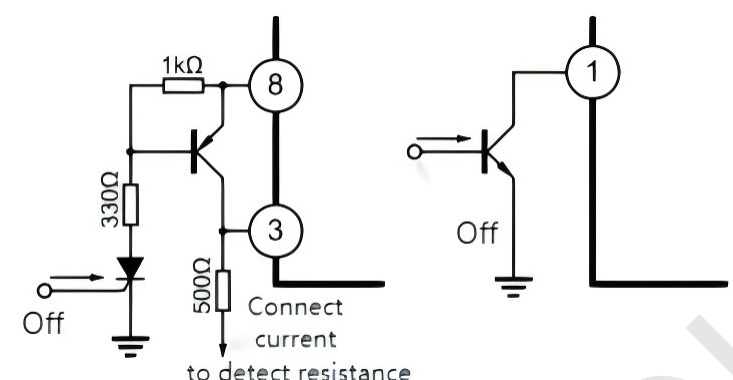
Relationship between oscillation dead time and capacitance C_T



Frequency (Hz)

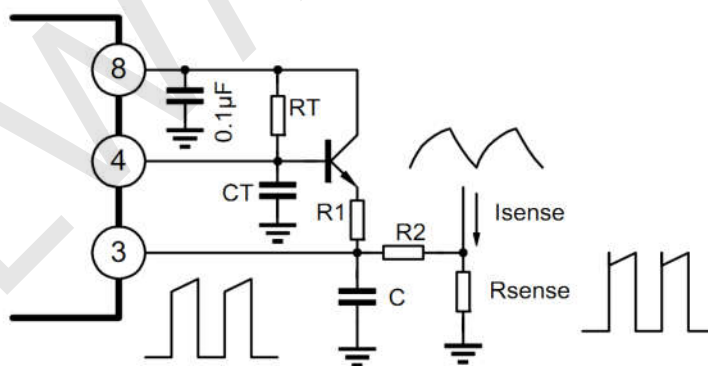
Relationship between frequency and timing resistance

Off technology

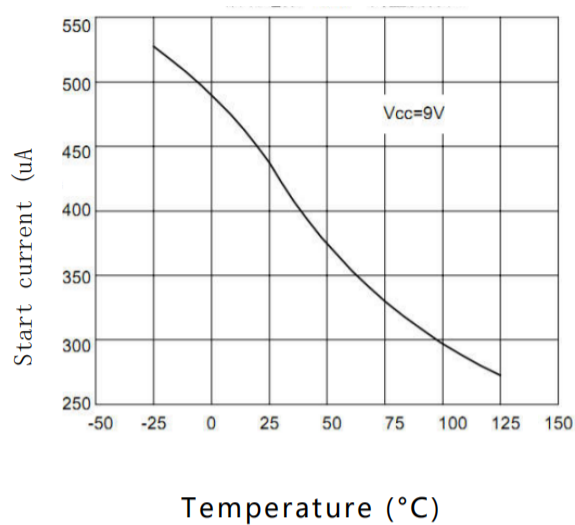


The shutdown of UC2843 can be accomplished in two ways: by raising the No. 3 pin voltage above 1V or by lowering the No. 1 pin voltage to within the forward voltage drop of the two diodes at the ground level, both methods make the output of the PWM comparator high (see internal block diagram). The PWM latch trigger is preferentially reset so that the output is kept at a low level until the next clock cycle after the off signal of Pin 1 or Pin 3 is removed. An example of an external latch-off is achieved by adding a one-way SCR, which resets when the supply voltage VCC is below the UVLO threshold. At this point, the SCR is allowed to reset when the reference voltage is turned off.

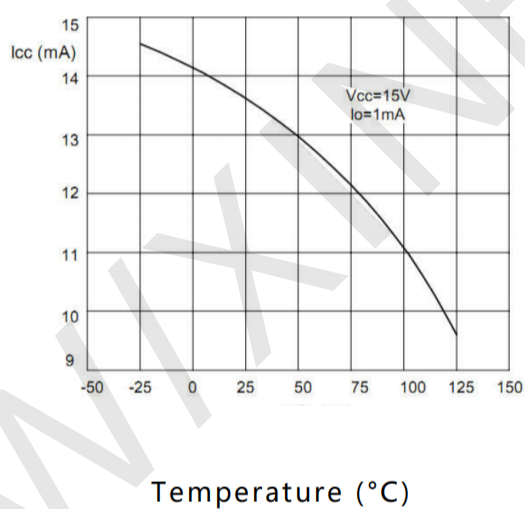
Slope Compensation



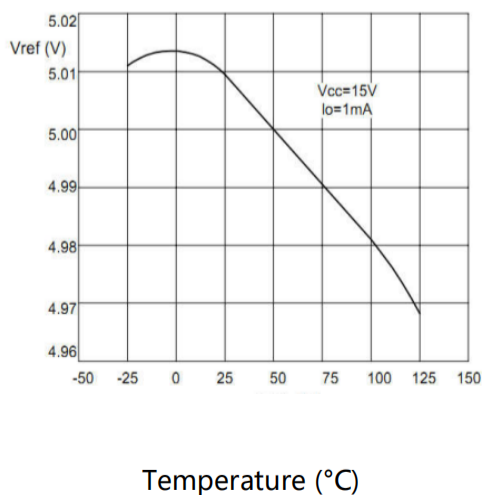
A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor CCSF forms a filter with RCSF to suppress the leading-edge switch spikes.



Start current IST temperature characteristics



Temperature characteristics of power dissipation current ICC

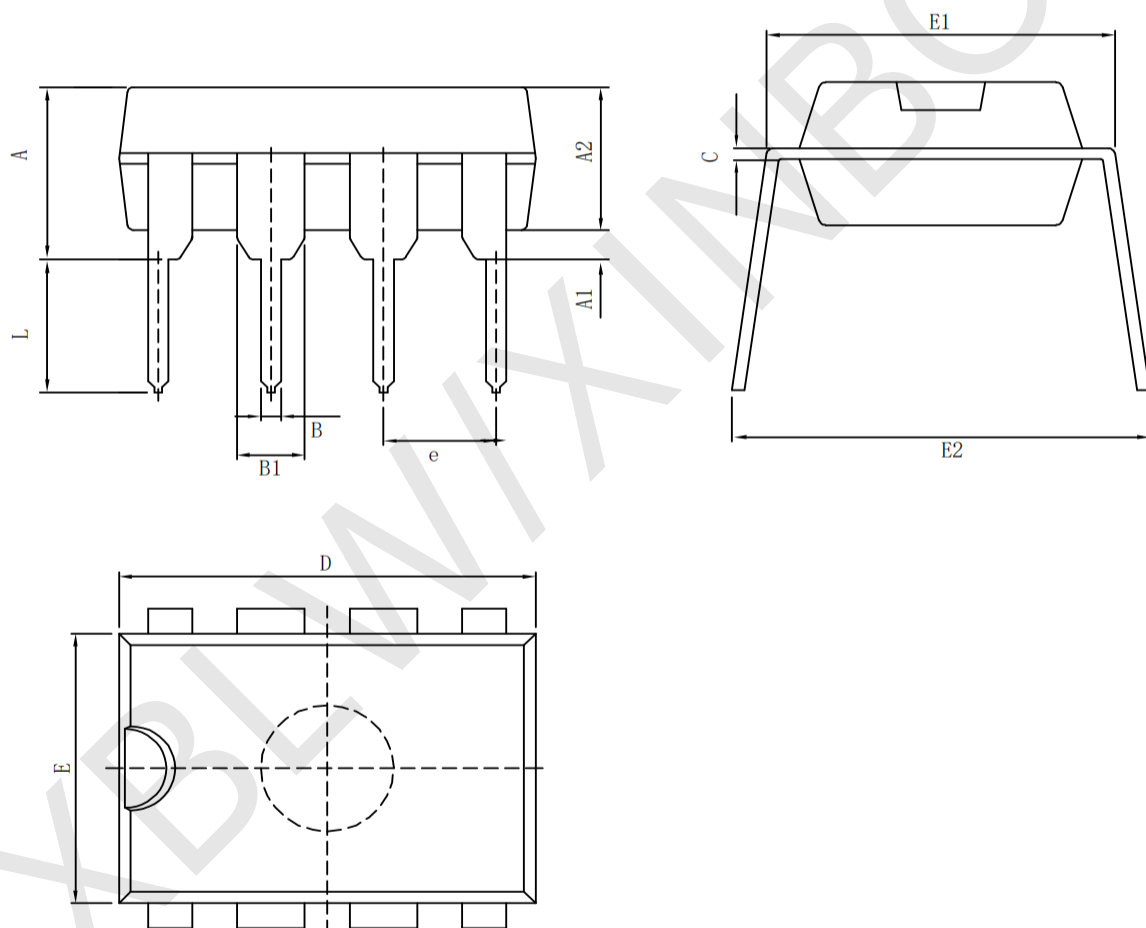


Refer to the temperature characteristics of the voltage source Vref

Package Information

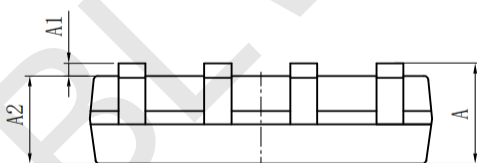
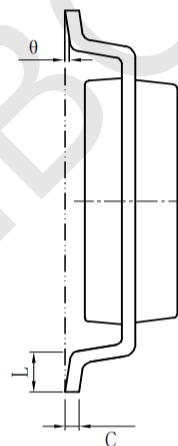
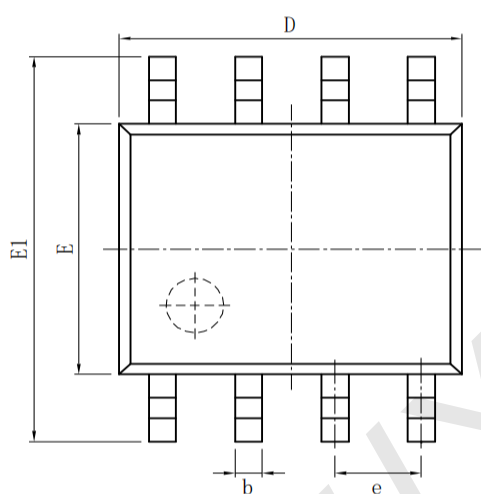
• DIP-8

Symbol	Size	Dimensions In Millimeters		Symbol	Size	Dimensions In Inches	
		Min(mm)	Max(mm)			Min(in)	Max(in)
A		3.710	4.310	A		0.146	0.170
A1		0.510		A1		0.020	
A2		3.200	3.600	A2		0.126	0.142
B		0.380	0.570	B		0.015	0.022
B1		1.524 (BSC)		B1		0.060 (BSC)	
C		0.204	0.360	C		0.008	0.014
D		9.000	9.400	D		0.354	0.370
E		6.200	6.600	E		0.244	0.260
E1		7.320	7.920	E1		0.288	0.312
e		2.540 (BSC)		e		0.100 (BSC)	
L		3.000	3.600	L		0.118	0.142
E2		8.400	9.000	E2		0.331	0.354



• SOP-8

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270 (BSC)		e	0.050 (BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°



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