

DS90LV110AT

DS90LV110AT 1 to 10 LVDS Data/Clock Distributor with Failsafe



Literature Number: SNOSAC2I

DS90LV110AT

1 to 10 LVDS Data/Clock Distributor with Failsafe

General Description

DS90LV110A is a 1 to 10 data/clock distributor utilizing LVDS (Low Voltage Differential Signaling) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. The design allows connection of 1 input to all 10 outputs. LVDS I/O enable high speed data transmission for point-to-point interconnects. This device can be used as a high speed differential 1 to 10 signal distribution / fanout replacing multi-drop bus applications for higher speed links with improved signal quality. It can also be used for clock distribution up to 200MHz.

The DS90LV110A accepts LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

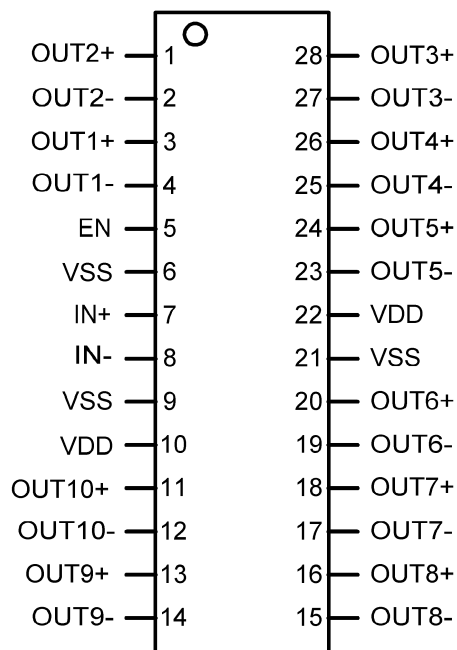
The LVDS outputs can be put into TRI-STATE® by use of the enable pin.

For more details, please refer to the Application Information section of this datasheet.

Features

- Low jitter 400 Mbps fully differential data path
- 145 ps (typ) of pk-pk jitter with PRBS = $2^{23}-1$ data pattern at 400 Mbps
- Single +3.3 V Supply
- Balanced output impedance
- Output channel-to-channel skew is 35ps (typ)
- Differential output voltage (V_{OD}) is 320mV (typ) with 100 Ω termination load.
- LVDS receiver inputs accept LVPECL signals
- LVDS input failsafe
- Fast propagation delay of 2.8 ns (typ)
- Receiver open, shorted, and terminated input failsafe
- 28 lead TSSOP package
- Conforms to ANSI/TIA/EIA-644 LVDS standard

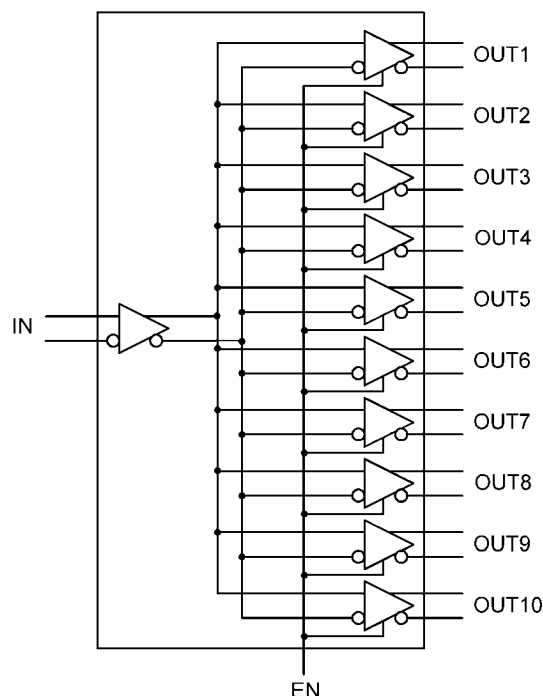
Connection Diagram



Order Number DS90LV110ATMT
See NS Package Number MTC28

20098205

Block Diagram



20098201

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD}-V_{SS}$)	-0.3V to +4V
LVC MOS/LVTTL Input Voltage (EN)	-0.3V to ($V_{CC} + 0.3V$)
LVDS Receiver Input Voltage (IN+, IN-)	-0.3V to +4V
LVDS Driver Output Voltage (OUT+, OUT-)	-0.3V to +4V
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
28L TSSOP	2.115 W

Package Derating

28L TSSOP

16.9 mW/°C above +25°C

θ_{JA}

(4-Layer, 2 oz. Cu, JEDEC)

28L TSSOP

59.1 °C/Watt

ESD Rating:

(HBM, 1.5kΩ, 100pF)

> 8 kV

(EIAJ, 0Ω, 200pF)

> 250 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ($V_{DD} - V_{SS}$)	3.0	3.3	3.6	V
Receiver Input Voltage	0		V_{DD}	V
Operating Free Air Temperature	-40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVC MOS/LVTTL DC SPECIFICATIONS (EN)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		V_{SS}		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 3.6V$ or $2.0V$; $V_{DD} = 3.6V$		±7	±20	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$ or $0.8V$; $V_{DD} = 3.6V$		±7	±20	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.8	-1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10)						
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	320	450	mV
		$R_L = 100\Omega$, $V_{DD} = 3.3V$, $T_A = 25^\circ C$	260	320	425	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	ImV
V_{OS}	Offset Voltage (Note 3)		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	ImV
I_{OZ}	Output TRI-STATE Current	EN = 0V, $V_{OUT} = V_{DD}$ or GND		±1	±10	μA
I_{OFF}	Power-Off Leakage Current	$V_{DD} = 0V$; $V_{OUT} = 3.6V$ or GND		±1	±10	μA
I_{SA}, I_{SB}	Output Short Circuit Current	V_{OUT+} OR $V_{OUT-} = 0V$ or V_{DD}		12	24	ImA
I_{SAB}	Both Outputs Shorted (Note 4)	$V_{OUT+} = V_{OUT-}$		6	12	ImA
LVDS RECEIVER DC SPECIFICATIONS (IN)						
V_{TH}	Differential Input High Threshold	$V_{CM} = +0.05V$ or $+1.2V$ or $+3.25V$, $V_{DD} = 3.3V$		0	+100	mV
V_{TL}	Differential Input Low Threshold		-100	0		mV
V_{CMR}	Common Mode Voltage Range	$V_{ID} = 100mV$, $V_{DD} = 3.3V$	0.05		3.25	V
I_{IN}	Input Current	$V_{IN} = +3.0V$, $V_{DD} = 3.6V$ or 0V		±1	±10	μA
		$V_{IN} = 0V$, $V_{DD} = 3.6V$ or 0V		±1	±10	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENT						
I_{CCD}	Total Supply Current	$R_L = 100\Omega$, $C_L = 5\text{ pF}$, 200 MHz, EN = High		125	160	mA
		No Load, 200 MHz, EN = High		80	125	mA
I_{CCZ}	TRI-STATE Supply Current	EN = Low		15	29	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical are given for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, unless otherwise stated.

Note 3: V_{OS} is defined as $(V_{OH} + V_{OL}) / 2$.

Note 4: Only one output can be shorted at a time. Don't exceed the package absolute maximum rating.

AC Electrical Characteristics

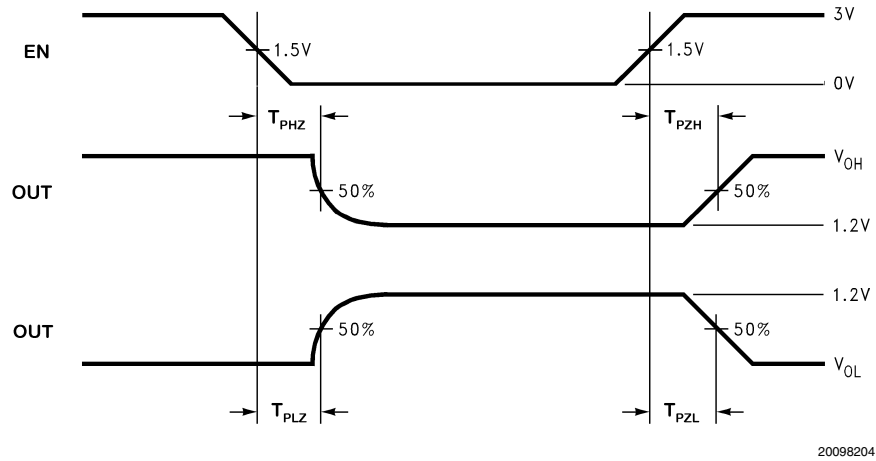
Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{LHT}	Output Low-to-High Transition Time, 20% to 80%, <i>Figure 4</i> (Note 5)			390	550	ps
T_{HLT}	Output High-to-Low Transition Time, 80% to 20%, <i>Figure 4</i> (Note 5)			390	550	ps
T_{DJ}	LVDS Data Jitter, Deterministic (Peak-to-Peak) (Note 6)	$V_{ID} = 300\text{mV}$; PRBS=2 ²³ -1 data; $V_{CM} = 1.2\text{V}$ at 400 Mbps (NRZ)		145		ps
T_{RJ}	LVDS Clock Jitter, Random (Note 6)	$V_{ID} = 300\text{mV}$; $V_{CM} = 1.2\text{V}$ at 200 MHz clock		2.8		ps
T_{PLHD}	Propagation Low to High Delay, <i>Figure 5</i>		2.2	2.8	3.6	ns
T_{PHLD}	Propagation High to Low Delay, <i>Figure 5</i>		2.2	2.8	3.9	ns
T_{SKEW}	Pulse Skew $ T_{PLHD} - T_{PHLD} $ (Note 5)			20	340	ps
T_{CCS}	Output Channel-to-Channel Skew, <i>Figure 6</i> (Note 5)			35	91	ps
T_{PHZ}	Disable Time (Active to TRI-STATE) High to Z, <i>Figure 1</i>			3.0	6.0	ns
T_{PLZ}	Disable Time (Active to TRI-STATE) Low to Z, <i>Figure 1</i>			1.8	6.0	ns
T_{PZH}	Enable Time (TRI-STATE to Active) Z to High, <i>Figure 1</i>			10.0	23.0	ns
T_{PZL}	Enable Time (TRI-STATE to Active) Z to Low, <i>Figure 1</i>			7.0	23.0	ns

Note 5: The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage and temperature) range.

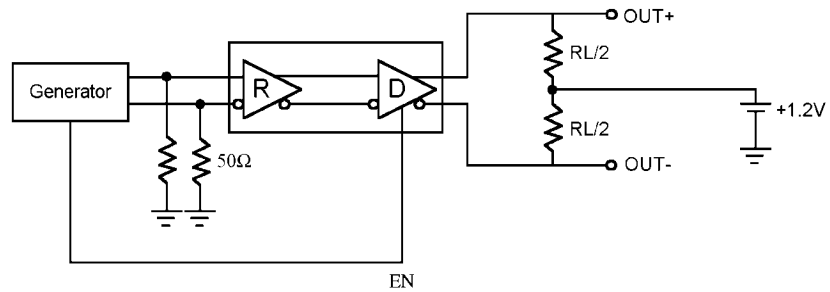
Note 6: The measurement used the following equipment and test setup: HP8133A pattern/pulse generator, 5 feet of RG-142 cable with DUT test board and HP83480A (digital scope mainframe) with HP83484A (50GHz scope module). The HP8133A with the RG-142 cable exhibit a $T_{DJ} = 26\text{ps}$ and $T_{RJ} = 1.3\text{ ps}$

AC Timing Diagrams



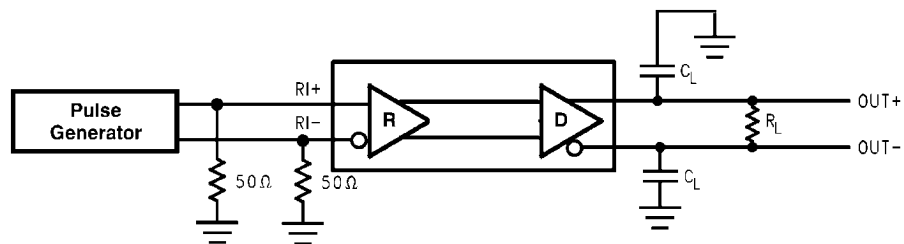
20098204

FIGURE 1. Output active to TRI-STATE and TRI-STATE to active output time



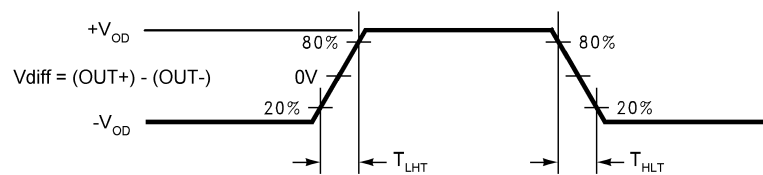
20098215

FIGURE 2. LVDS Driver TRI-STATE Circuit



20098206

FIGURE 3. LVDS Output Load



20098209

FIGURE 4. LVDS Output Transition Time

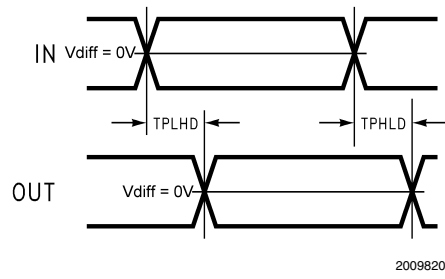


FIGURE 5. Propagation Delay Low-to-High and High-to-Low

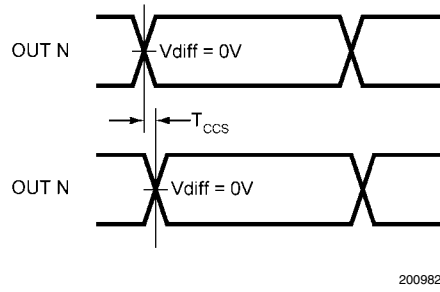


FIGURE 6. Output 1 to 10 Channel-to-Channel Skew

DS90LV110A Pin Descriptions

Pin Name	# of Pin	Input/Output	Description
IN+	1	I	Non-inverting LVDS input
IN -	1	I	Inverting LVDS input
OUT+	10	O	Non-inverting LVDS Output
OUT -	10	O	Inverting LVDS Output
EN	1	I	This pin has an internal pull-down when left open. A logic low on the Enable puts all the LVDS outputs into TRI-STATE and reduces the supply current.
V _{SS}	3	P	Ground (all ground pins must be tied to the same supply)
V _{DD}	2	P	Power Supply (all power pins must be tied to the same supply)

Application Information

INPUT FAIL-SAFE

The receiver inputs of the DS90LV110A have internal fail-safe biasing for short, open, and terminated input conditions.

LVDS INPUTS TERMINATION

The LVDS Receiver input must have a 100Ω termination resistor placed as close as possible across the input pins.

UNUSED CONTROL INPUTS

The EN control input pin has internal pull down device. If left open, the 10 outputs will default to TRI-STATE.

EXPANDING THE NUMBER OF OUTPUT PORTS

To expand the number of output ports, more than one DS90LV110A can be used. Total propagation delay through the devices should be considered to determine the maximum expansion. Adding more devices will increase the output jitter due to each pass.

PCB LAYOUT AND POWER SYSTEM BYPASS

Circuit board layout and stack-up for the DS90LV110A should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the

value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 μF to 0.1 μF. Tantalum capacitors may be in the range 2.2 μF to 10 μF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the DS90LV110A as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

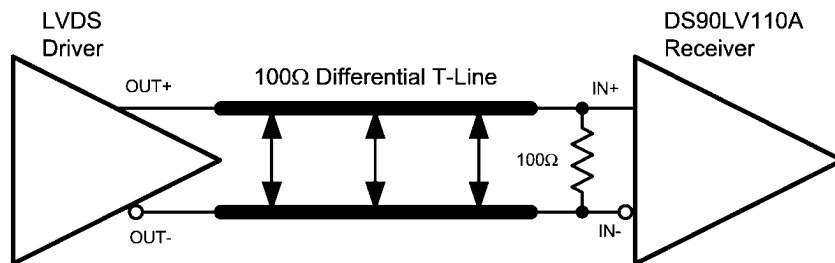
The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

There are more common practices which should be followed when designing PCBs for LVDS signaling. Please see Application Note: AN-1108 for additional information.

INPUT INTERFACING

The DS90LV110A accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the DS90LV110A can be DC-coupled with all common differential

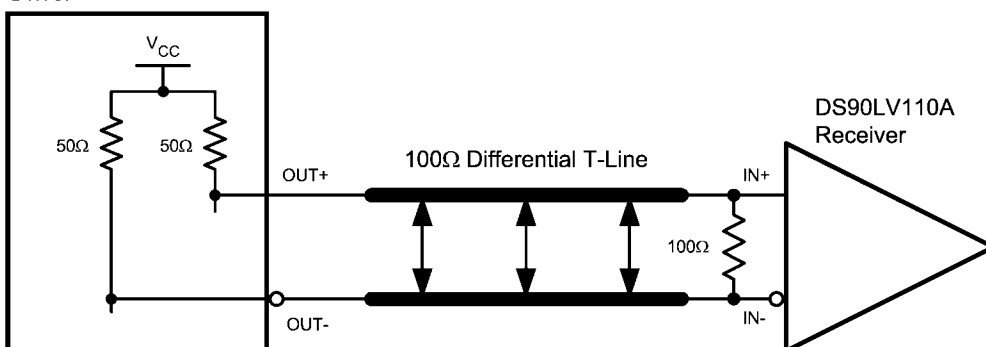
drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.



20098241

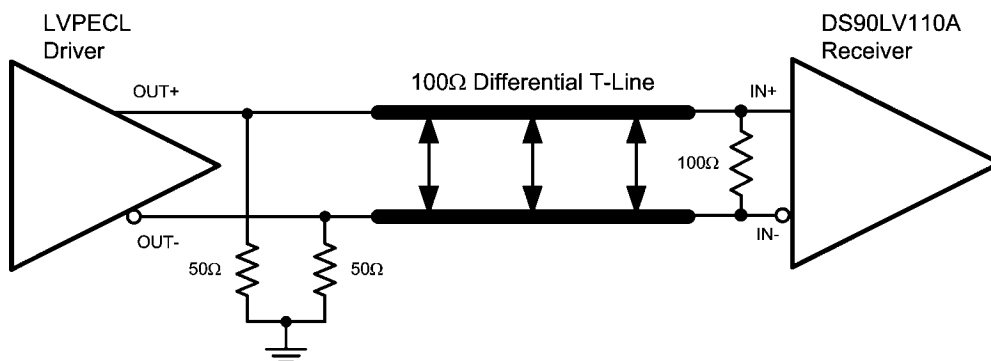
Typical LVDS Driver DC-Coupled Interface to DS90LV110A Input

CML3.3V or CML2.5V
Driver



20098242

Typical CML Driver DC-Coupled Interface to DS90LV110A Input



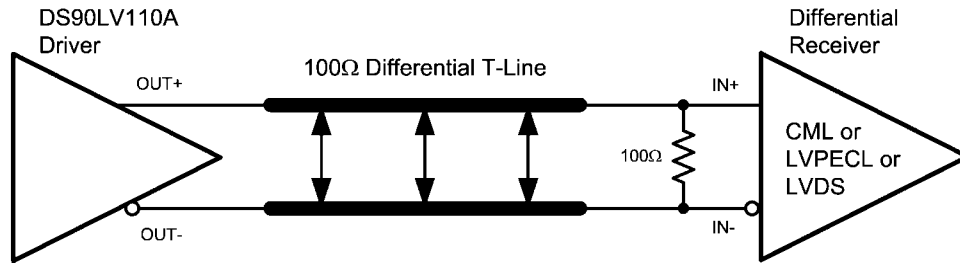
20098243

Typical LVPECL Driver DC-Coupled Interface to DS90LV110A Input

OUTPUT INTERFACING

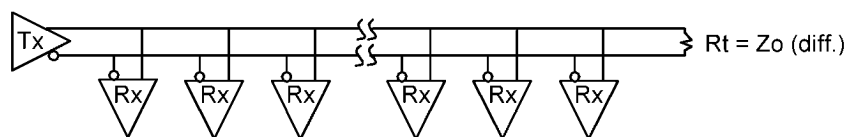
The DS90LV110A outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers

and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



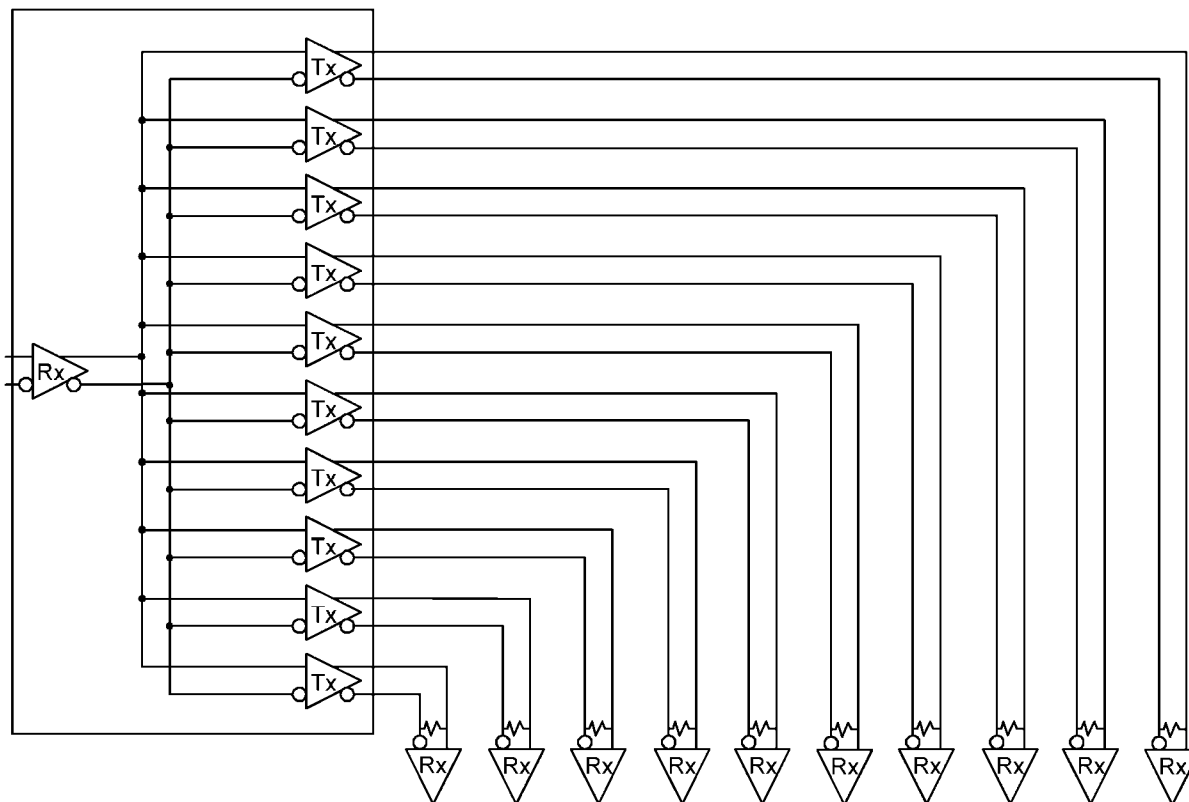
Typical DS90LV110A Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver 20098244

Multi-Drop Applications



20098202

Point-to-Point Distribution Applications



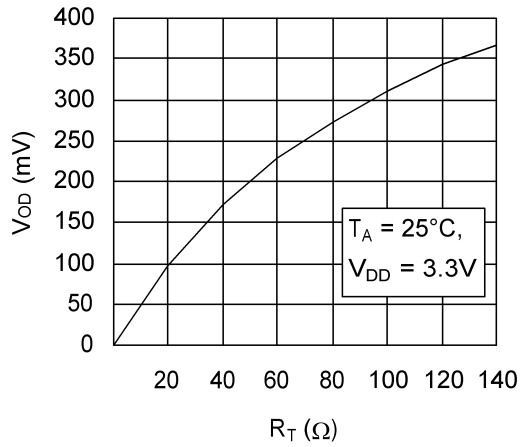
20098203

For applications operating at data rate greater than 400Mbps, a point-to-point distribution application should be used. This improves signal quality compared to multi-drop applications due to no stub PCB trace loading. The only load is a receiver

at the far end of the transmission line. Point-to-point distribution applications will have a wider LVDS bus lines, but data rate can increase well above 400Mbps due to the improved signal quality.

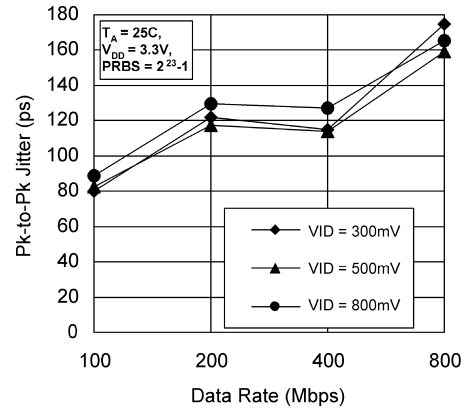
Typical Performance Characteristics

Output Voltage (V_{OD}) vs. Resistive Load (R_L)



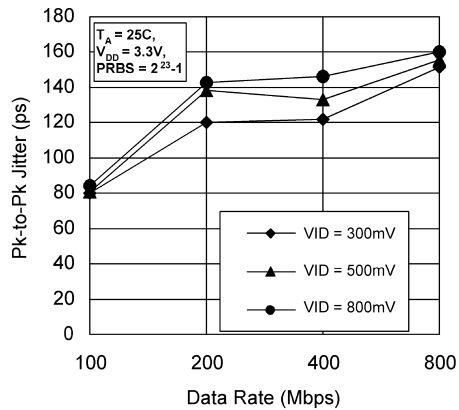
20098211

Peak-to-Peak Output Jitter at $V_{CM} = +0.4\text{V}$ vs. VID



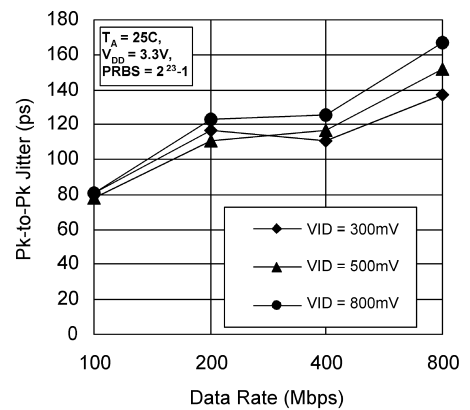
20098212

Peak-to-Peak Output Jitter at $V_{CM} = +1.2\text{V}$ vs. VID



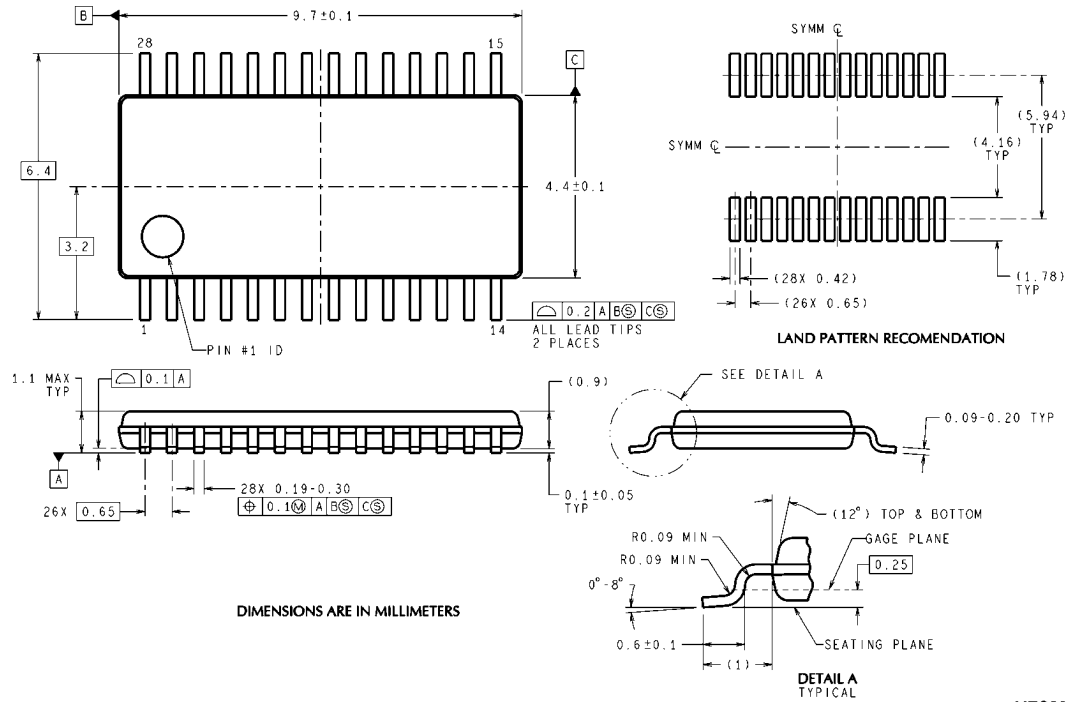
20098213

Peak-to-Peak Output Jitter at $V_{CM} = +2.9\text{V}$ vs. VID



20098214

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number MTC28
Order Number DS90LV110ATMT (Rail quantity of 48)
DS90LV110ATMTX (2500 piece Tape and Reel)

MTC28 (Rev D)

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adac	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation

For the most current product information visit us at www.national.com



**National Semiconductor
Americas Technical
Support Center**
Email: support@nsc.com
Tel: 1-800-272-9959

**National Semiconductor Europe
Technical Support Center**
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

**National Semiconductor Asia
Pacific Technical Support Center**
Email: ap.support@nsc.com

**National Semiconductor Japan
Technical Support Center**
Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated