JSMICRO SEMICONDUCTOR

BT148W-600R

1. General description

Planar passivated SCR with sensitive gate in a SOT223 (SC-73) surface mountable plastic package. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- Adapters
- Battery powered applications
- Industrial automation

4. Quick reference data

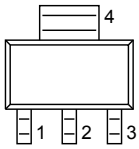
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	-	600	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	10	A
$I_{T(AV)}$	average on-state current	half sine wave; T_{sp} ≤ 112 °C; Fig. 1		-	-	0.6	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; T_{sp} ≤ 112 °C; Fig. 2; Fig. 3		-	-	1	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 9		-	50	200	µA

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 **SC-73 (SOT223)**	
2	A	anode		
3	G	gate		
4	mb	mb; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT148W-600R	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
BT148W-600R	BT148W 60

8. Limiting values

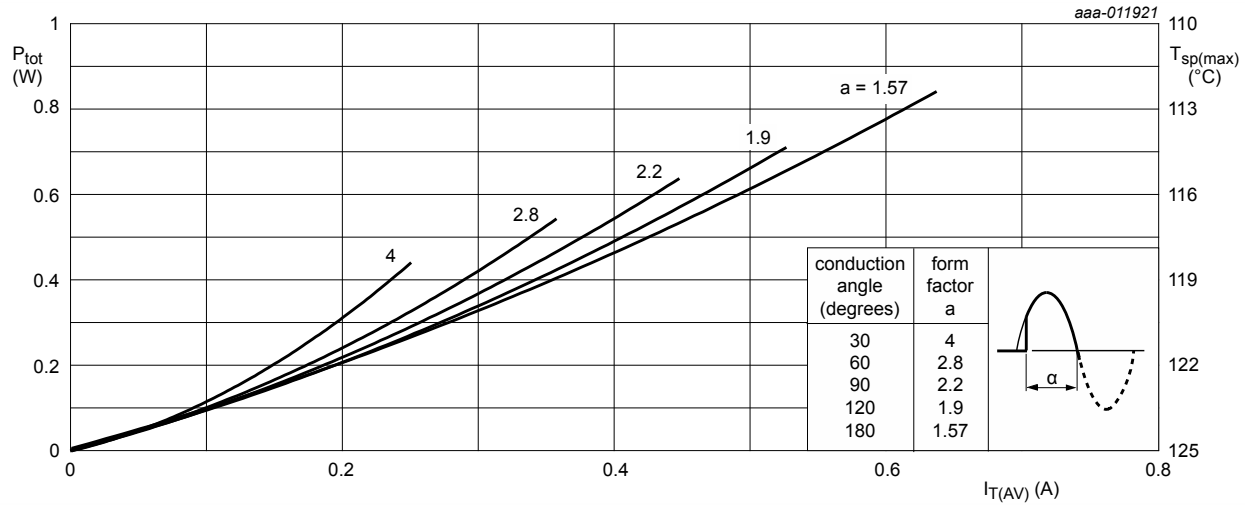
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 112$ °C; Fig. 1		-	0.6	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 112$ °C; Fig. 2; Fig. 3		-	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	10	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	11	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	0.5	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 400$ µA		-	100	A/µs
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	1.2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.12	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature		[2]	-	125	°C

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state.

[2] Operation above 110˚C may require the use of a gate to cathode resistor of 1kΩ or less.



α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

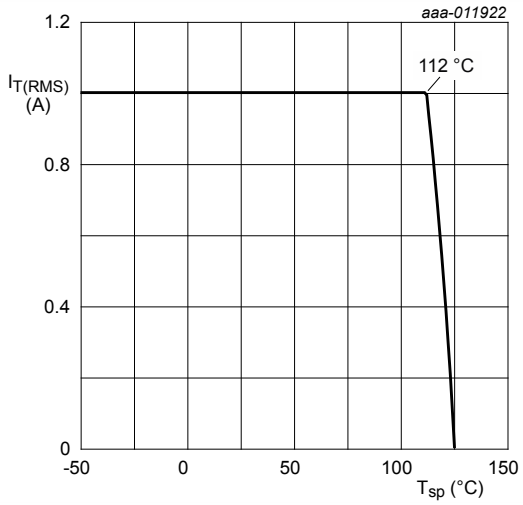
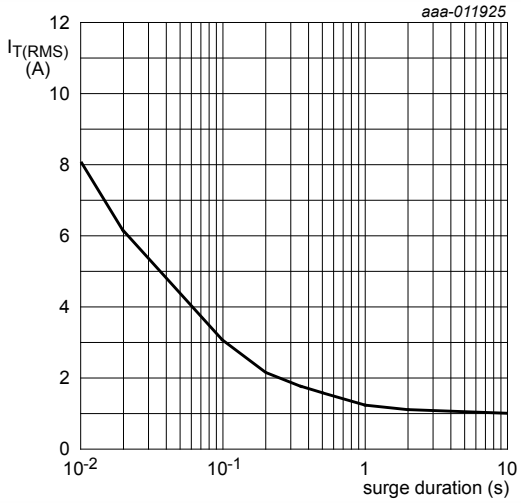
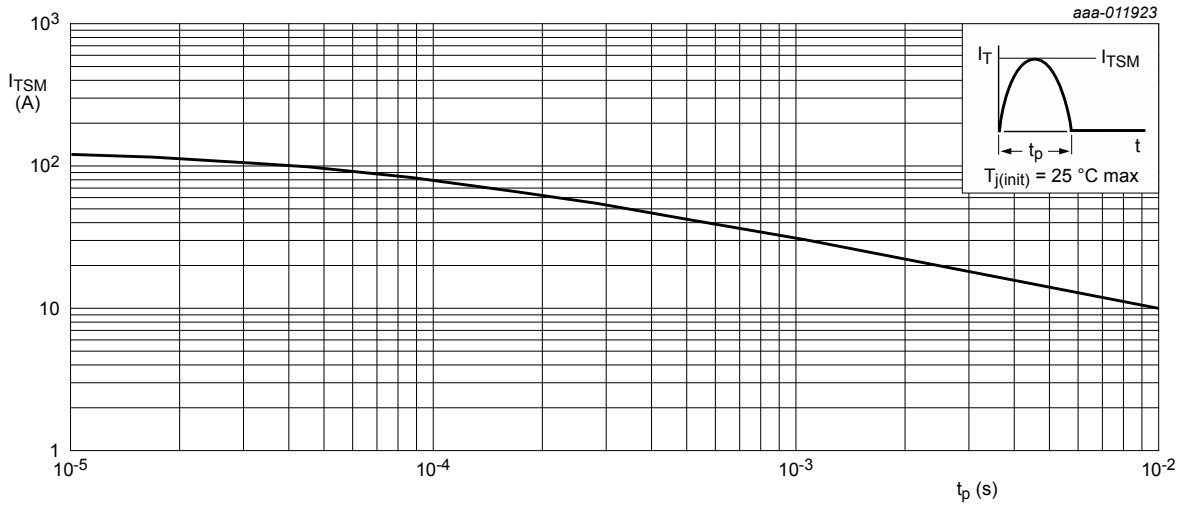


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values



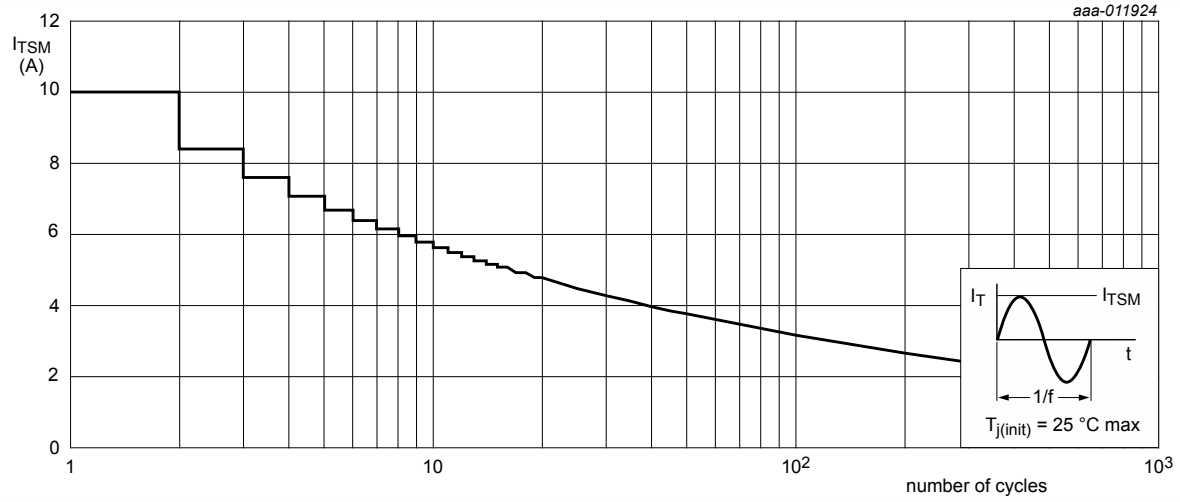
f = 50 Hz; T_{sp} = 112 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



$t_p \leq 10$ ms

Fig. 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



f = 50 Hz

Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 6		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted; pad area; Fig. 7		-	70	-	K/W
		printed circuit board mounted; minimum footprint; Fig. 8		-	156	-	K/W

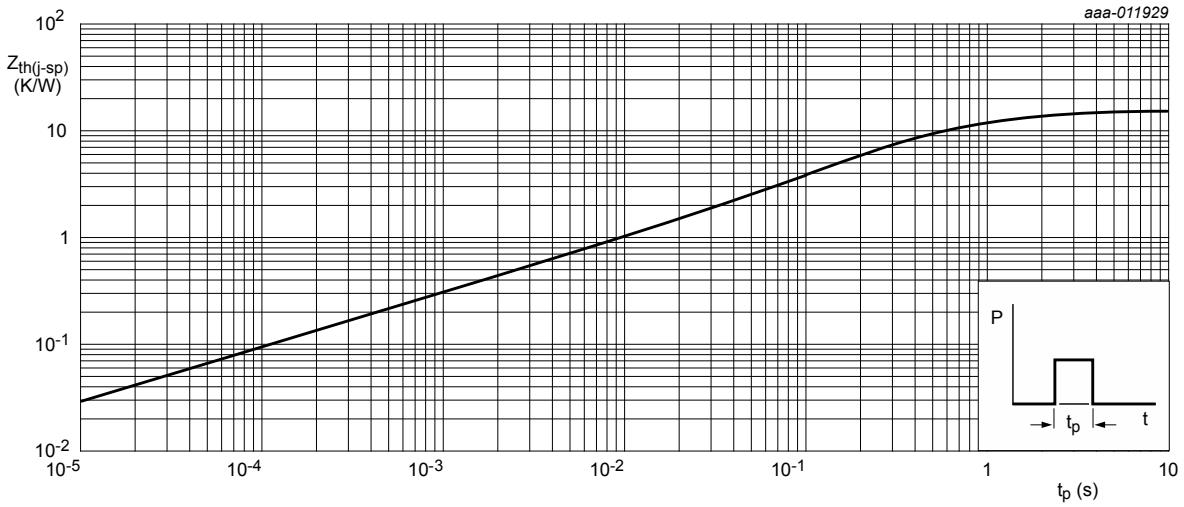
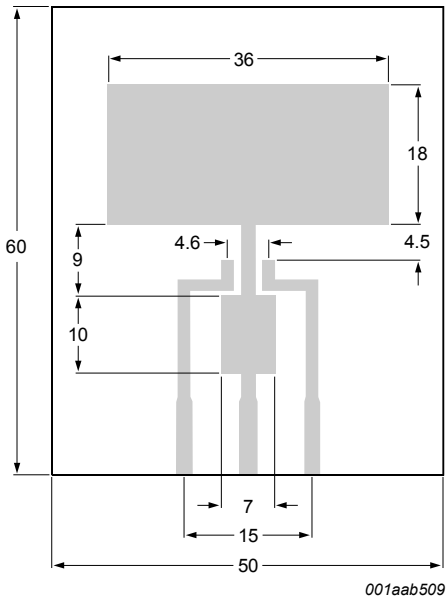


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width

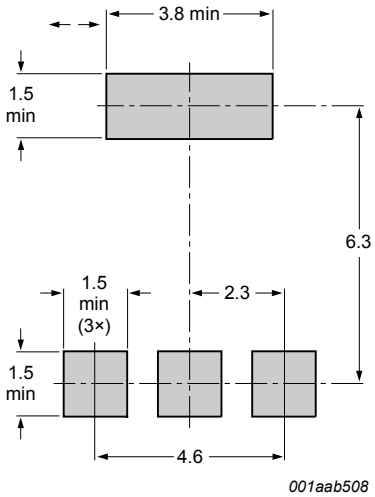


All dimensions are in mm

Printed circuit board:

FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 7. Printed circuit board pad area: SOT223



All dimensions are in mm

Fig. 8. Minimum footprint SOT223

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 9		-	50	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 10		-	0.17	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 11		-	0.1	6	mA
V_T	on-state voltage	I_T = 2 A; T_j = 25 °C; Fig. 12		-	1.3	1.5	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 13		-	0.4	1	V
		V_D = 600 V; I_T = 0.1 A; T_j = 125 °C; Fig. 13		0.1	0.2	-	V
I_D	off-state current	V_D = 600 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 600 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 14		-	50	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 4 A; V_D = 600 V; I_G = 5 mA; dI_G/dt = 0.2 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 402 V; T_j = 125 °C; I_{TM} = 4 A; V_R = 35 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 2 V/µs; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

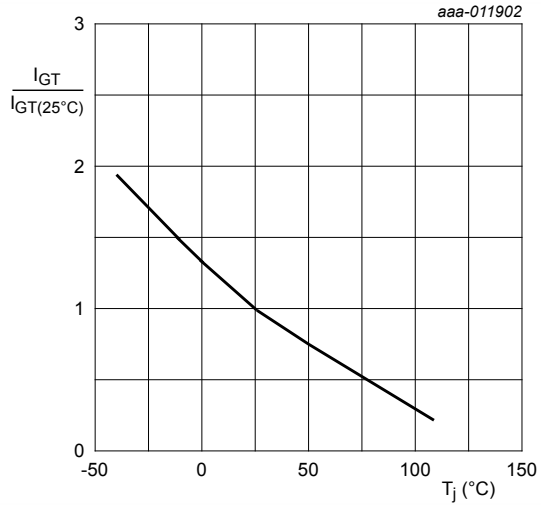
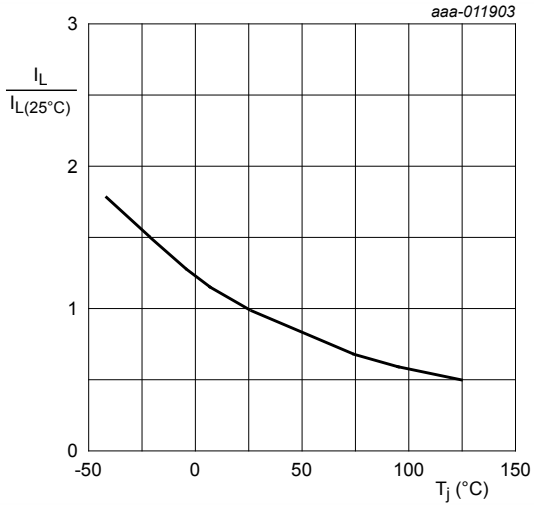
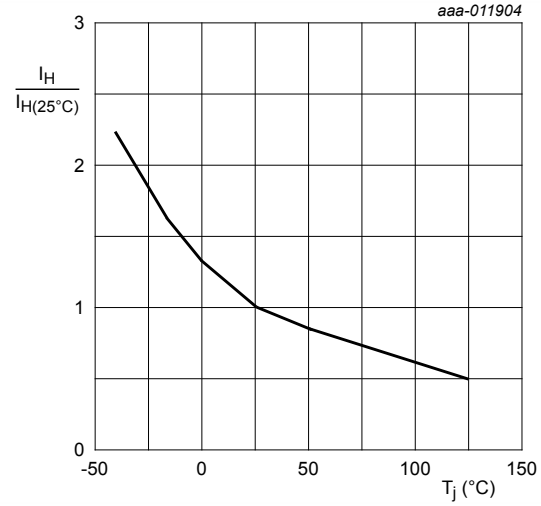


Fig. 9. Normalized gate trigger current as a function of junction temperature



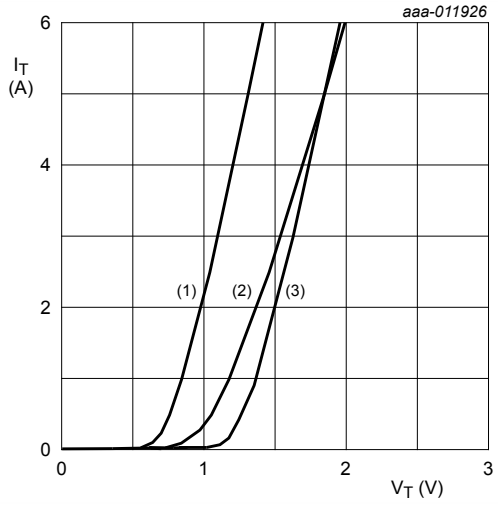
R_{GK} = 1 kΩ

Fig. 10. Normalized latching current as a function of junction temperature



R_{GK} = 1 kΩ

Fig. 11. Normalized holding current as a function of junction temperature



V_o = 1.107 V; R_s = 0.14 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

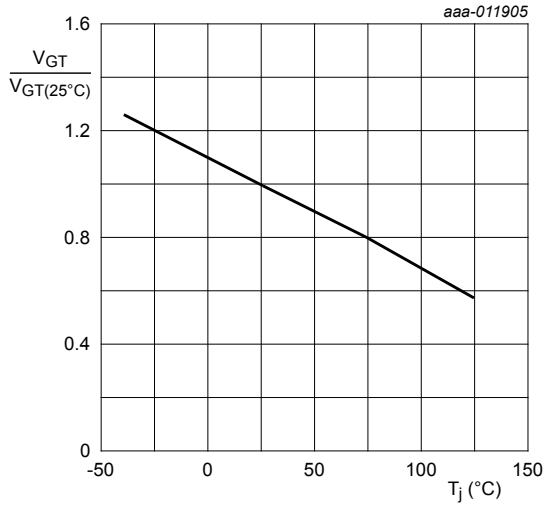
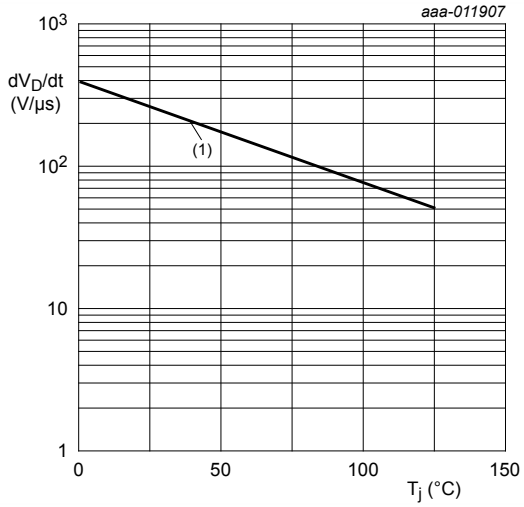


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

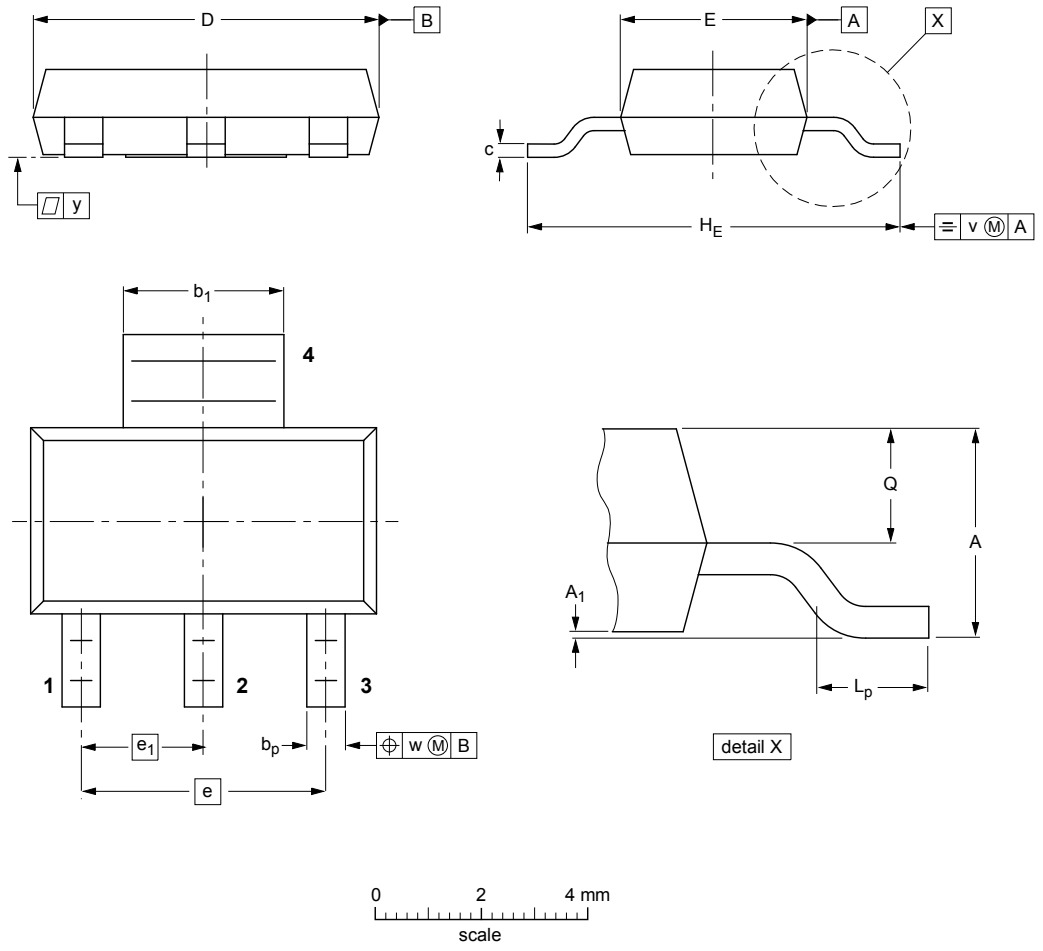


(1) R_{GK} = 100 Ω

Fig. 14. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig. 15. Package outline SC-73 (SOT223)

12. Soldering

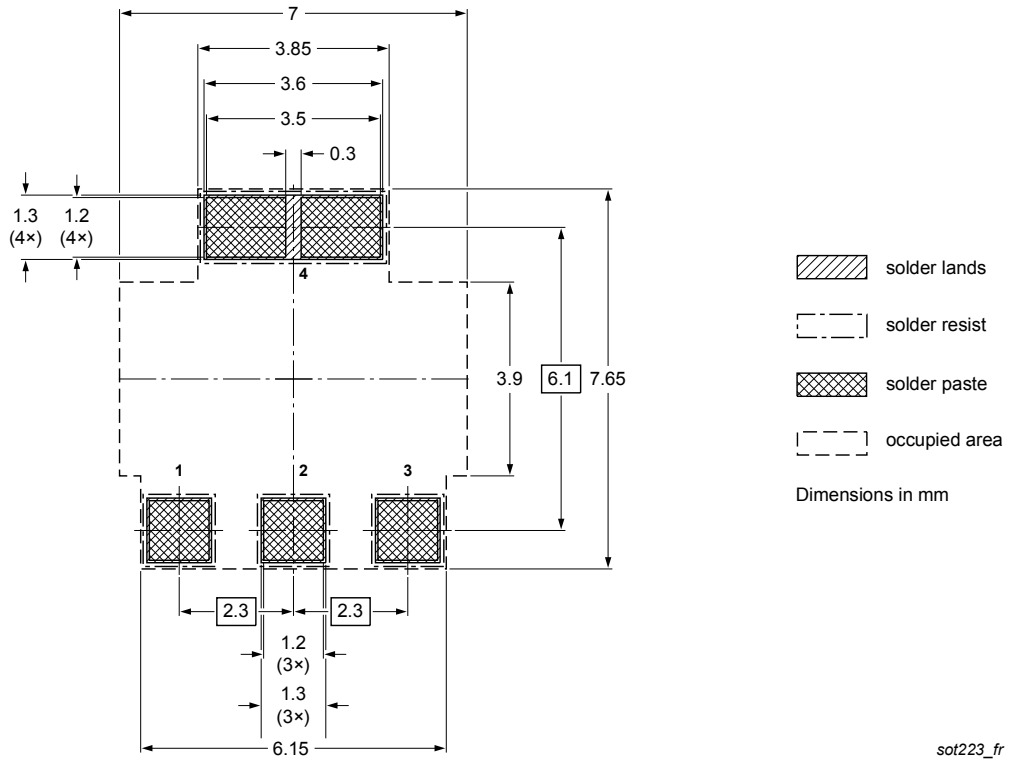


Fig. 16. Reflow soldering footprint for SC-73 (SOT223)

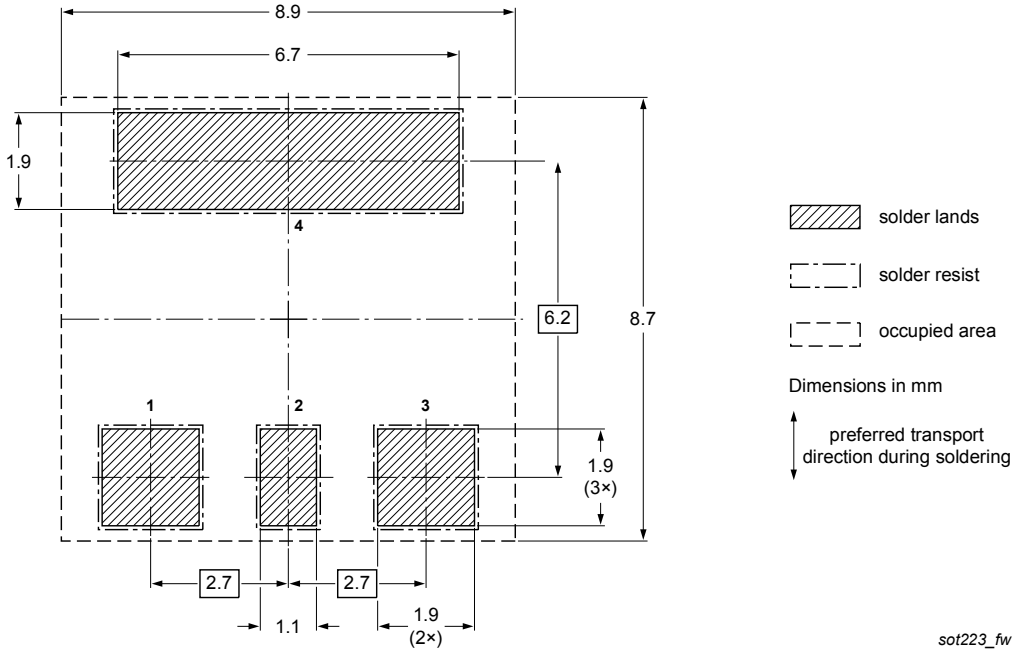


Fig. 17. Wave soldering footprint for SC-73 (SOT223)