JSMICRO SEMICONDUCTOR

BT151S-500R

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a TO252 (DPAK) surface mountable plastic package intended for use in applications requiring high bidirectional blocking voltage, High surge current capability and high thermal cycling performance.

2. Features and benefits

- High bidirectional blocking voltage capability
- High surge current capability
- High thermal cycling performance
- Surface mountable package

3. Applications

- Ignition circuits
- Motor control
- Protection circuits
- Voltage regulation

4. Quick reference data

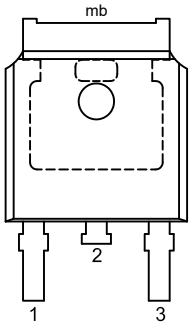
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq$ 103 °C; Fig. 1		-	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq$ 103 °C; Fig. 2; Fig. 3		-	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	120	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	-	132	A
T_j	junction temperature			-	-	125	°C
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 8		-	2	15	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 335 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 13		200	1000	-	V/µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{DM} = 335 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		50	130	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 **DPAK (TO252N)**	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151S-500R	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	TO252N

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	500	V
V_{RRM}	repetitive peak reverse voltage			-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq$ 103 °C; Fig. 1		-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq$ 103 °C; Fig. 2; Fig. 3		-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	120	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	132	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	72	A^2s
dI_T/dt	rate of rise of on-state current	I_G = 30 mA		-	50	A/µs
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

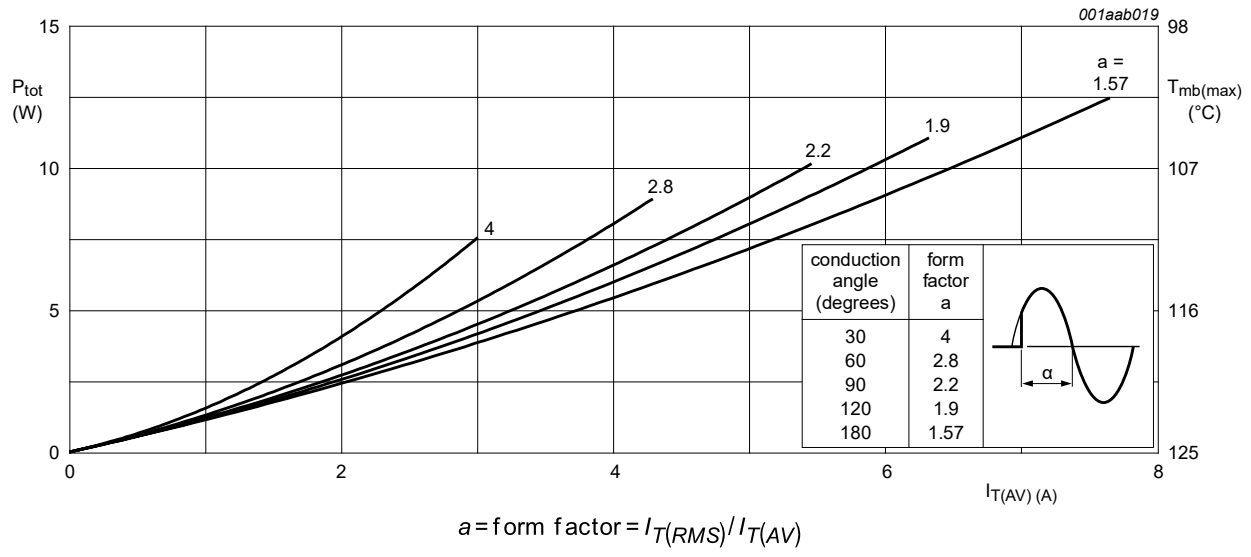


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

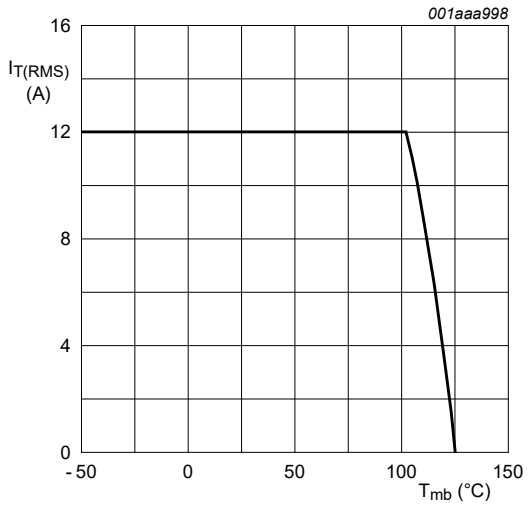
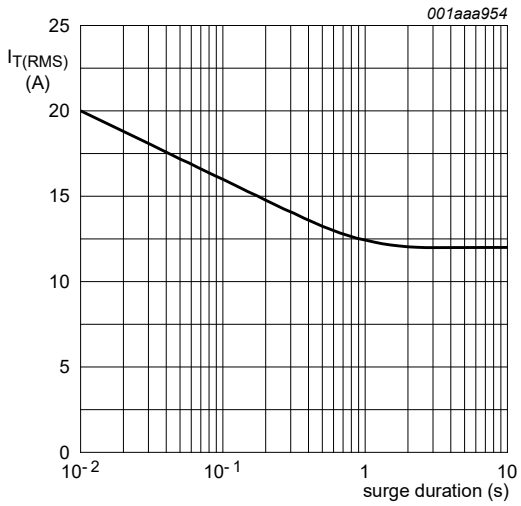
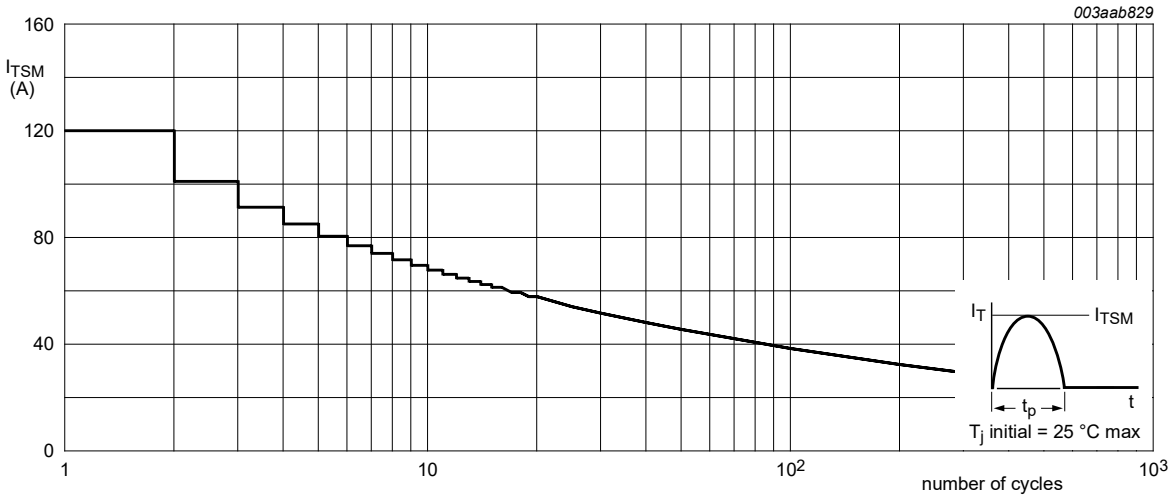


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



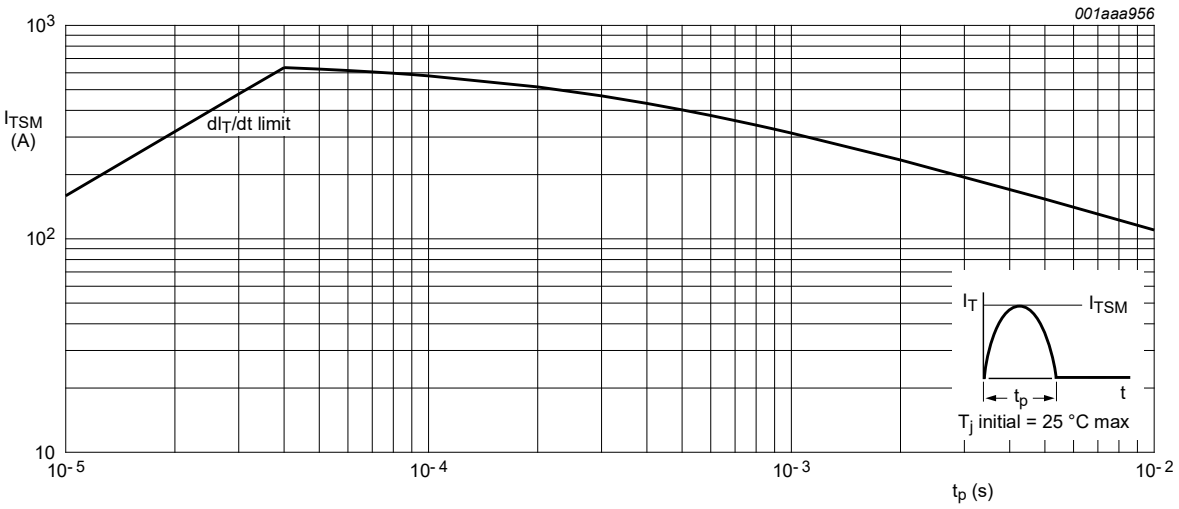
f = 50 Hz; T_{mb} = 103 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



f = 50 *Hz*

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p = 10\,ms$

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	1.8	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient free air	mounted on an FR4 printed-circuit board; Fig. 7		-	75	-	K/W

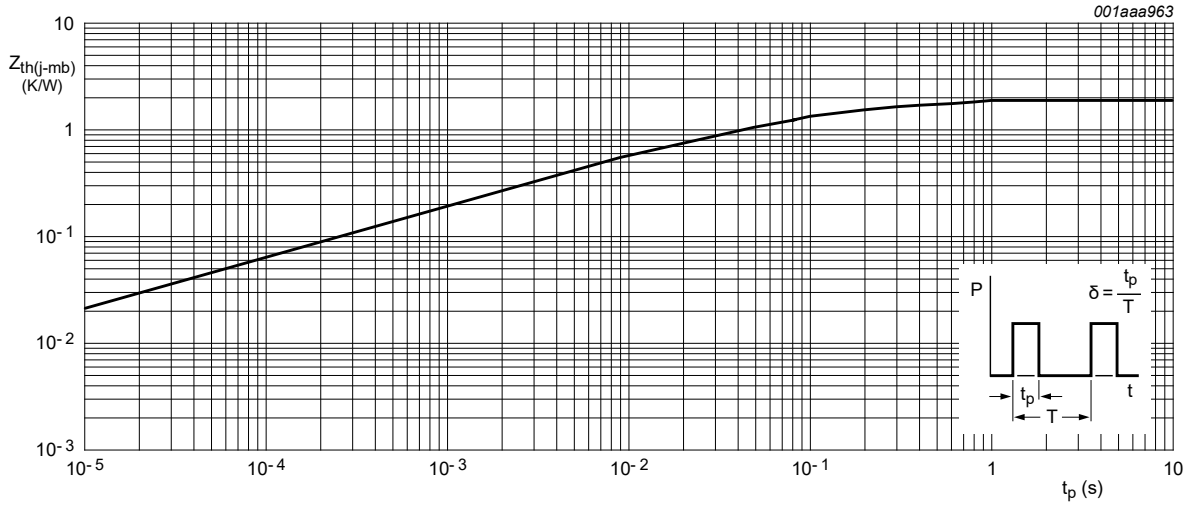
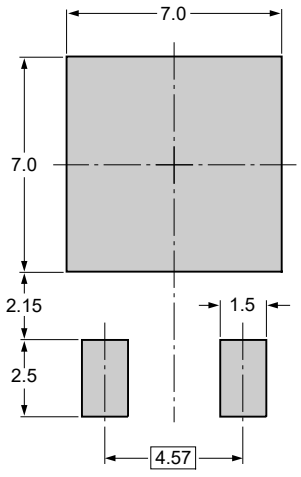


Fig. 6. Transient thermal impedance from junction to mounting base as as function of pulse width



001aab021 all dimensions are in mm

Fig. 7. Minimum footprint SOT428

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 8		-	2	15	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 9		-	10	40	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	7	20	mA
V_T	on-state voltage	I_T = 23 A; T_j = 25 °C; Fig. 11		-	1.4	1.75	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 12		-	0.6	1	V
		V_D = 500 V; I_T = 0.1 A; T_j = 125 °C; Fig. 12		0.25	0.4	-	V
I_D	off-state current	V_D = 500 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 500 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 335 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 13		200	1000	-	V/µs
		V_{DM} = 335 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		50	130	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 500 V; I_G = 0.1 A; dI_G/dt = 5 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 335 V; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; $R_{GK(ext)}$ = 100 Ω; (V_{DM} = 67% of V_{DRM})		-	70	-	µs

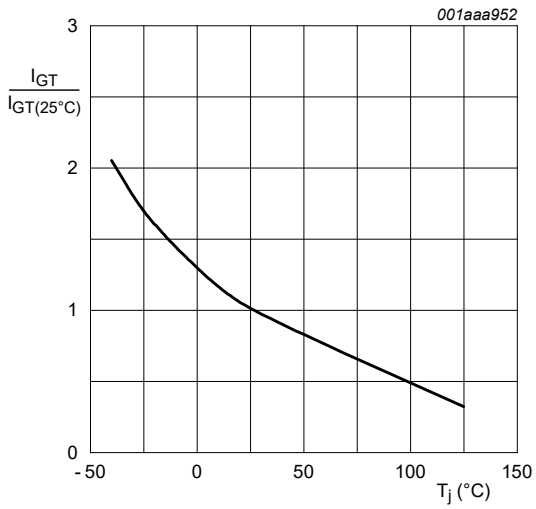


Fig. 8. Normalized gate trigger current as a function of junction temperature

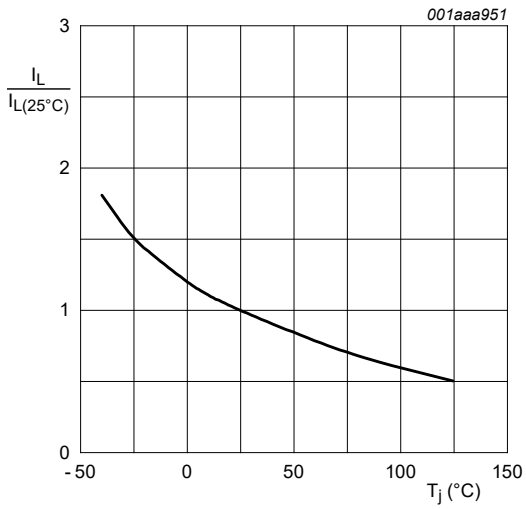


Fig. 9. Normalized latching current as a function of junction temperature

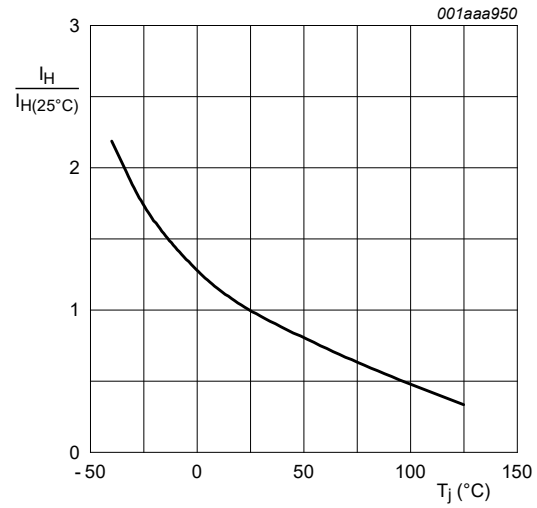
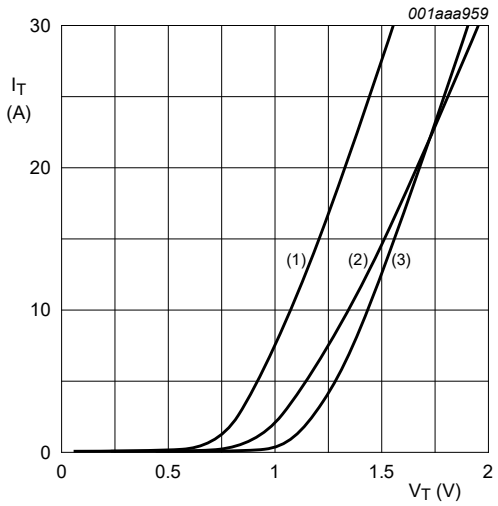


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.06 V; R_s = 0.0304 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

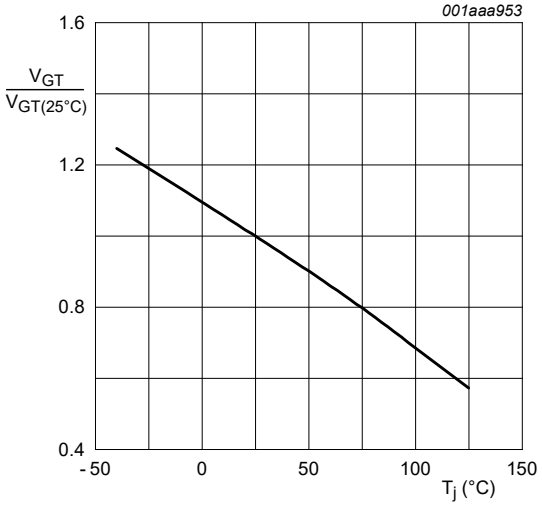
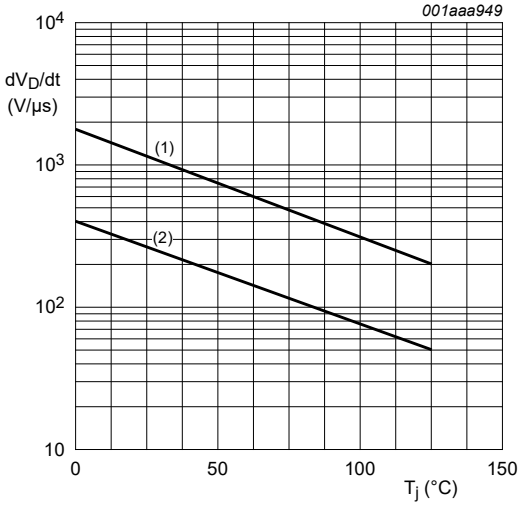


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

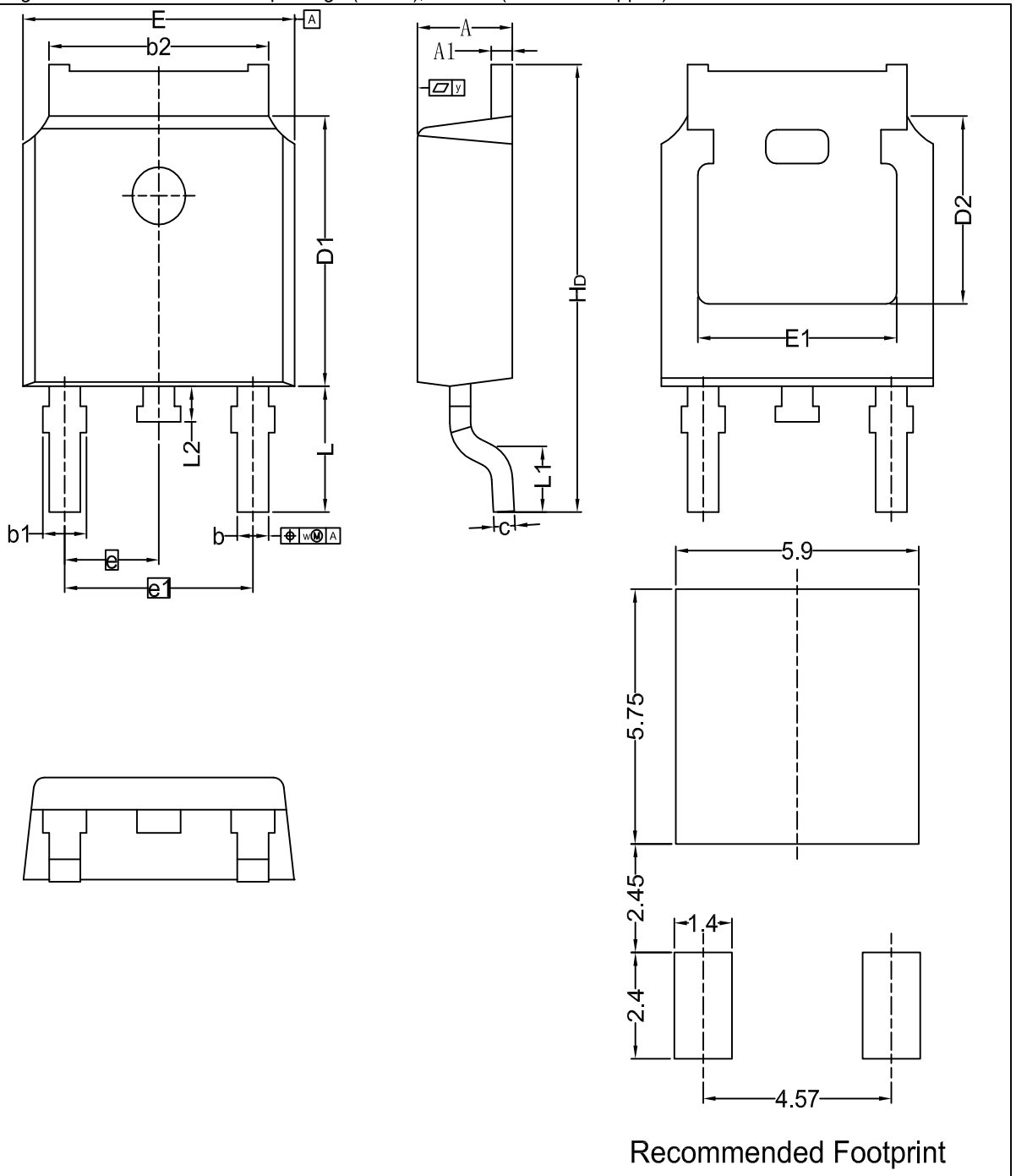


(1) R_{GK} = 100 Ω;
(2) gate open circuit

Fig. 13. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252



Unit	A	A1	b	b1	b2	c	D1	D2	E	E1	e	e1	H_D	L	L1	L2	w	y
min	2.22	0.46	0.71	0.72	5.00	0.20	5.98	4.00	6.47	4.45	2.285	4.57	9.60	2.90 (Ref.)	0.50	0.50	0.20	
mm nom																		
max	2.38	0.93	0.89	1.10	5.46	0.56	6.22	---	6.73	---			10.40		---	0.90		0.20

Fig. 14. Package outline DPAK (TO252N)