

GENERAL DESCRIPTION

Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

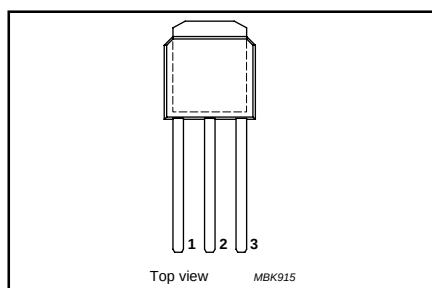
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
V_{DRM} , V_{RRM}	BT151U- Repetitive peak off-state voltages	500C 500	650C 650	800C 800	V
$I_{T(AV)}$	Average on-state current	7.5	7.5	7.5	A
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	100	100	100	A

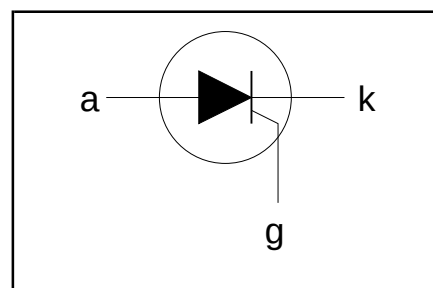
PINNING - SOT533, (I-PAK)

PIN NUMBER	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
V_{DRM} , V_{RRM}	Repetitive peak off-state voltages		-	-500C 500 ¹	-650C 650 ¹	-800C 800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 104^\circ\text{C}$	-	7.5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	12			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25^\circ\text{C}$ prior to surge	-	100			A
		$t = 10\text{ ms}$	-	110			A
		$t = 8.3\text{ ms}$	-	50			A ² s
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	50			A/μs
di_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20\text{ A}$; $I_G = 50\text{ mA}$; $di_G/dt = 50\text{ mA}/\mu\text{s}$	-	50			
I_{GM}	Peak gate current		-	2			A
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			°C
T_j	Junction temperature		-	125			°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	in free air	-	-	1.3	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	70	-	K/W

STATIC CHARACTERISTICS

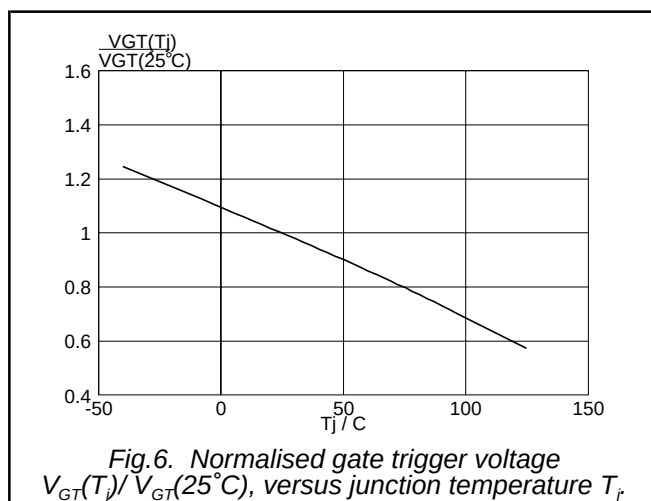
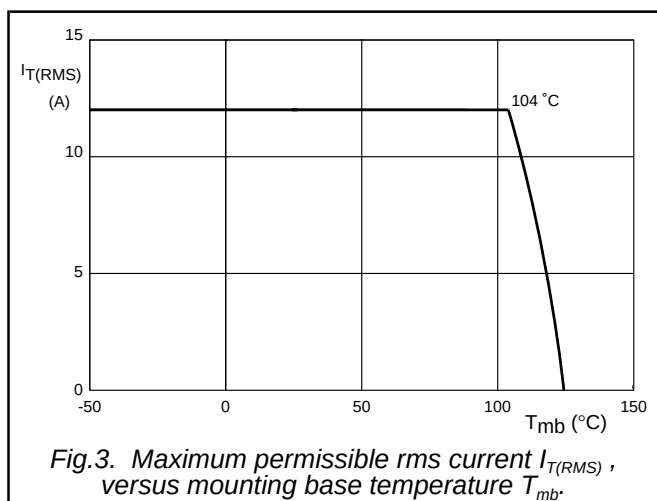
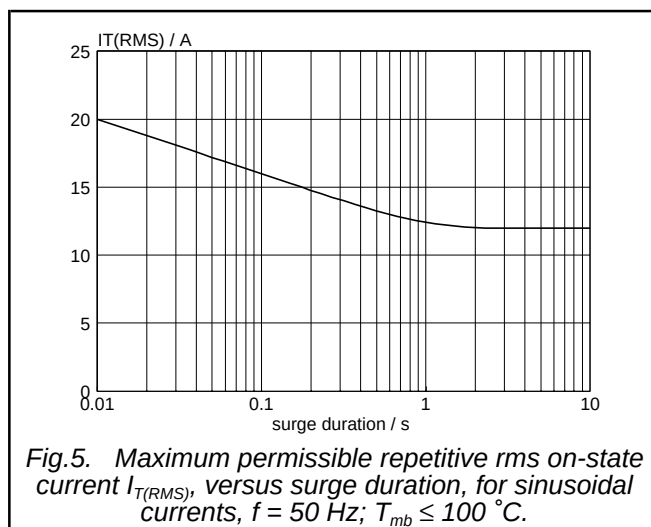
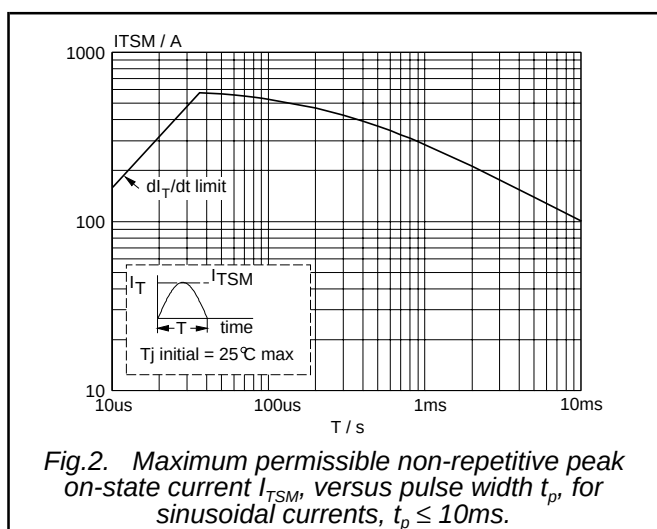
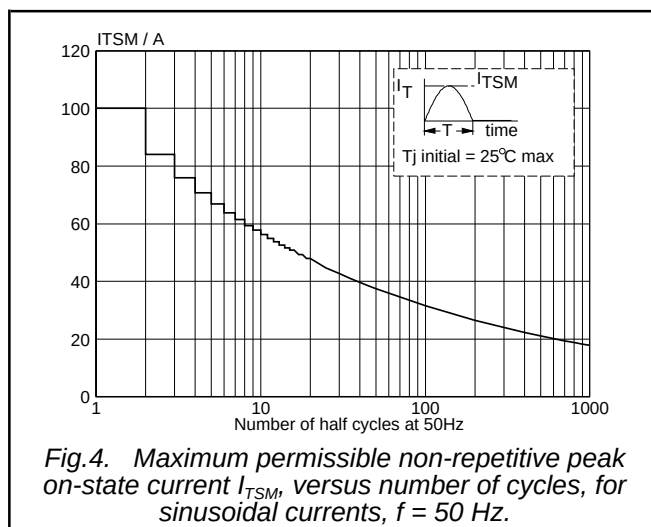
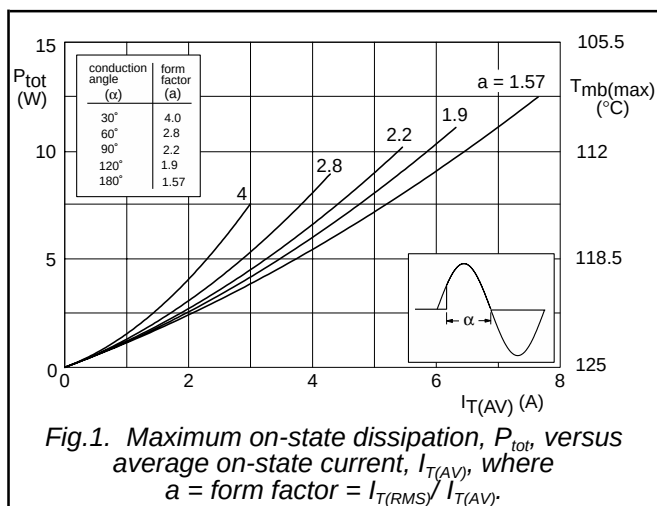
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

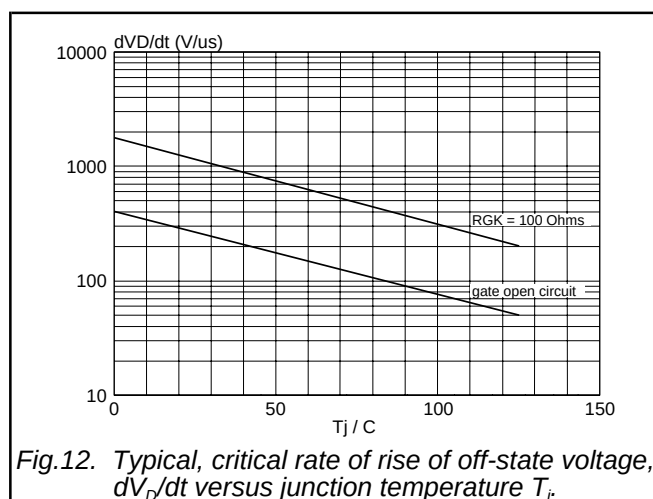
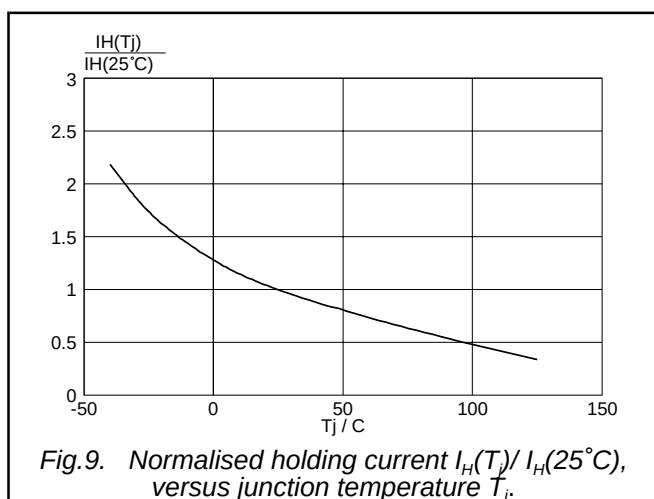
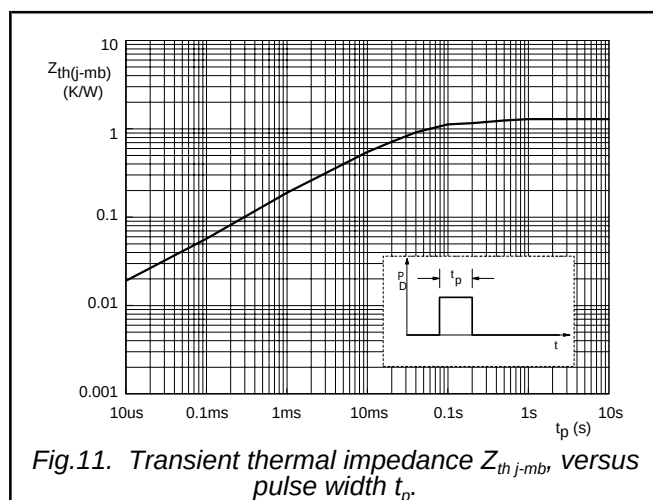
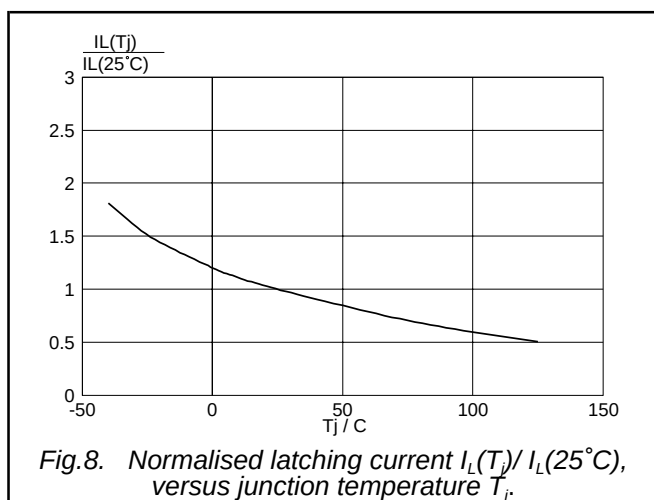
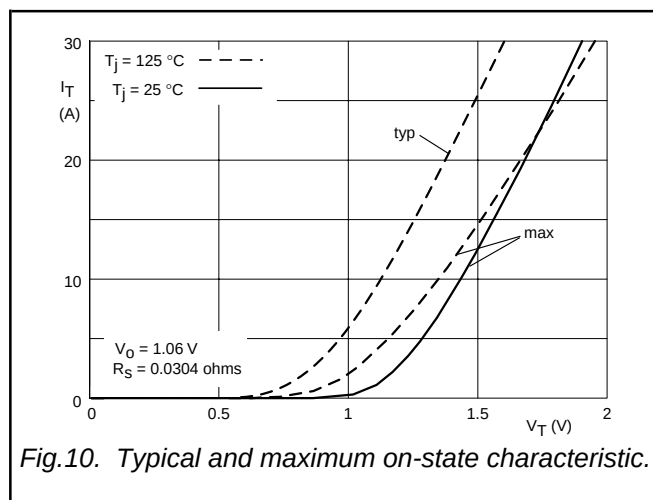
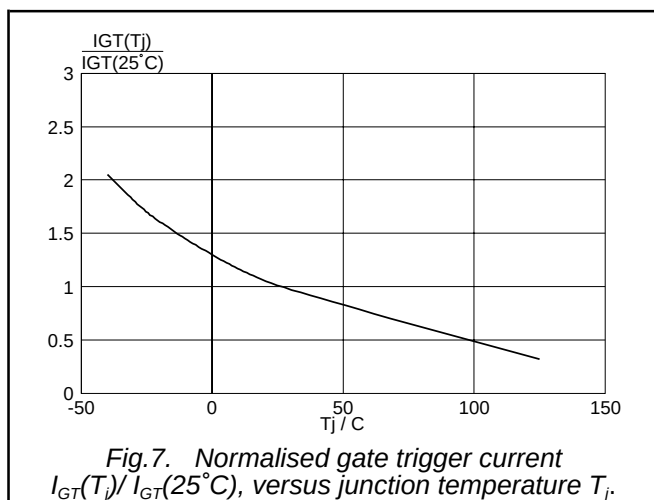
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	2	15	mA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	10	40	mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	7	20	mA
V_T	On-state voltage	$I_T = 23\text{ A}$	-	1.44	1.75	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.6	1.5	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}; I_T = 0.1\text{ A}; T_j = 125\text{ }^{\circ}\text{C}$	0.25	0.4	-	V
		$V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ }^{\circ}\text{C};$ exponential waveform				
t_{gt}	Gate controlled turn-on time	Gate open circuit $R_{GK} = 100\text{ }\Omega$	50	130	-	V/ μs
		$I_{TM} = 40\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$	200	1000	-	V/ μs
t_q	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}; T_j = 125\text{ }^{\circ}\text{C};$ $I_{TM} = 20\text{ A}; V_R = 25\text{ V}; dI_{TM}/dt = 30\text{ A}/\mu\text{s};$ $dV_D/dt = 50\text{ V}/\mu\text{s}; R_{GK} = 100\text{ }\Omega$	-	70	-	μs

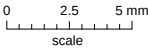
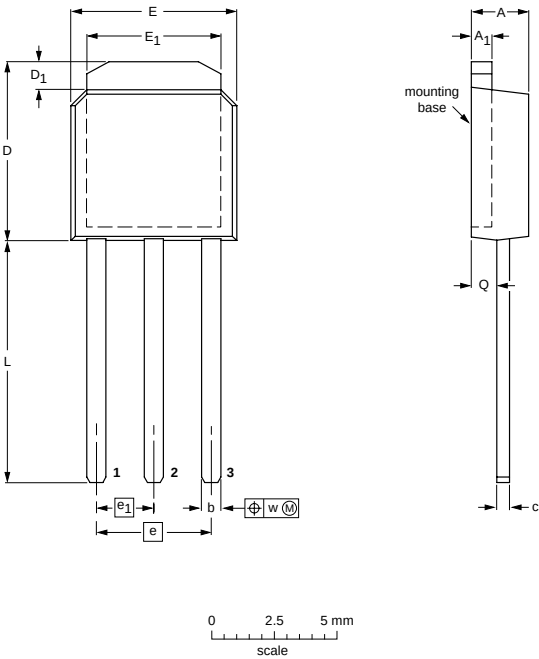




MECHANICAL DATA

Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line)

SOT533



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D	D ₁	E	E ₁	e	e ₁	L	Q
mm	2.38 2.22	0.89 0.71	0.89 0.71	0.56 0.46	7.28 6.94	1.06 0.96	6.73 6.47	5.36 5.26	4.57	2.285	9.8 9.4	1.00 1.10

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT533		TO-251				99-02-18

Fig.13. SOT533, (I-PAK). Pin 2 connected to mounting base.