

1. Product profile

1.1 General description

Passivated thyristors in a SOT186A full pack plastic package.

1.2 Features

- High thermal cycling performance
- High bidirectional blocking voltage capability
- Isolated mounting base.

1.3 Applications

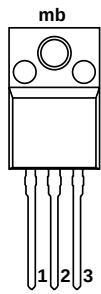
- Motor control
- Industrial and domestic lighting, heating and static switching.

1.4 Quick reference data

- $V_{\text{DRM}}, V_{\text{RRM}} \leq 800 \text{ V}$ (BT151X-800)
- $V_{\text{DRM}}, V_{\text{RRM}} \leq 650 \text{ V}$ (BT151X-650)
- $V_{\text{DRM}}, V_{\text{RRM}} \leq 500 \text{ V}$ (BT151X-500)
- $I_{\text{T(RMS)}} \leq 12 \text{ A}$
- $I_{\text{T(AV)}} \leq 7.5 \text{ A}$
- $I_{\text{TSM}} \leq 120 \text{ A}$.

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1	cathode (k)	 mb 1 2 3 SOT186A (TO-220)	 <i>sym037</i>
2	anode (a)		
3	gate (g)		
mb	mounting base; isolated		

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BT151X-500R	-	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; SOT186A	
BT151X-650R		3 lead TO-220 'full pack'	
BT151X-800C			

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM} , V_{RRM}	repetitive peak off-state voltage				
	BT151X-500R		[1]	500	V
	BT151X-650R		[1]	650	V
	BT151X-800C		-	800	V
$I_{T(AV)}$	average on-state current	half sinewave; $T_{hs} \leq 69^\circ\text{C}$; Figure 1	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; Figure 4 and Figure 5	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sinewave; $T_j = 25^\circ\text{C}$ prior to surge; Figure 2 and Figure 3			
		$t = 10\text{ ms}$	-	120	A
		$t = 8.3\text{ ms}$	-	132	A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	72	A^2s
di_T/dt	repetitive rate of rise of on-state current after triggering	$I_{TM} = 20\text{ A}$; $I_G = 50\text{ mA}$; $dI_G/dt\ 50\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	+150	$^\circ\text{C}$
T_j	junction temperature		-	125	$^\circ\text{C}$

- [1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .

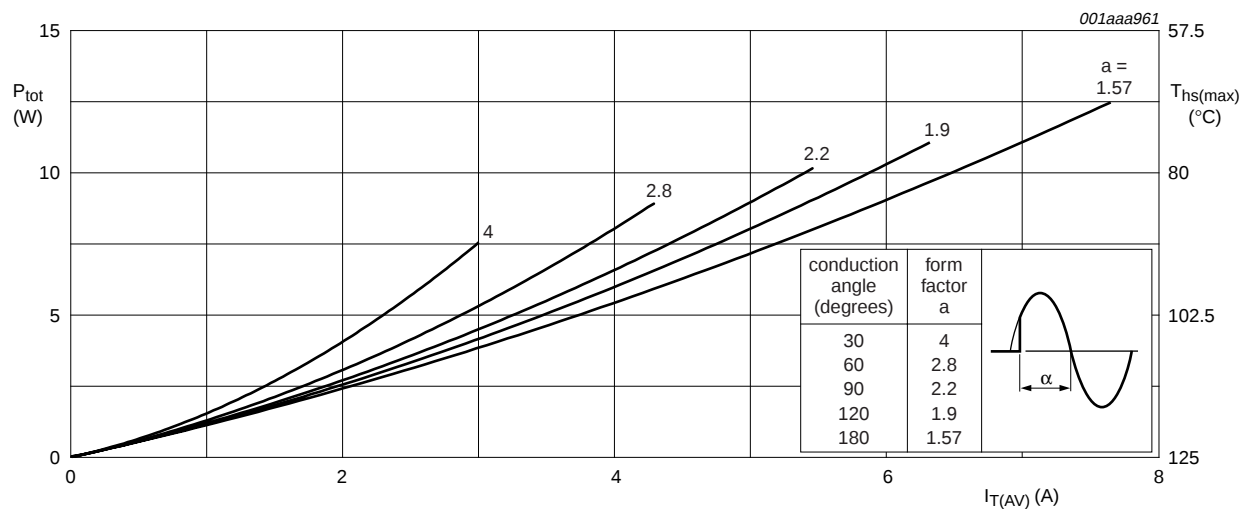
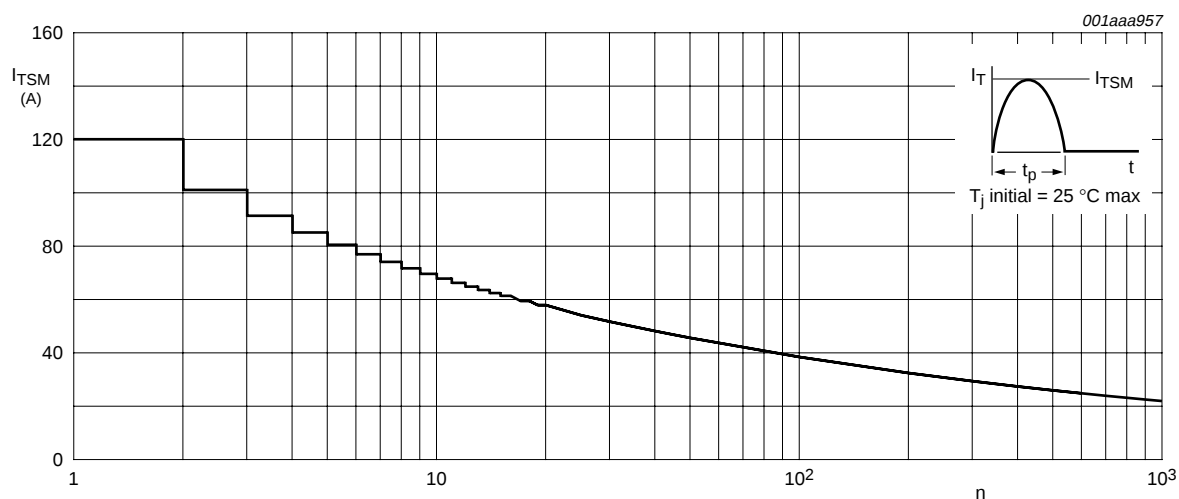
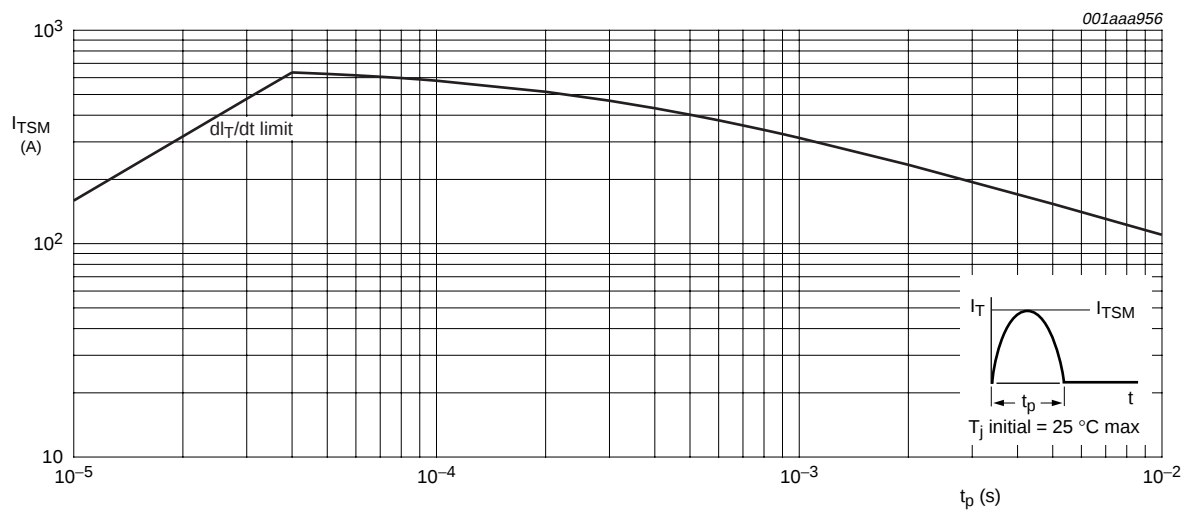


Fig 1. Total power dissipation as a function of average on-state current; maximum values.



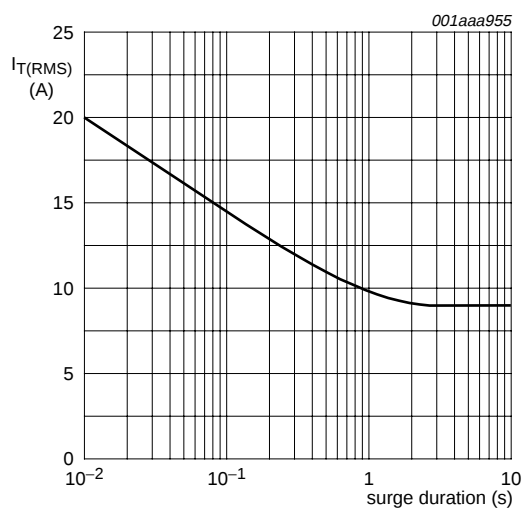
$f = 50 \text{ Hz.}$

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values.



$t_p \leq 10 \text{ ms.}$

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values.



$f = 50 \text{ Hz; } T_{hs} \leq 87^\circ\text{C.}$

Fig 4. RMS on-state current as a function of surge duration; maximum values.

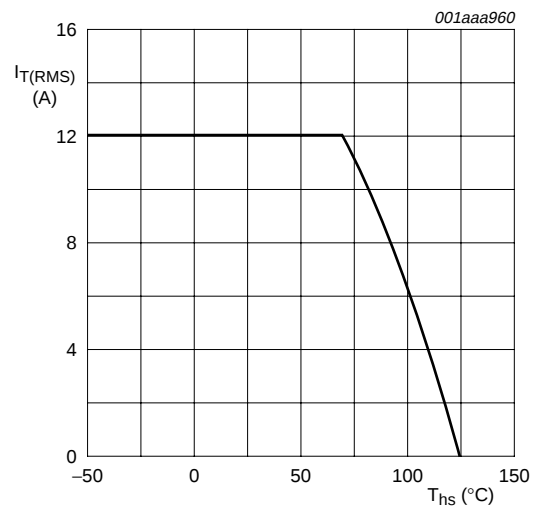
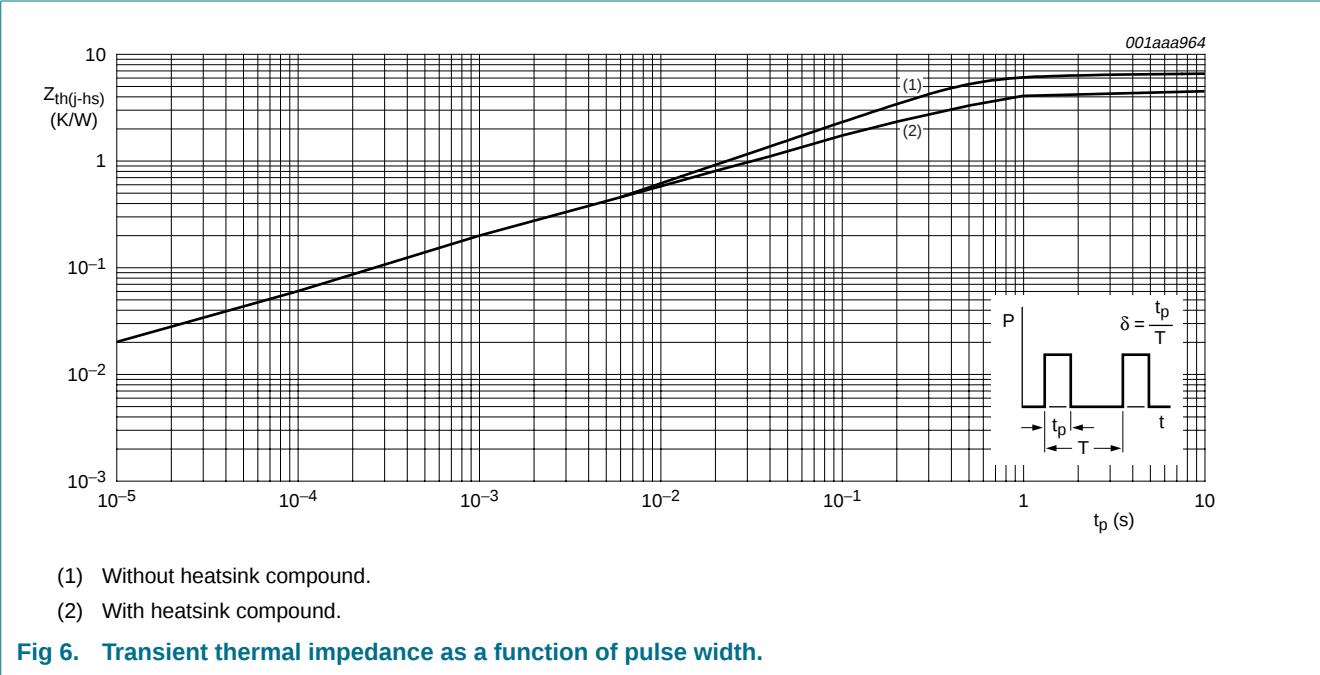


Fig 5. RMS on-state current as a function of heatsink temperature; maximum values.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-hs)}$	thermal resistance from junction to heatsink	Figure 6			
		with heatsink compound	-	4.5	K/W
		without heatsink compound	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	55	-	K/W



6. Isolation characteristics

Table 5: Isolation limiting values and characteristics

$T_{hs} = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{isol}	RMS isolation voltage from all three terminals to external heatsink	$f = 50$ to 60 Hz; sinusoidal waveform; R.H. $\leq 65\%$; clean and dust free	-	2500	V
C_{isol}	capacitance from pin 2 to external heatsink	$f = 1$ MHz	10	-	pF

7. Characteristics

Table 6: Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; Figure 8	-	2	15	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$; Figure 10	-	10	40	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$; Figure 11	-	7	20	mA
V_T	on-state voltage	$I_T = 23\text{ A}$; Figure 9	-	1.4	1.75	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; Figure 7	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^{\circ}\text{C}$	0.25	0.4	-	V
I_D, I_R	off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$; $T_j = 125\text{ }^{\circ}\text{C}$; exponential waveform; Figure 12				
		gate open circuit	50	130	-	V/ μs
		$R_{GK} = 100\text{ }\Omega$	200	1000	-	V/ μs
t_{gt}	gate controlled turn-on time	$I_{TM} = 40\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs
t_q	circuit commuted turn-on time	$V_D = 67\% V_{DRM(max)}$; $T_j = 125\text{ }^{\circ}\text{C}$; $I_{TM} = 20\text{ A}$; $V_R = 25\text{ V}$; $dI_{TM}/dt = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 50\text{ V}/\mu\text{s}$; $R_{GK} = 100\text{ }\Omega$	-	70	-	μs

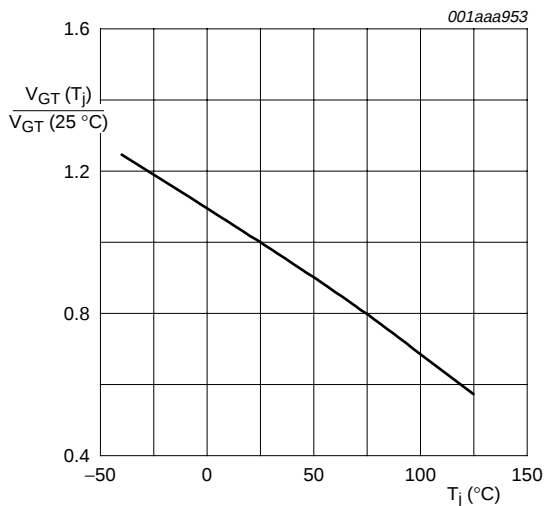


Fig 7. Normalized gate trigger voltage as a function of junction temperature.

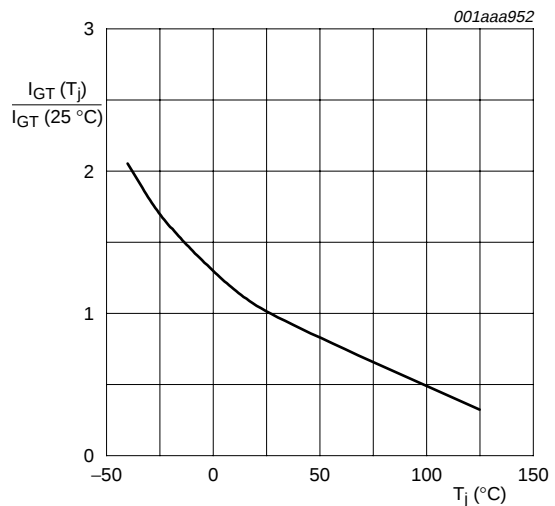
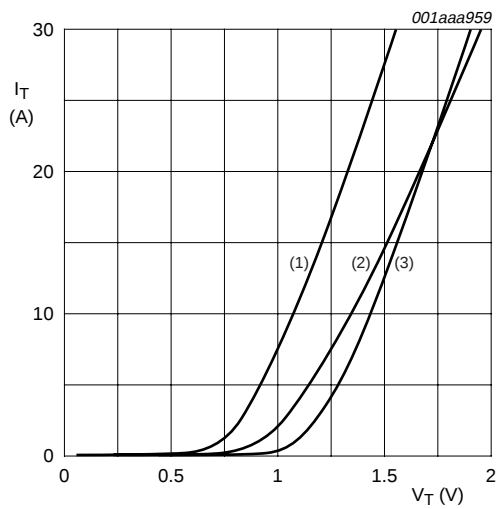


Fig 8. Normalized gate trigger current as a function of junction temperature.



$V_O = 1.06 \text{ V.}$

$R_S = 0.0304 \text{ } \Omega.$

- (1) $T_j = 125 \text{ } ^\circ\text{C}$; typical values.
- (2) $T_j = 125 \text{ } ^\circ\text{C}$; maximum values.
- (3) $T_j = 25 \text{ } ^\circ\text{C}$; maximum values.

Fig 9. On-state current characteristics.

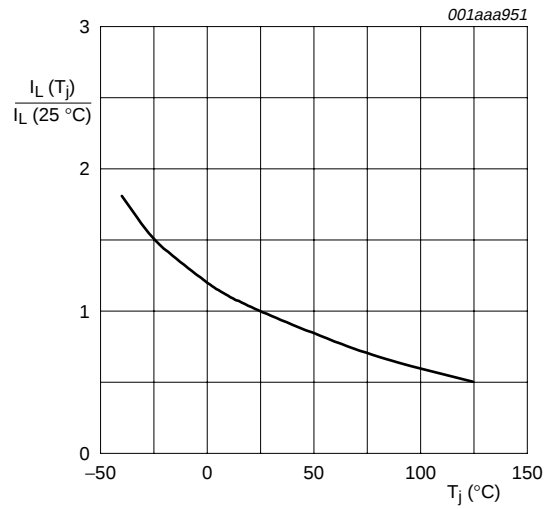


Fig 10. Normalized latching current as a function of junction temperature.

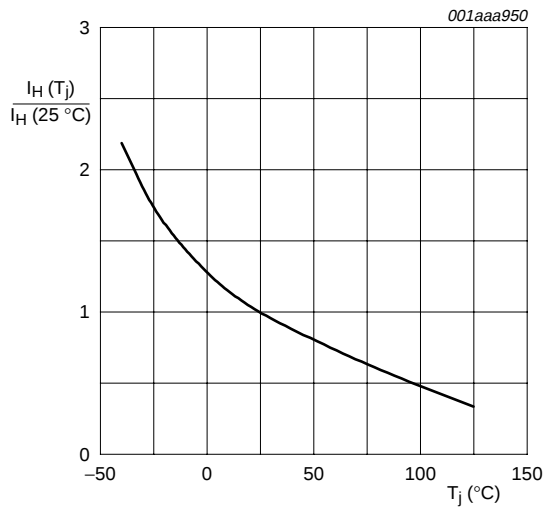
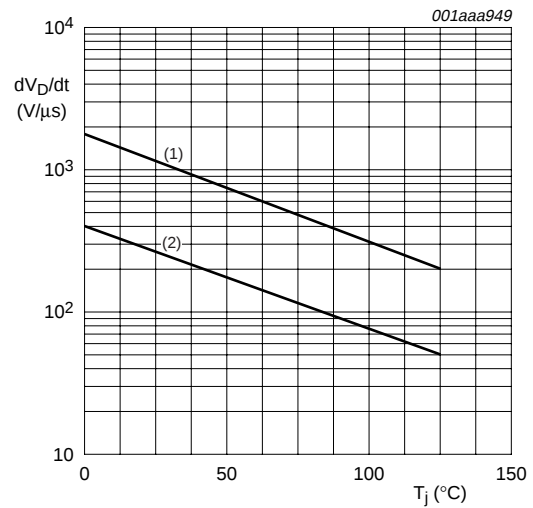


Fig 11. Normalized holding current as a function of junction temperature.



- (1) $R_{GK} = 100 \text{ } \Omega.$
- (2) Gate open circuit.

Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values.

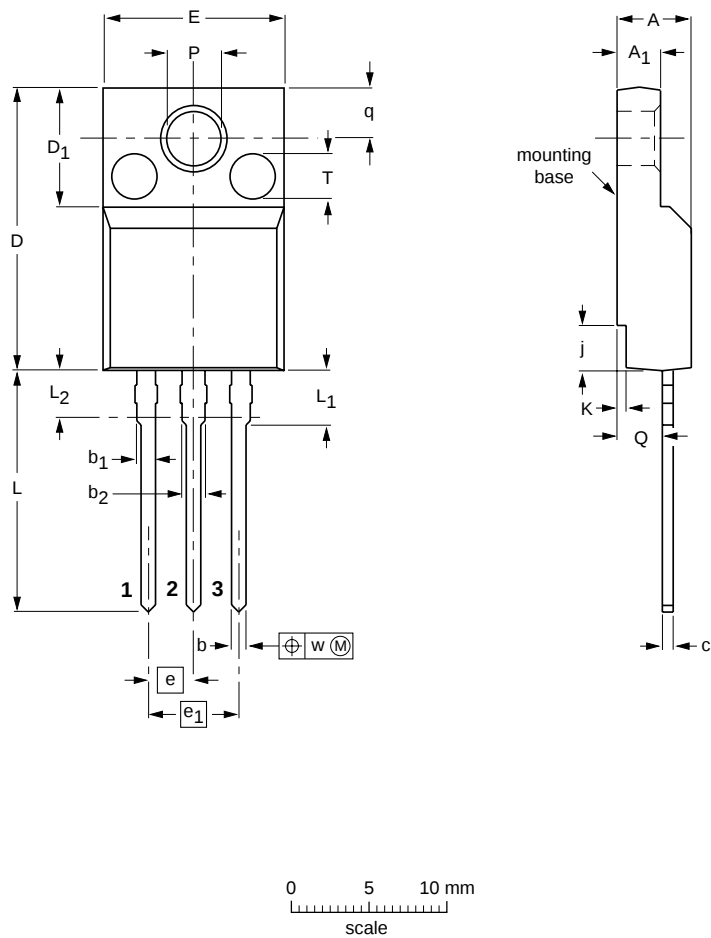
8. Package information

Epoxy meets requirements of UL94 V-0 at $\frac{1}{8}$ inch.

9. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	T ⁽²⁾	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

- Notes
1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
 2. Both recesses are $\varnothing 2.5 \times 0.8$ max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				02-03-12- 02-04-09