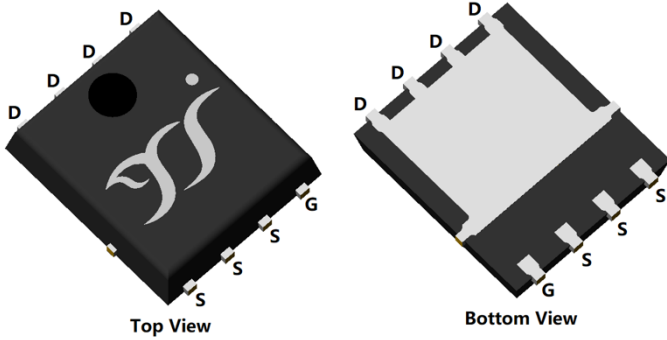
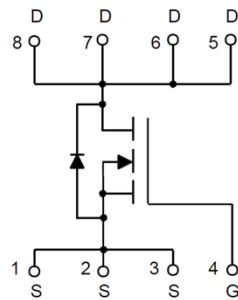


N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L



Product Summary

- V_{DS} 100V
- I_D 18A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <60mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <70mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Backlighting

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	18	A
	$T_C=100^\circ\text{C}$		11.4	
Pulsed Drain Current ^A		I_{DM}	75	A
Total Power Dissipation @ $T_C=25^\circ\text{C}$		P_D	45	W
Single Pulse Avalanche Energy ^B		E_{AS}	12.5	mJ
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	2.8	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG18N10A	F1	YJG18N10A	5000	10000	100000	13" reel



YJG18N10A

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.1	1.8	3.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =8A		49	60	mΩ
		V _{GS} = 4.5V, I _D =8A		52	70	
Diode Forward Voltage	V _{SD}	I _S =18A, V _{GS} =0V		0.8	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	1.2	-	Ω
Maximum Body-Diode Continuous Current	I _S				18	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		2071		pF
Output Capacitance	C _{oss}			73		
Reverse Transfer Capacitance	C _{rss}			54		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =10A		51.4		nC
Gate-Source Charge	Q _{gs}			9.1		
Gate-Drain Charge	Q _{gd}			11.5		
Reverse Recovery Chrage	Q _{rr}	I _F =10A, di/dt=100A/us		35.3		ns
Reverse Recovery Time	t _{rr}			38		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =2A R _{GEN} =3Ω		10		
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			42		
Turn-off fall Time	t _f			26		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. T_J=25℃, V_{DD}=50V, V_{GS}=10V, L=1mH, I_{AS}=5A.

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

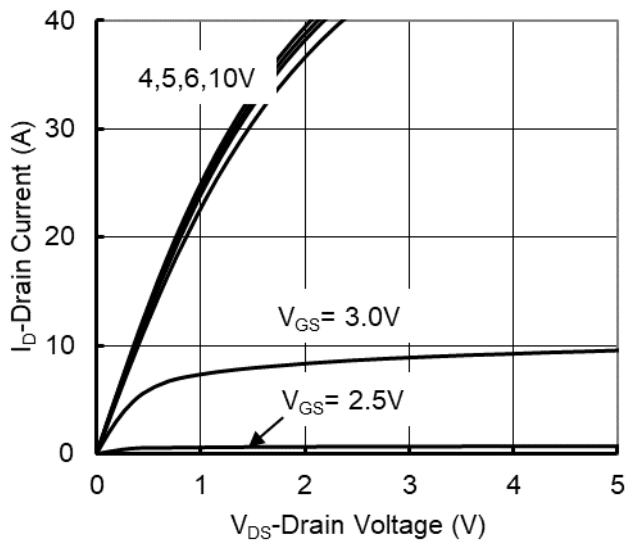


Figure 1. Output Characteristics

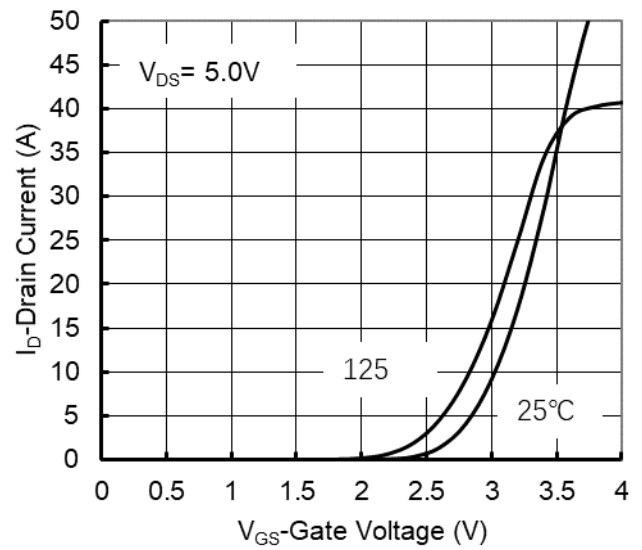


Figure 2. Transfer Characteristics

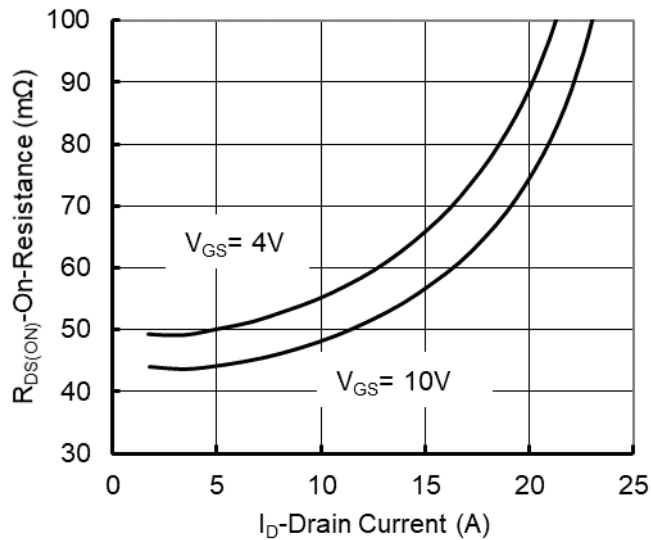


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

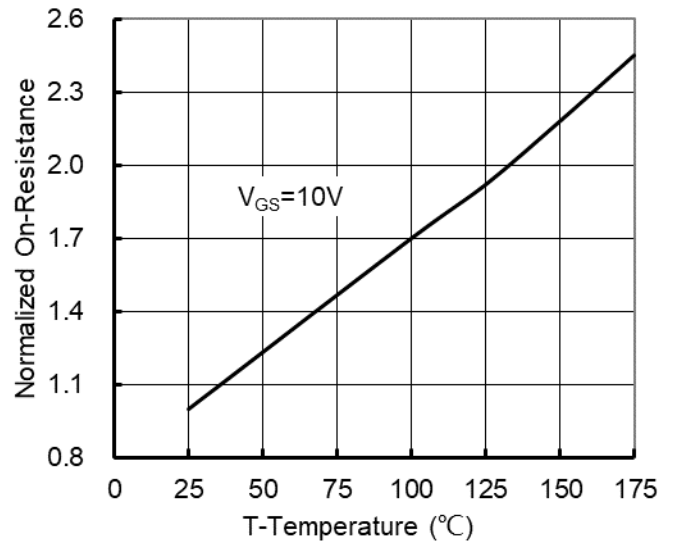


Figure 4. On-Resistance vs. Junction Temperature

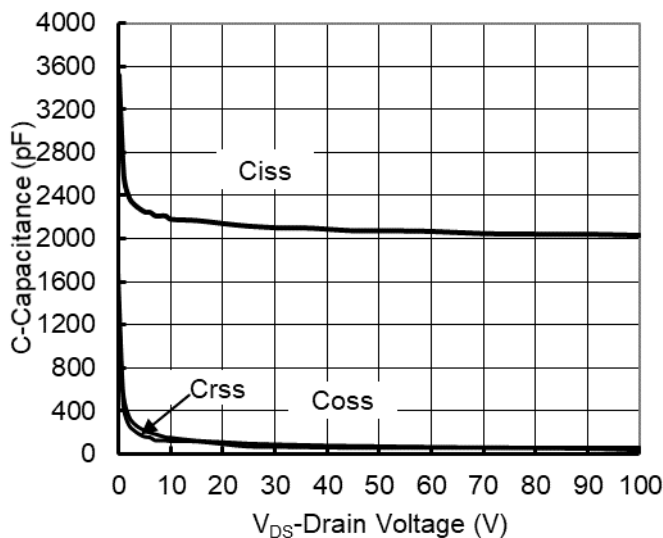


Figure 5. Capacitance Characteristics

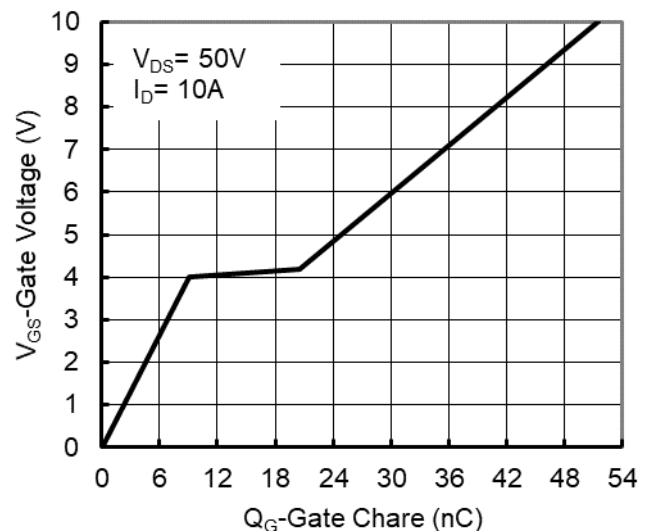


Figure 6. Gate Charge

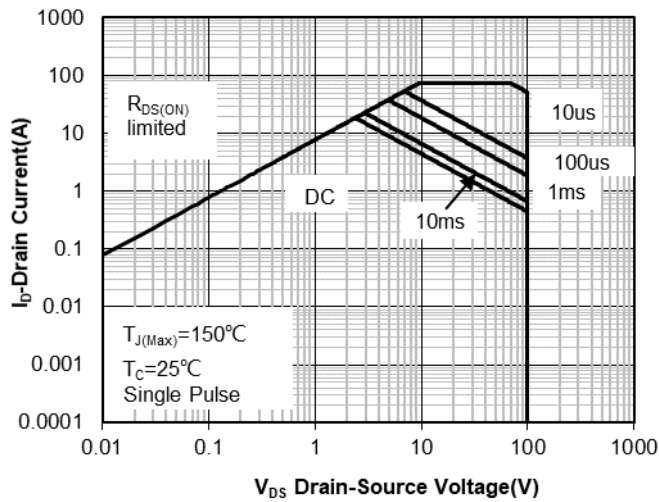


Figure 7. Safe Operation Area

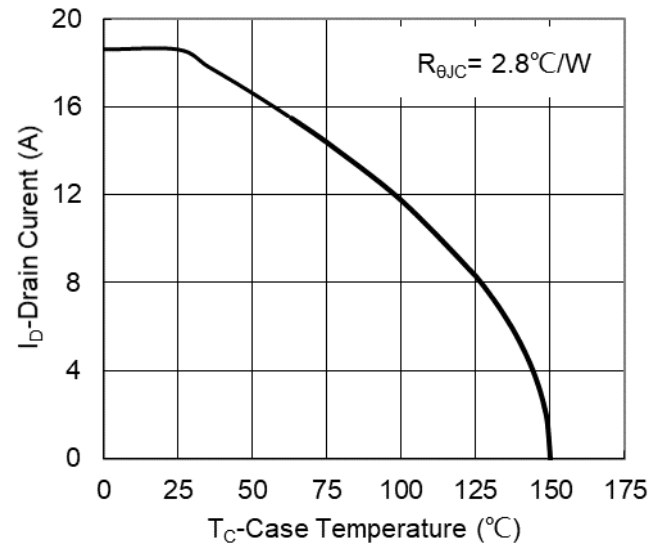


Figure 8. Maximum Continuous Drain Current vs Case Temperature

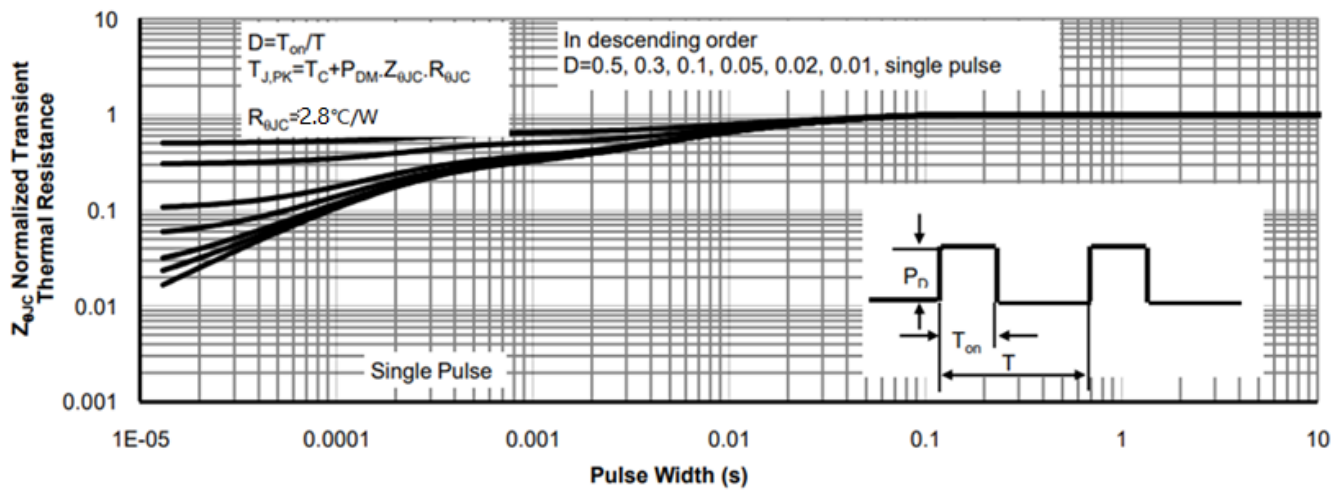
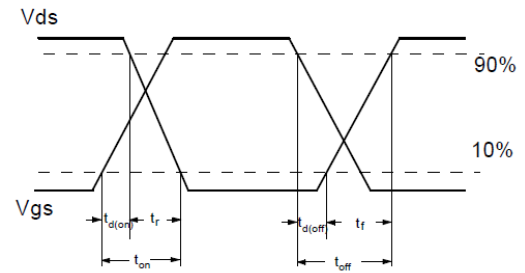
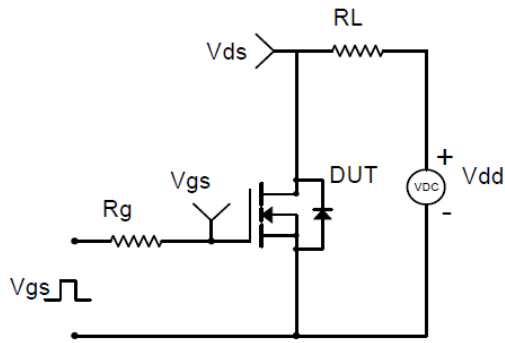
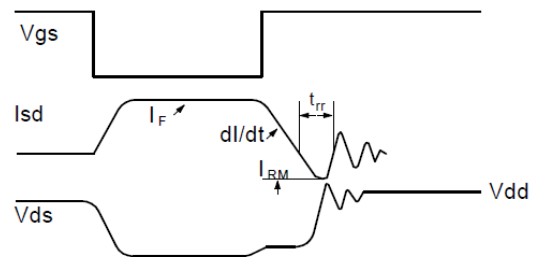
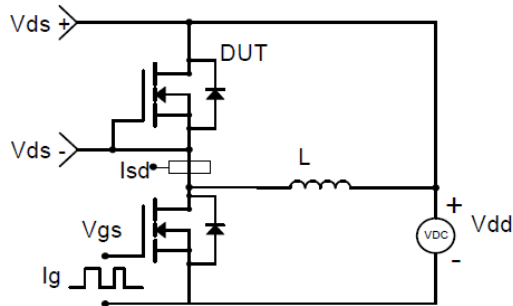


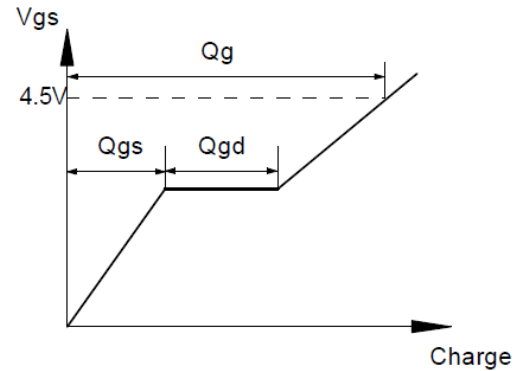
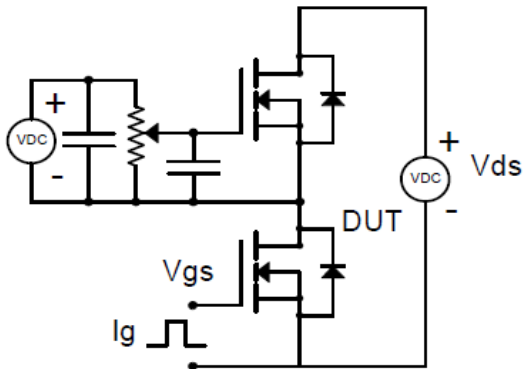
Figure 9. Normalized Maximum Transient Thermal Impedance



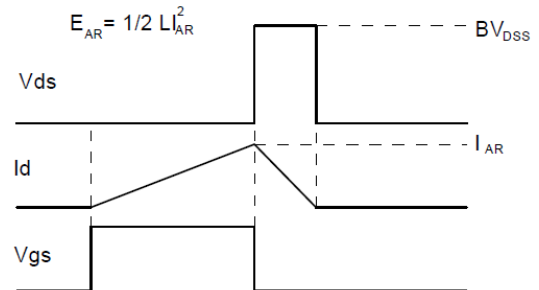
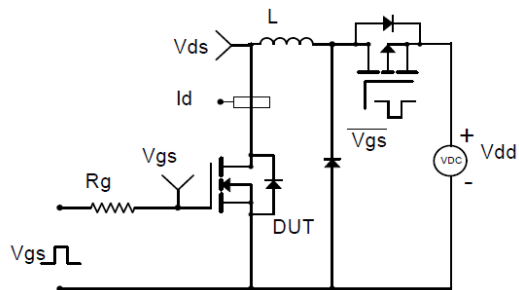
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

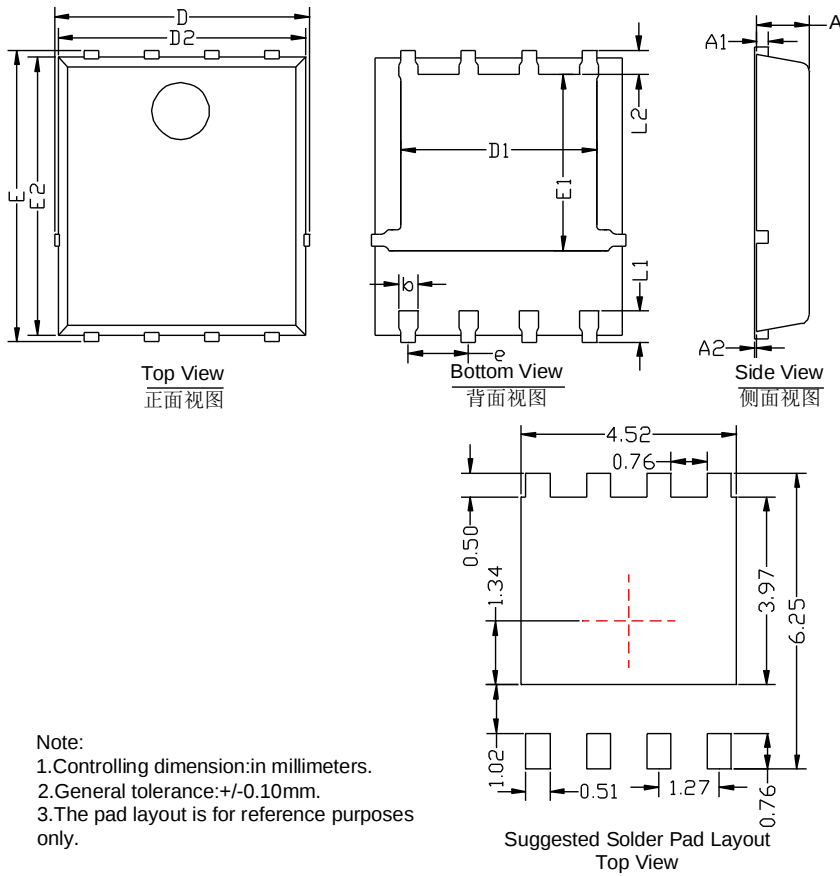


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJG18N10A

■ PDFN5060-8L Package Information



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



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