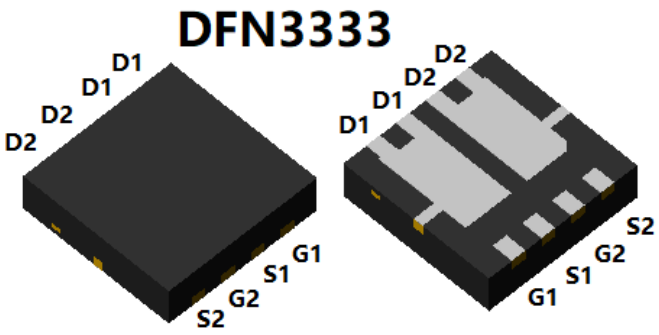
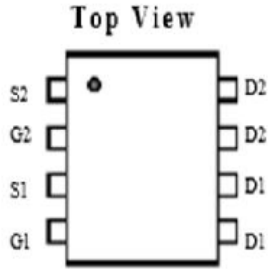
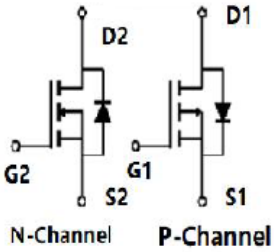
N-Channel and P-Channel Complementary Power MOSFET







Product Summary

NMOS

- V_{DS} 30V
- I_D 3.6A
- $R_{DS(ON)}$(at VGS=10V) ＜30mohm
- $R_{DS(ON)}$(at VGS=4.5V) ＜52mohm

PMOS

- V_{DS} -30V
- I_D -5A
- $R_{DS(ON)}$(at VGS=-10V) ＜45mohm
- $R_{DS(ON)}$(at VGS=-4.5V) ＜65mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

Applications

- Wireless charger
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	±20	±20	V
Drain Current	T_A=25℃	I_D	3.6	-5	A
	T_A=70℃		2.9	-4	
Pulsed Drain Current [A]		I_{DM}	15	-20	A
Total Power Dissipation	T_A=25℃	P_D	2	2	W
	T_A=70℃		1.3	1.3	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	62.5	62.5	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ3611A	F1	Q3611	5000	10000	100000	13“ reel

■ N-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3.6A		23	30	mΩ
		V_{GS}=4.5V, I_D=3A		40	52	
Diode Forward Voltage	V_{SD}	I_S=3.6A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		314		pF
Output Capacitance	C_{oss}			59		
Reverse Transfer Capacitance	C_{rss}			48		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=2A		6.08		nC
Gate-Source Charge	Q_{gs}			1.26		
Gate-Drain Charge	Q_{gd}			1.32		
Reverse Recovery Chrage	Q_{rr}	I_F=3.6A, di/dt=100A/us		1.66		
Reverse Recovery Time	t_{rr}			17.33		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=15V, R_L=4.1Ω R_{GEN}=3Ω		3.8		
Turn-on Rise Time	t_r			23.2		
Turn-off Delay Time	$t_{D(off)}$			7		
Turn-off fall Time	t_f			18.6		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ P-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-4.1A		35	45	mΩ
		V_{GS}=-4.5V, I_D=-3.5A		49	65	
Diode Forward Voltage	V_{SD}	I_S=-4.1A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		719		pF
Output Capacitance	C_{oss}			78		
Reverse Transfer Capacitance	C_{rss}			64		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-5.1A		14.23		nC
Gate-Source Charge	Q_{gs}			3.16		
Gate-Drain Charge	Q_{gd}			2		
Reverse Recovery Chrage	Q_{rr}	I_F=-5.1A, di/dt=100A/us		5.3		
Reverse Recovery Time	t_{rr}			30		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V, I_D=5.1A R_{GEN}=3Ω		7.4		
Turn-on Rise Time	t_r			37		
Turn-off Delay Time	$t_{D(off)}$			31.6		
Turn-off fall Time	t_f			42		

C. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

D. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ N-MOS Typical Performance Characteristics

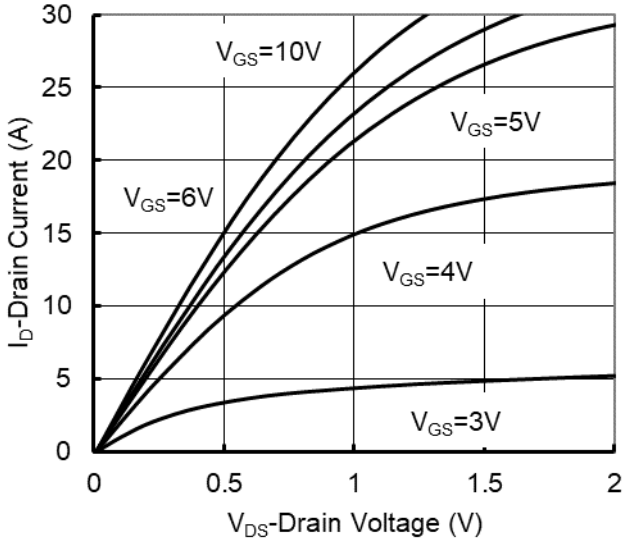


Figure1. Output Characteristics

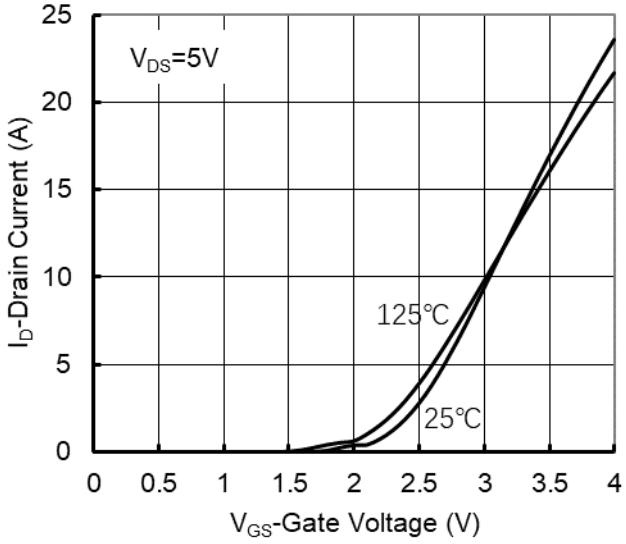


Figure2. Transfer Characteristics

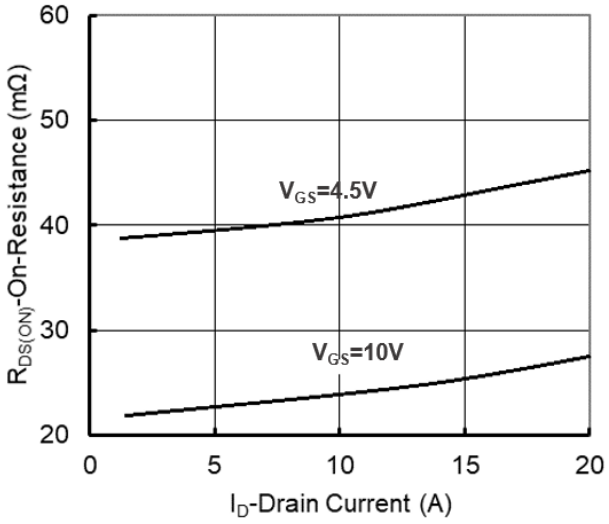


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

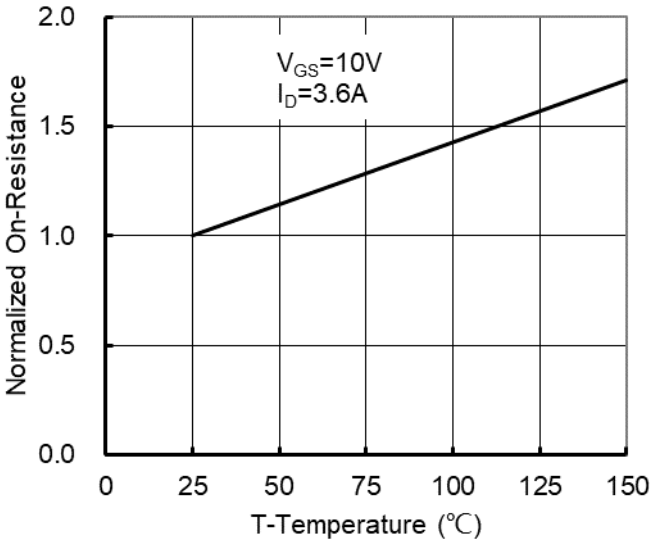


Figure 4: On-Resistance vs. Junction Temperature

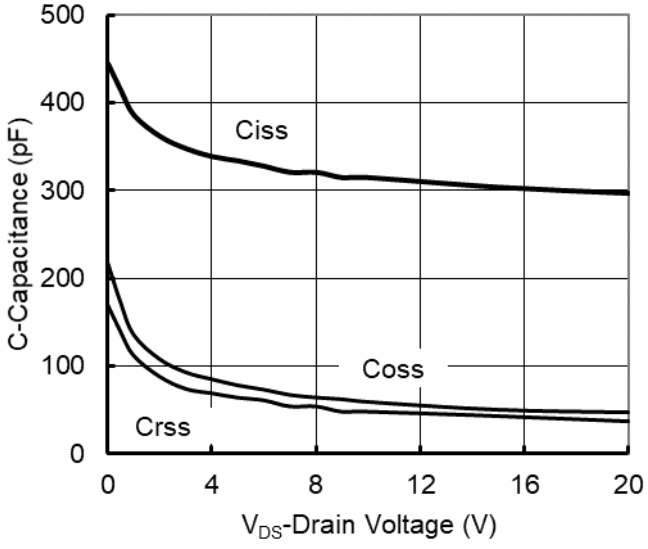


Figure5. Capacitance Characteristics

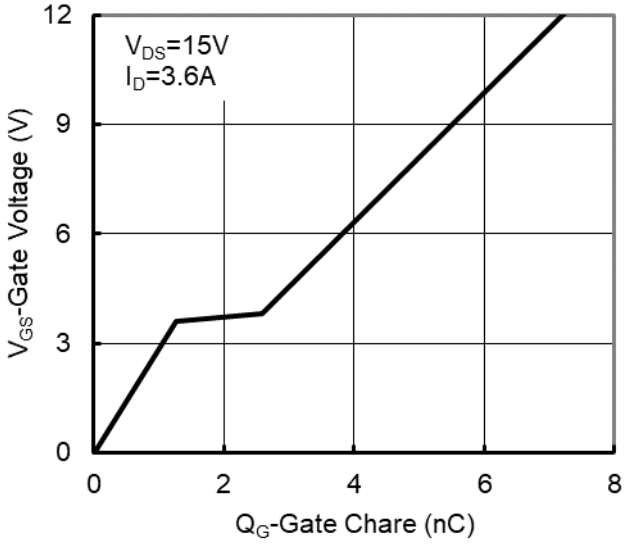


Figure6. Gate Charge

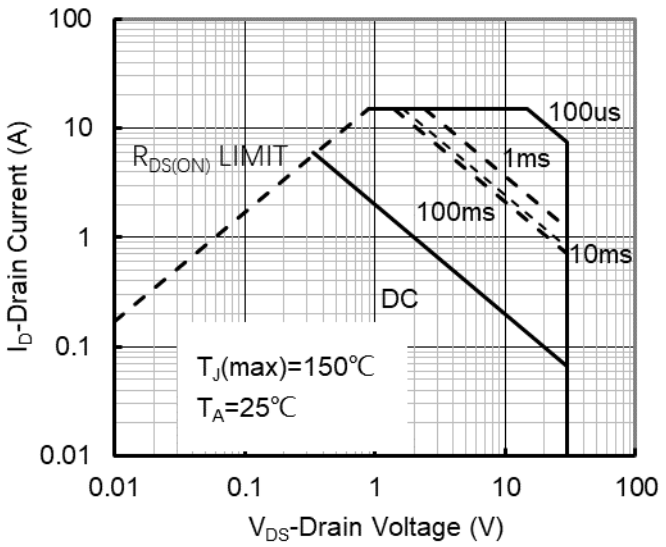


Figure7. Safe Operation Area

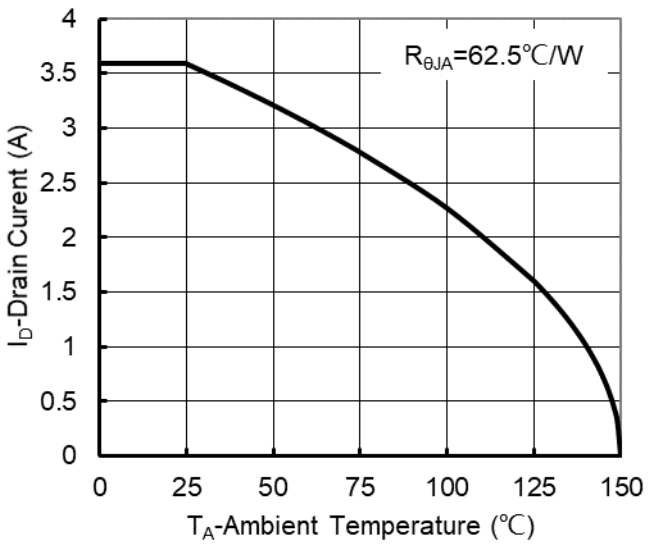


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

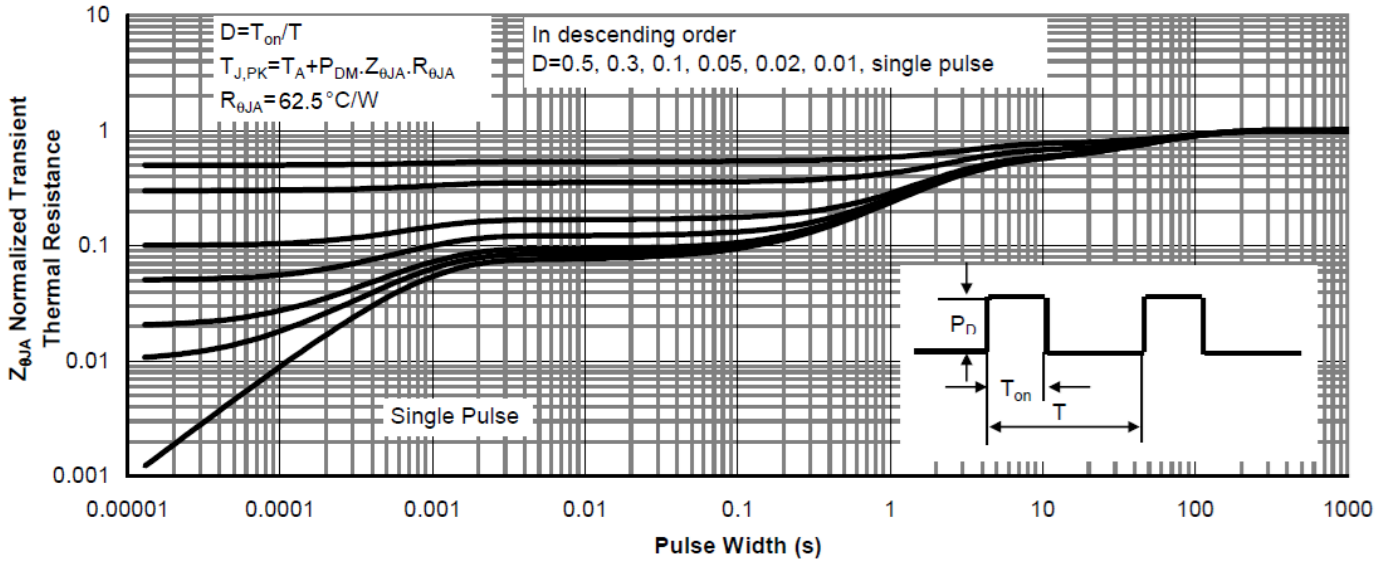


Figure9.Normalized Maximum Transient Thermal Impedance

■ P-MOS Typical Performance Characteristics

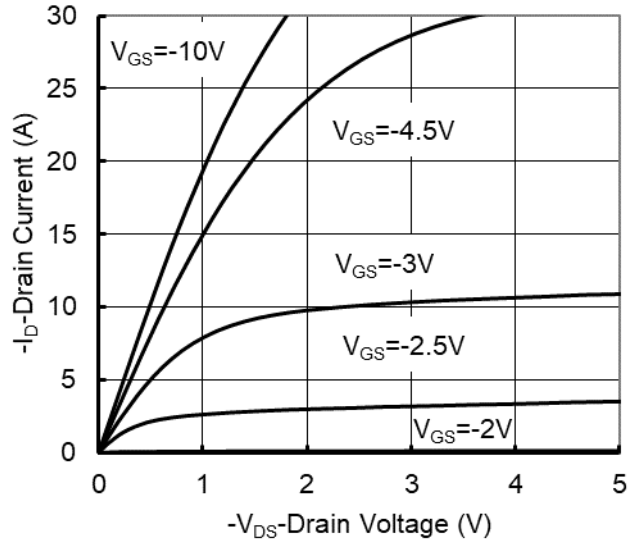


Figure1. Output Characteristics

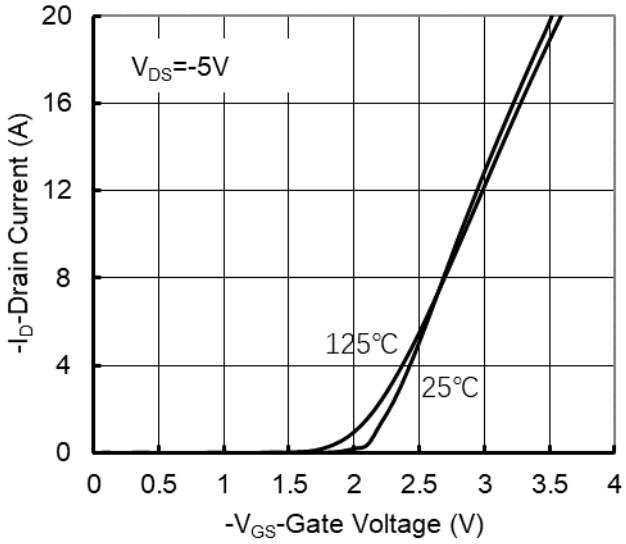


Figure2. Transfer Characteristics

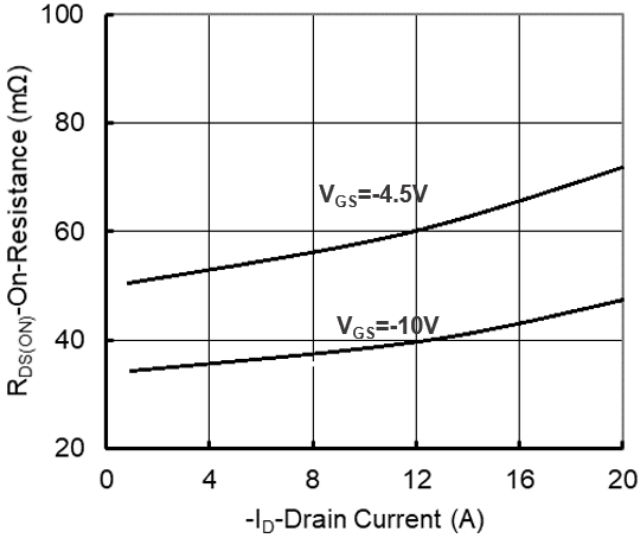


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

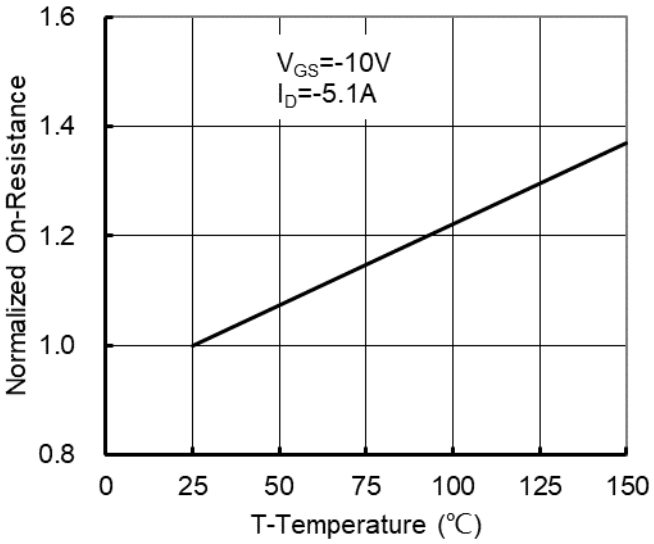


Figure 4: On-Resistance vs. Junction Temperature

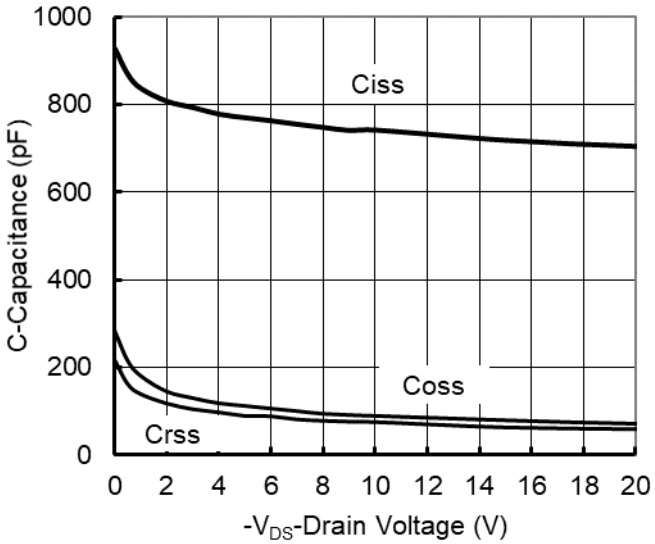


Figure5. Capacitance Characteristics

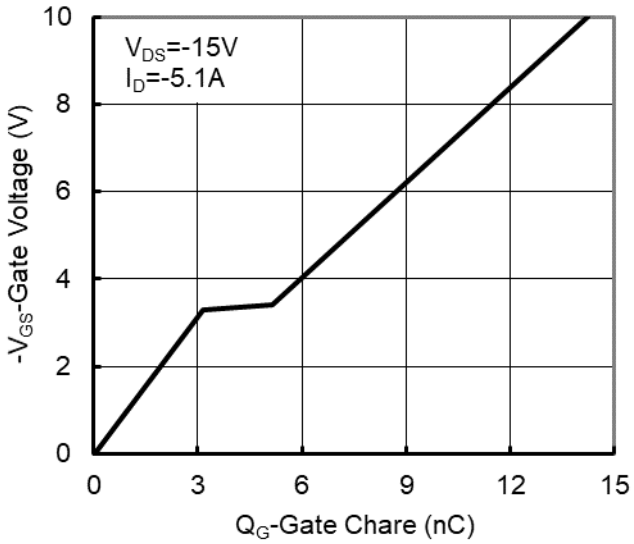


Figure6. Gate Charge

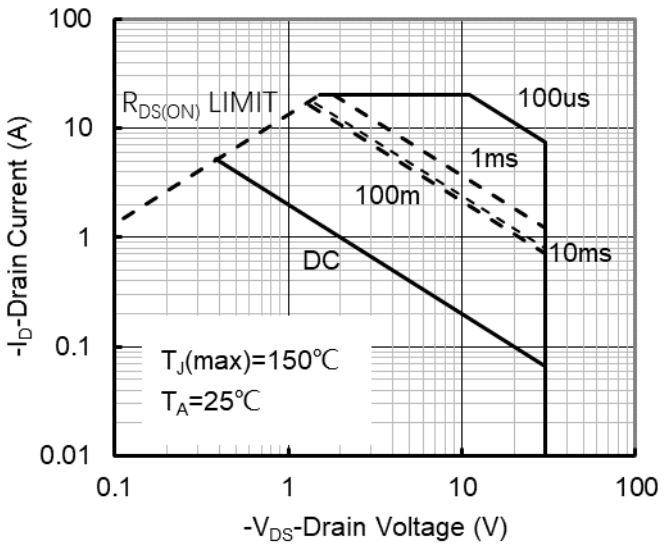


Figure7. Safe Operation Area

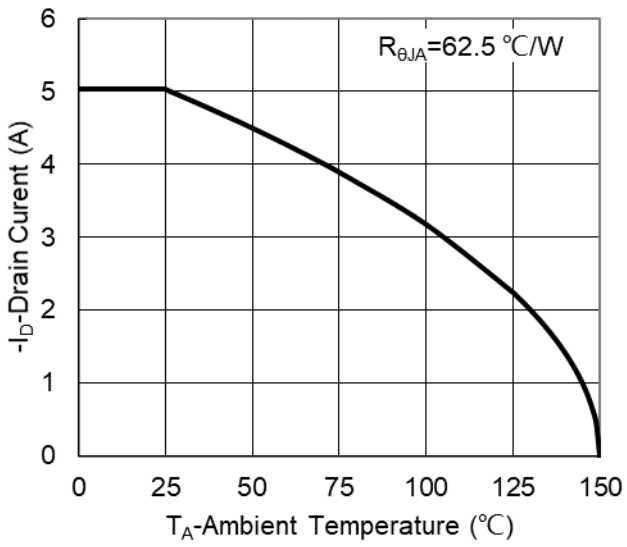


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

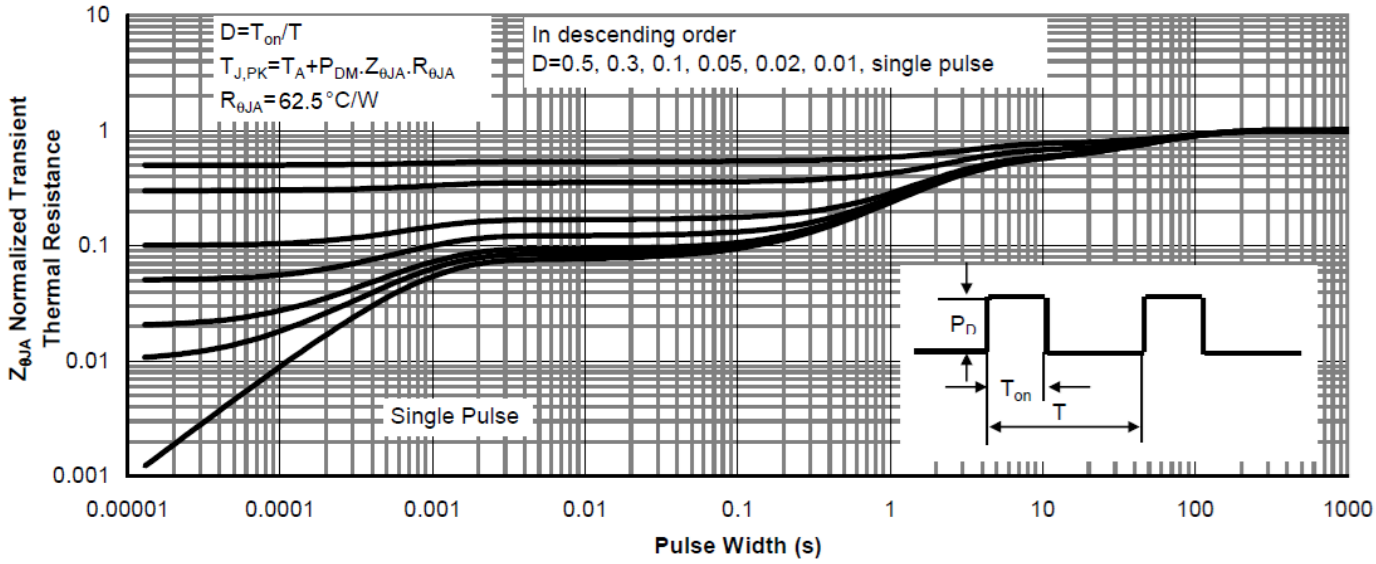
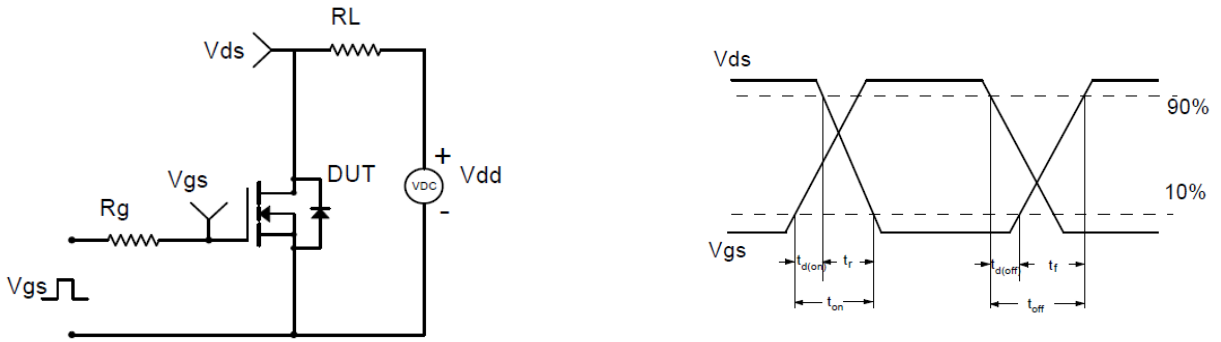
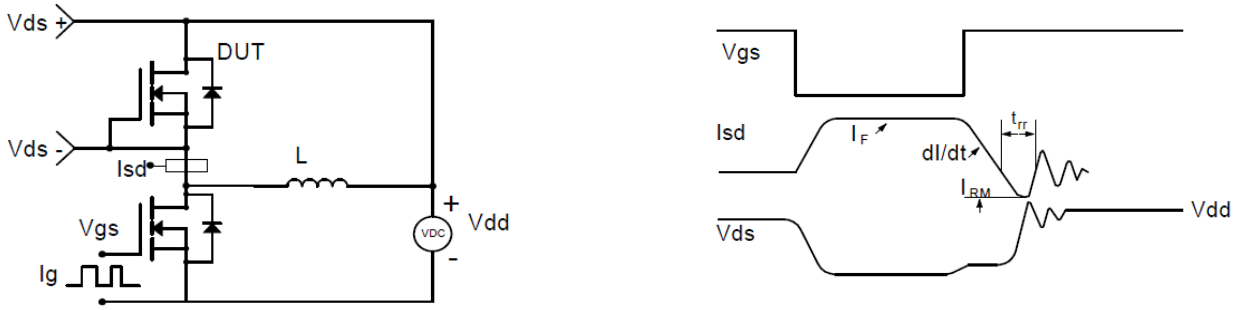


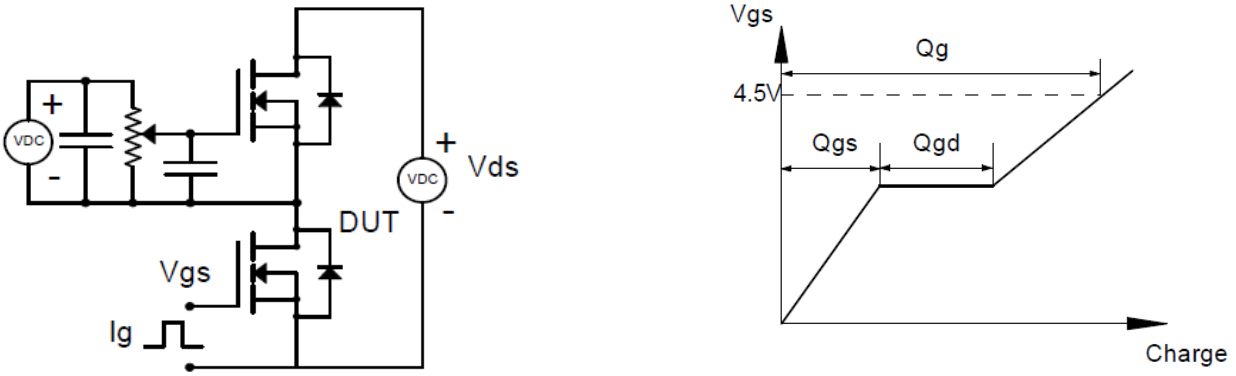
Figure9.Normalized Maximum Transient Thermal Impedance



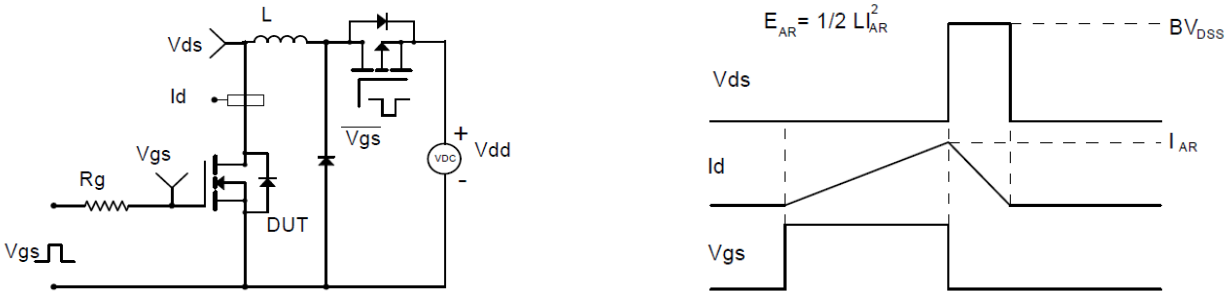
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

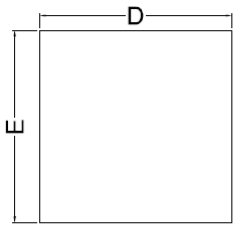


Gate Charge Test Circuit & Waveform

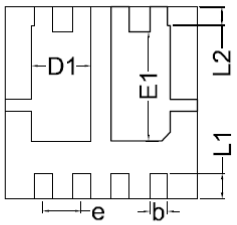


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

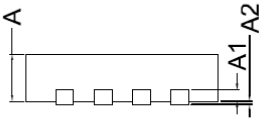
■ DFN3333-8L Package Information



Top View
正面视图

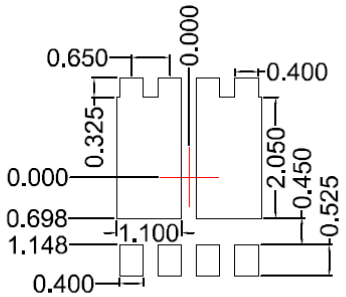


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
L1	0.325	0.425	0.525
L2		0.325 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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