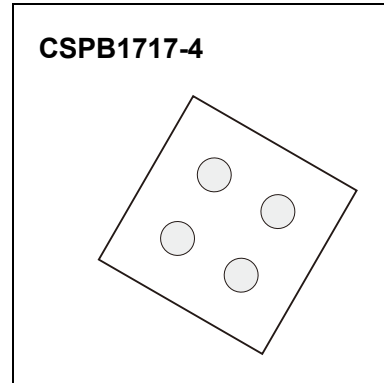


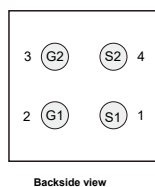
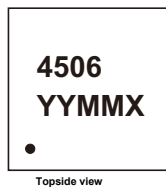
**CSP Enhancement Mode Power MOSFET****CJ4506SP Dual N-Channel MOSFET**

V_{SSS}	$R_{SS(on)}$ TYP	I_S
20V	11.2m Ω @4.5V	10A
	11.5m Ω @4.0V	
	11.8m Ω @3.7V	
	12.7m Ω @3.1V	
	14.7m Ω @2.5V	

**DESCRIPTION**

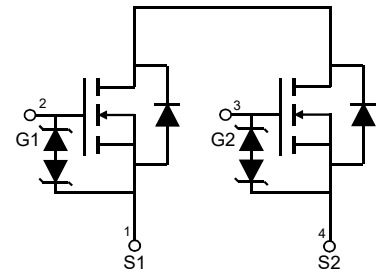
The CJ4506SP uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected.

This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment

Marking:

- | | |
|-----------------------|-----------|
| 1. 4506: Product Code | 1 Source1 |
| 2. YYMMX: Date Code | 2 Gate1 |
| 3. Solid dot: Pin 1 | 3 Gate2 |
| | 4 Source2 |

Equivalent Circuit**ABSOLUTE MAXIMUM RATINGS ($T_a=25^{\circ}\text{C}$ unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Source Current(DC)	I_S ①	10	A
Source Current (Pulsed)	I_{SP} ①	100	A
Total Power Dissipation	P_T ①	2.1	W
Channel Temperature	T_{ch}	150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55 To 150	$^{\circ}\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS

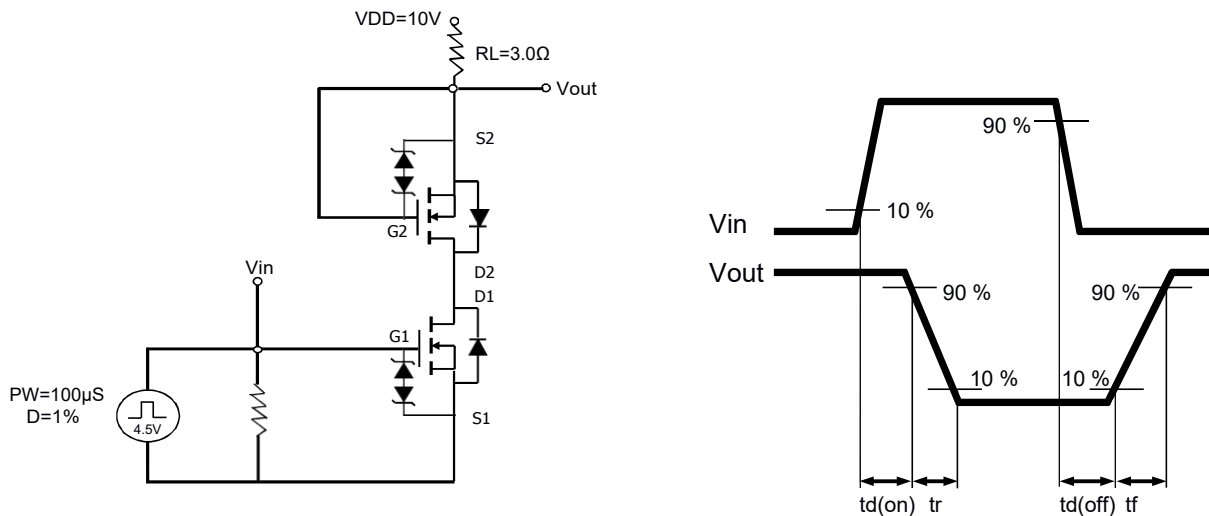
$T_a=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	$I_S=1\text{mA}, V_{GS}=0\text{V}$	20			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=16\text{V}, V_{GS}=0\text{V}$			1.0	μA
Gate to Source Leakage Current	I_{GSS}	$V_{SS}=0\text{V}, V_{GS}=\pm 10\text{V}$			± 10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=V_{GS}, I_S=250\mu\text{A}$	0.3	0.88	1.1	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=3\text{A}$	7.8	11.2	13.5	$\text{m}\Omega$
		$V_{GS}=4.0\text{V}, I_S=3\text{A}$	8.0	11.5	14.1	$\text{m}\Omega$
		$V_{GS}=3.7\text{V}, I_S=3\text{A}$	8.2	11.8	15.5	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=3\text{A}$	8.9	12.7	17.0	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=3\text{A}$	10.3	14.7	21.4	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{SS}=10\text{V}, V_{GS}=0\text{V}, f=1\text{kHz}$		1746		pF
Output Capacitance	C_{oss}			260		pF
Reverse Transfer Capacitance	C_{rss}			189		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10\text{V}, R_L=3\Omega, V_{GS}=4.5\text{V}$		0.38		μS
Turn-on Rise Time	t_r			0.56		μS
Turn-off Delay Time	$t_{d(off)}$			2.54		μS
Turn-off Fall Time	t_f			1.01		μS
Total Gate Charge	Q_g	$V_{SS}=10\text{V}, I_S=5\text{A}, V_{GS}=8\text{V}$		28		nC
Gate1-source1 charge	Q_{g1s1}			3.5		nC
Gate1-source2 charge	Q_{g1s2}			6.0		nC
Diode Forward Voltage	$V_{F(S-S)}$	$V_{GS}=0\text{V}, I_S=1\text{A}$			1.0	V

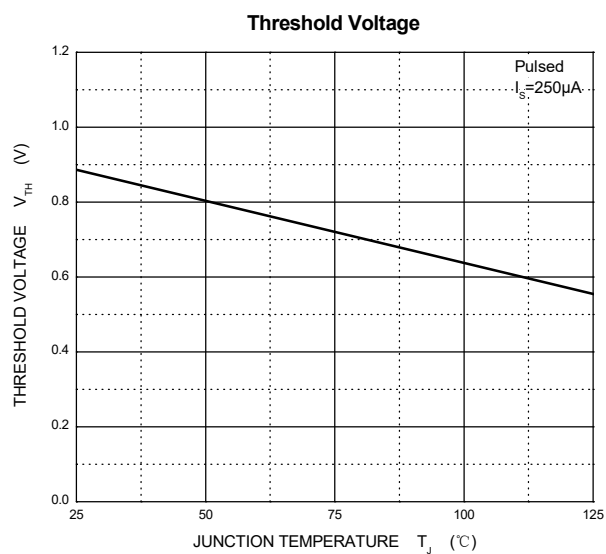
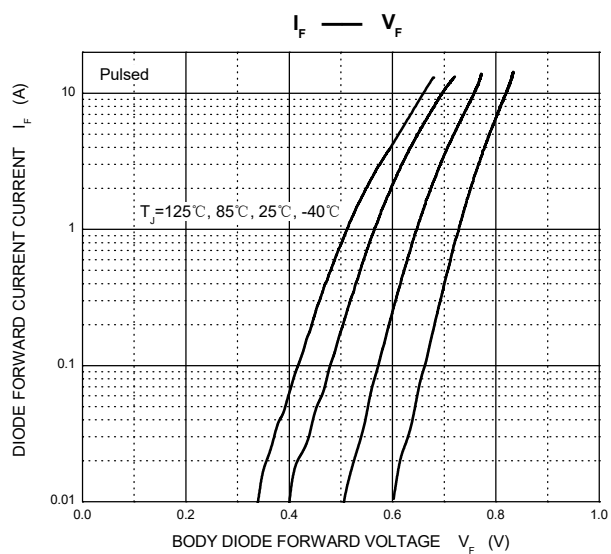
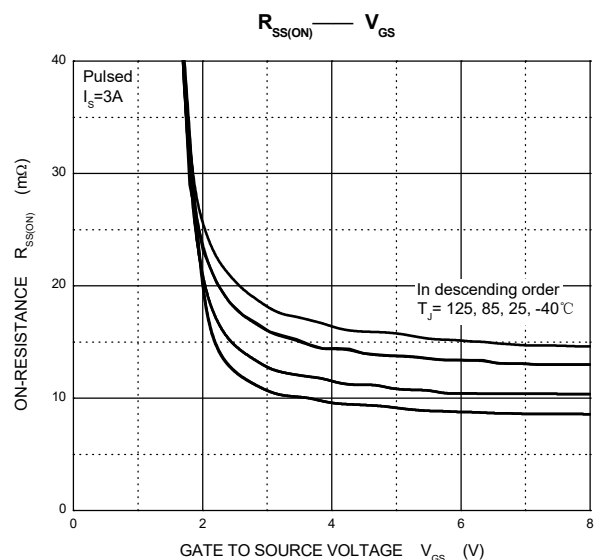
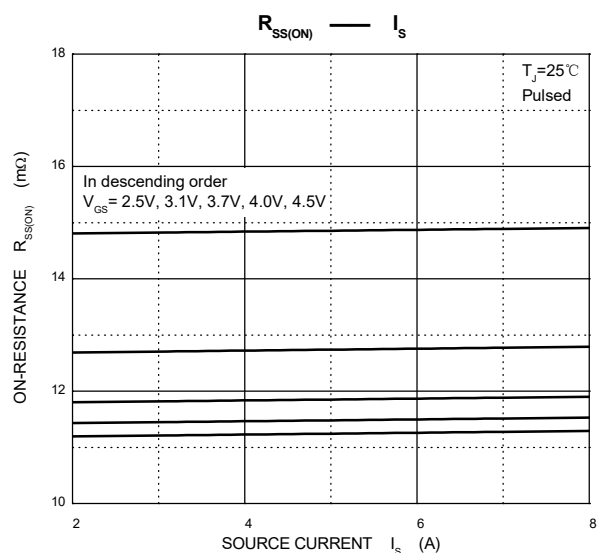
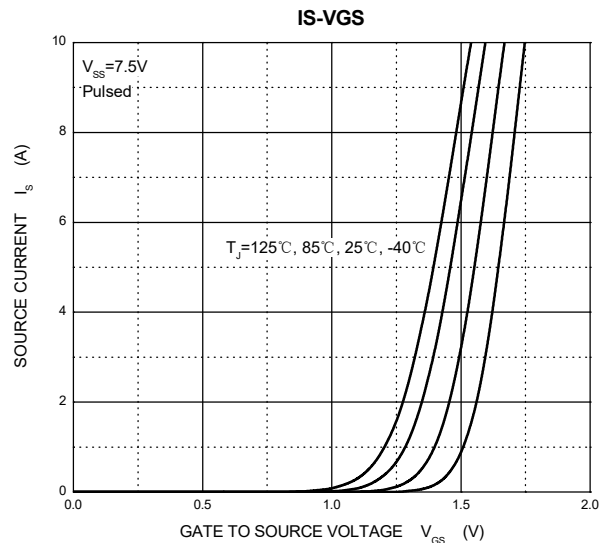
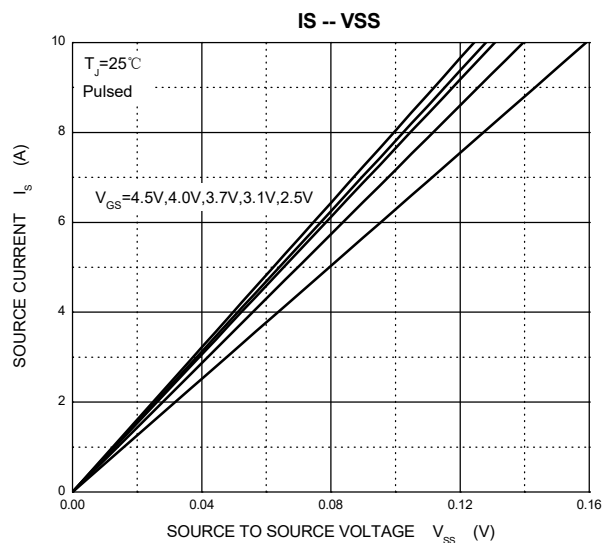
Notes: 1.Mounted on FR4 board (25.4mm×25.4mm×1.0mm) using the minimum recommended pad size (36um Copper).

2. $t = 10\text{ms}$, Duty Cycle = 1 %.

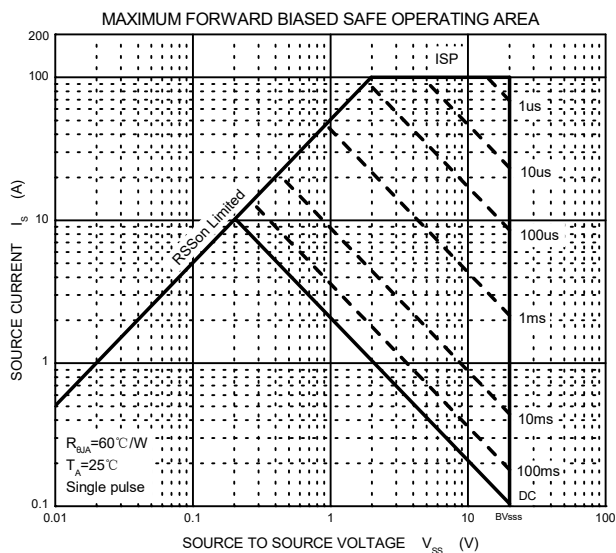
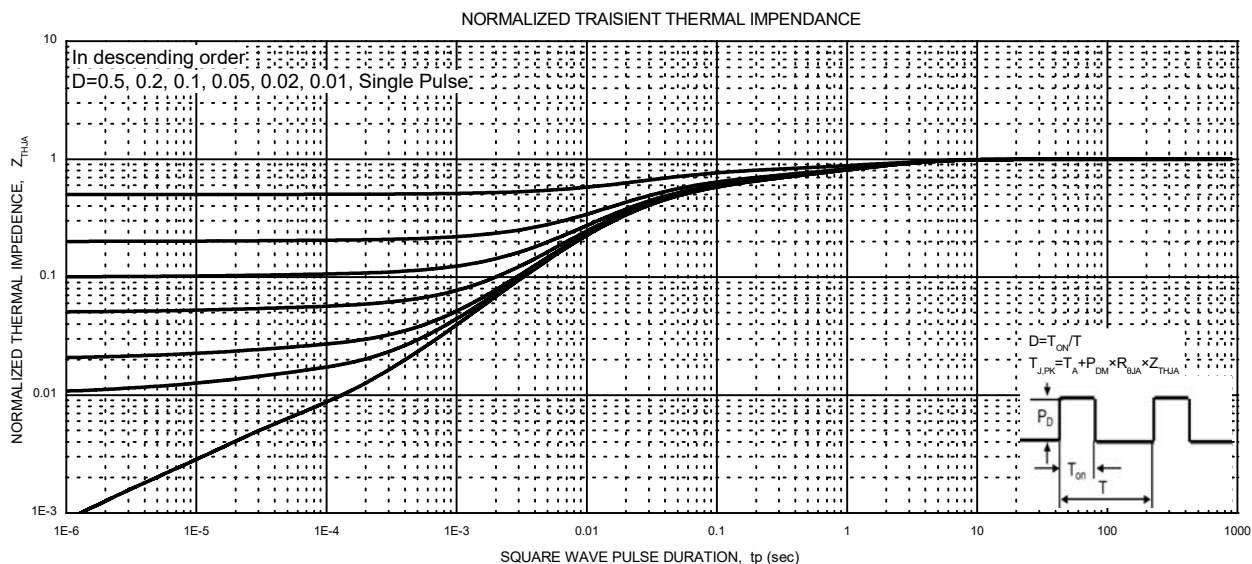
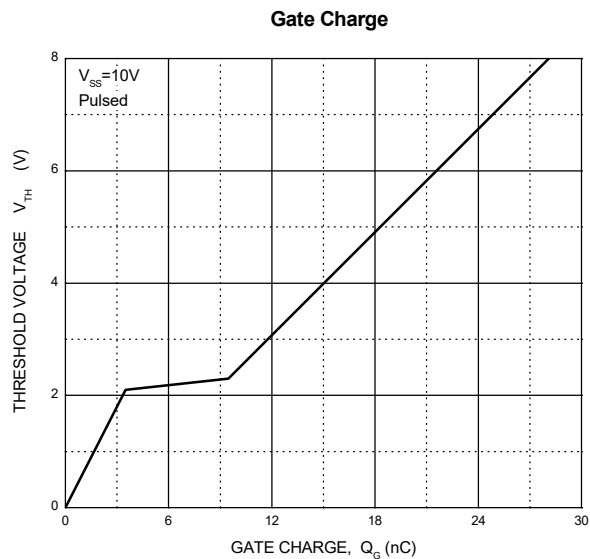
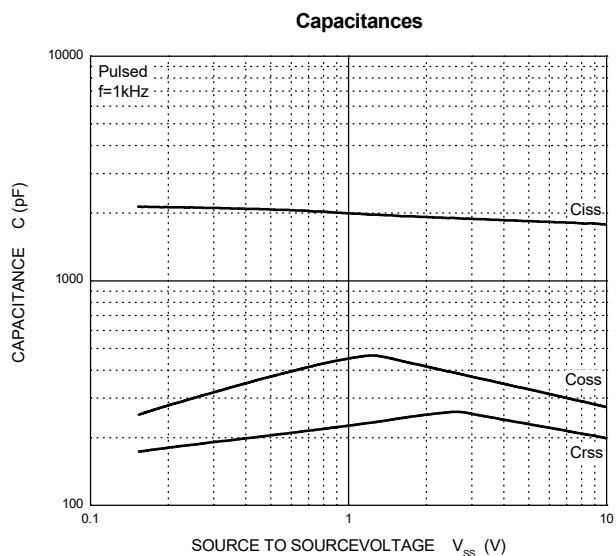
3.When FET1 is measured,G2 and S2 are short-circuited.



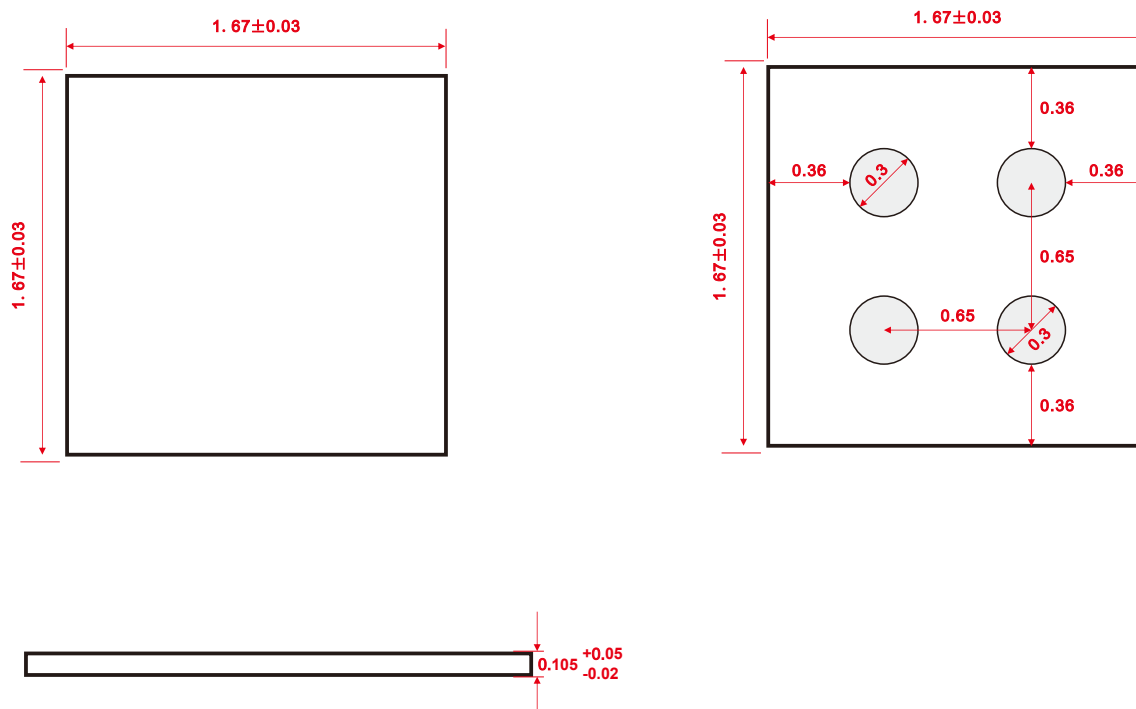
Typical Characteristics



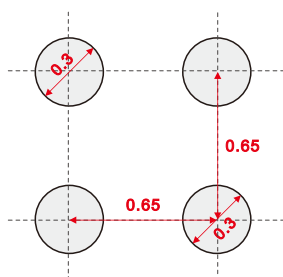
Typical Characteristics



CSPB1717-4 Package Outline Dimensions(Unit:mm)



CSPB1717-4 Suggested Pad Layout (Unit:mm)



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.050 mm.
3. The pad layout is for reference purposes only.

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