

LP2323LT1G

S-LP2323LT1G

12V P-Channel Enhancement MOSFET

1. FEATURES

- $V_{DS} = -12V$
- $R_{DS(ON)} \leq 32m\Omega, V_{GS} @ -4.5V, I_{DS} @ -1.0A$
- $R_{DS(ON)} \leq 40m\Omega, V_{GS} @ -2.5V, I_{DS} @ -1.0A$
- $R_{DS(ON)} \leq 71m\Omega, V_{GS} @ -1.8V, I_{DS} @ -1.0A$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. APPLICATIONS

- Battery Switch
- High Side Load Switch

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2323LT1G	12K	3000/Tape&Reel
LP2323LT3G	12K	10000/Tape&Reel

4. MAXIMUM RATINGS($T_a = 25^\circ C$)

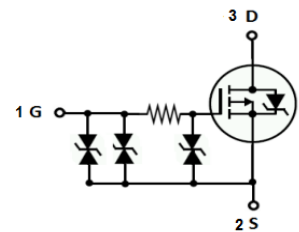
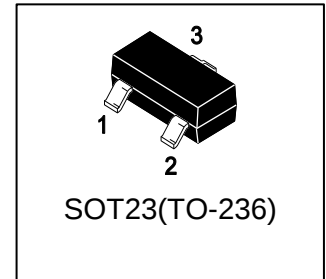
Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DSS}	-12	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 8	V
Drain Current			
– Continuous $T_a = 25^\circ C$	I_D	-6	A
– Pulsed(Note 1)	I_{DM}	-21	
Avalanche Current($L=0.1mH$)	I_{AS}	15	A
Avalanche energy($L=0.1mH$)	E_{AS}	11.25	mJ

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	P_D	0.9	W
Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	140	$^\circ C/W$
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ C$

1. Repetitive Rating: Pulse width limited by the Maximum junction temperature.

2. 1-in² 2oz Cu PCB board.

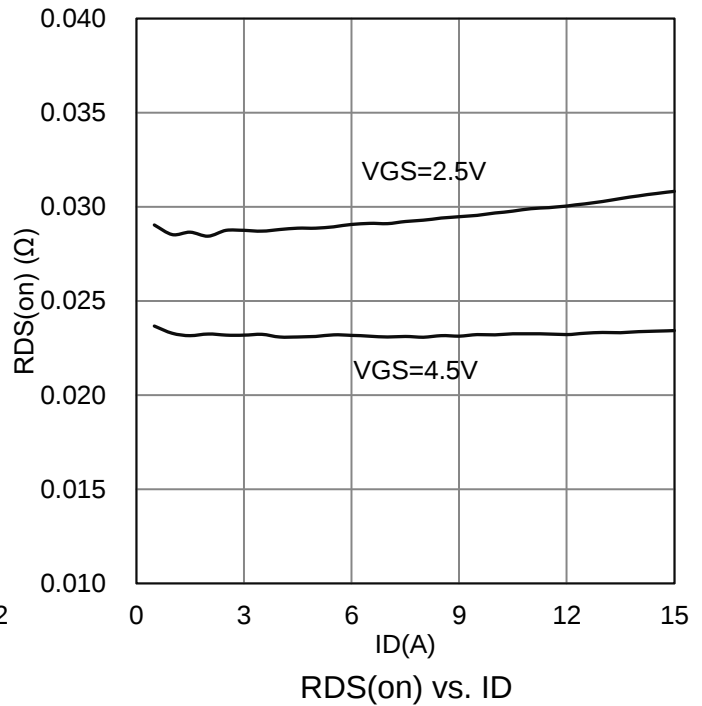
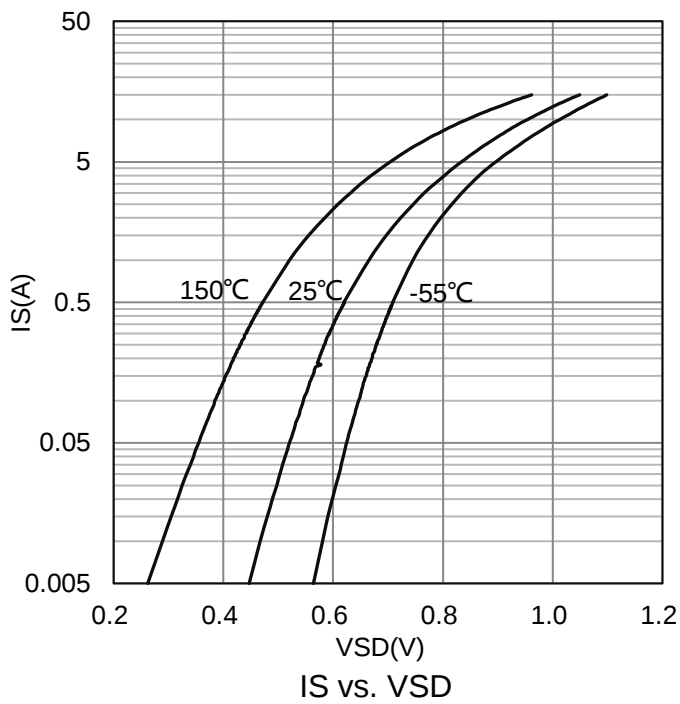
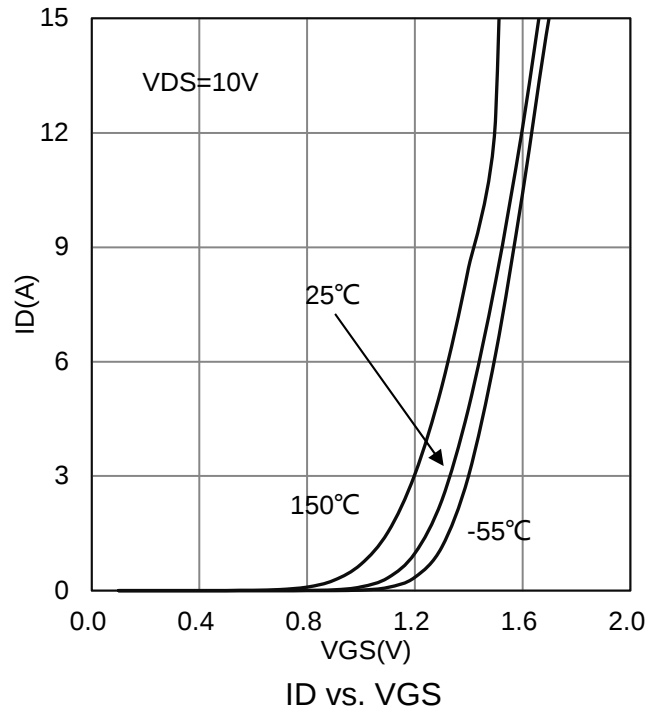
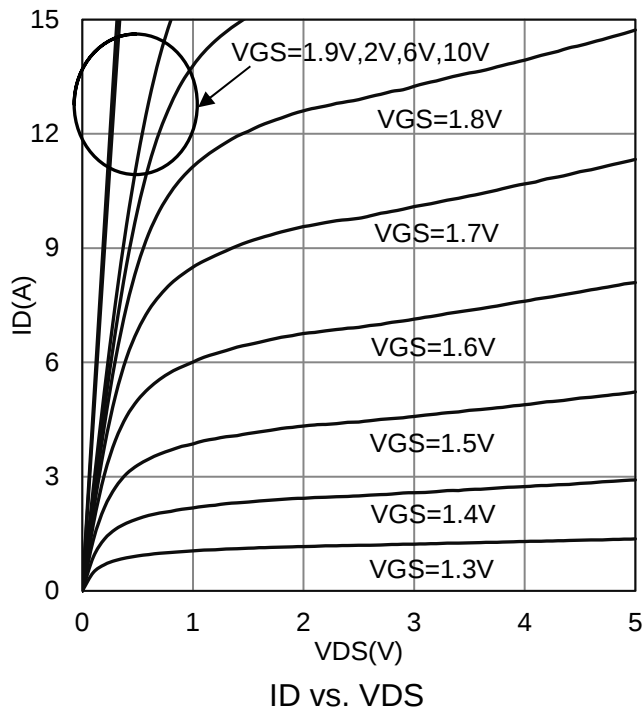


6. ELECTRICAL CHARACTERISTICS

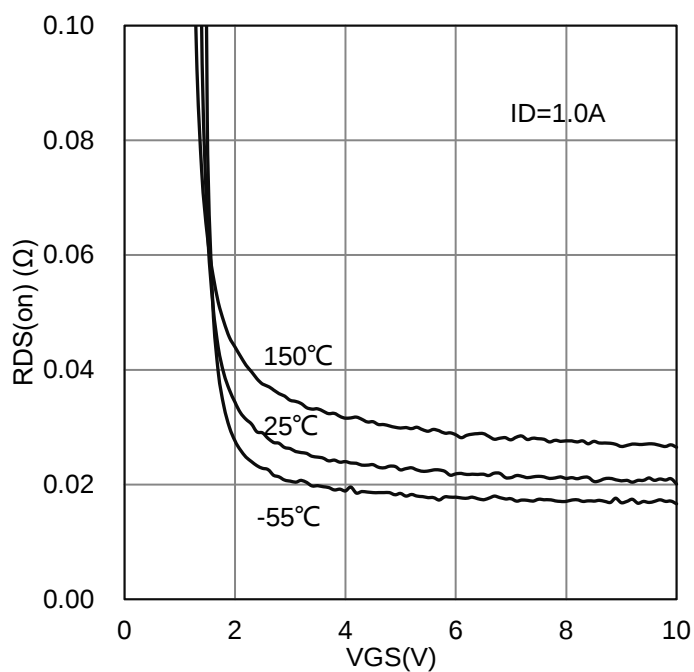
Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)		VBRDSS	-12	-	-	V
Gate-Source Threshold Voltage (VDS =VGS , ID =-250μA)		VGS(th)	-	-	-1	V
Gate-Body Leakage Current (VDS =0V, VGS =± 8V)		IGSS	-	-	± 10	μA
Zero Gate Voltage Drain Current (VDS = -12 V, VGS = 0 V)		IDSS	-	-	-1	μA
Drain-Source On-Resistance(Note 3) (VGS = -4.5 V, ID = -1 A) (VGS = -2.5 V, ID = -1 A) (VGS = -1.8 V, ID = -1 A)		RDS(ON)	- - -	27 32 45	32 40 71	mΩ
Diode Forward Voltage(Note 3) (IS = -1 A, VGS = 0 V)		VSD	-	-	-1.5	V
DYNAMIC						
Total Gate Charge	(VDS = -15 V, VGS = -4.5 V,ID = -4 A)	Qg	-	17	-	nC
Gate-Source Charge		Qgs	-	2	-	
Gate-Drain Charge		Qgd	-	5	-	
Turn-On Delay Time	(VGS = -4.5 V, VDD = -15V ID =-4A RG=1Ω)	td(on)	-	8.6	-	ns
Rise Time		tr	-	15	-	
Turn-Off Delay Time		td(off)	-	150	-	
Fall Time		tf	-	88	-	
Input Capacitance	(VDS = -15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	1624	-	pF
Output Capacitance		Coss	-	315	-	
Reverse Transfer Capacitance		Crss	-	348	-	
Gate Resistance (VDS=0V ,VGS=0V, f=1.0MHz)		Rg	-	188	-	Ω

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

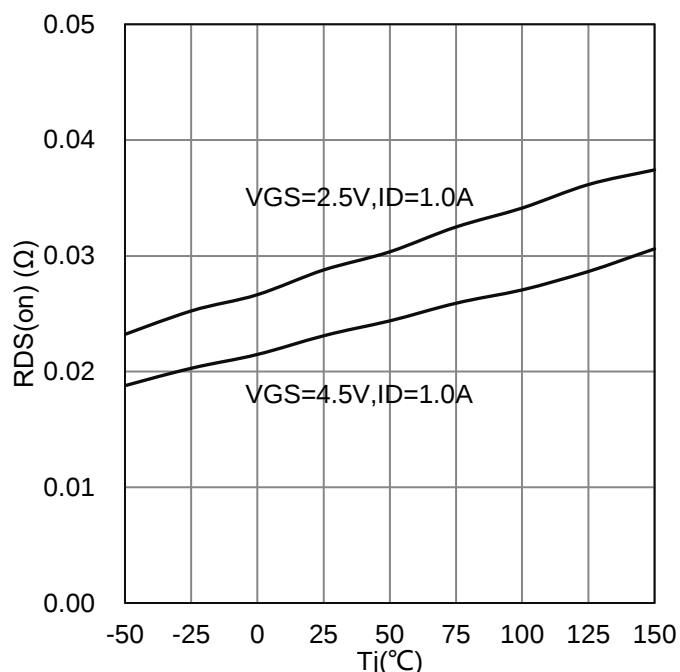
7. ELECTRICAL CHARACTERISTICS CURVES



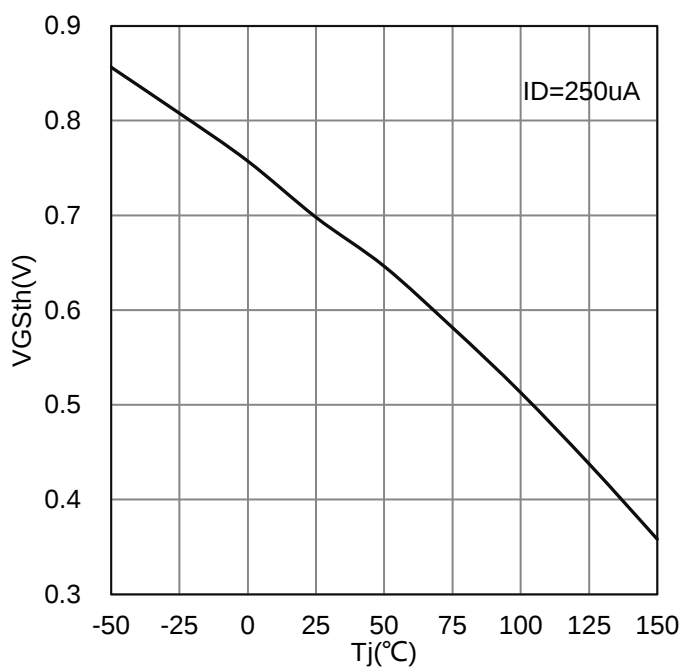
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



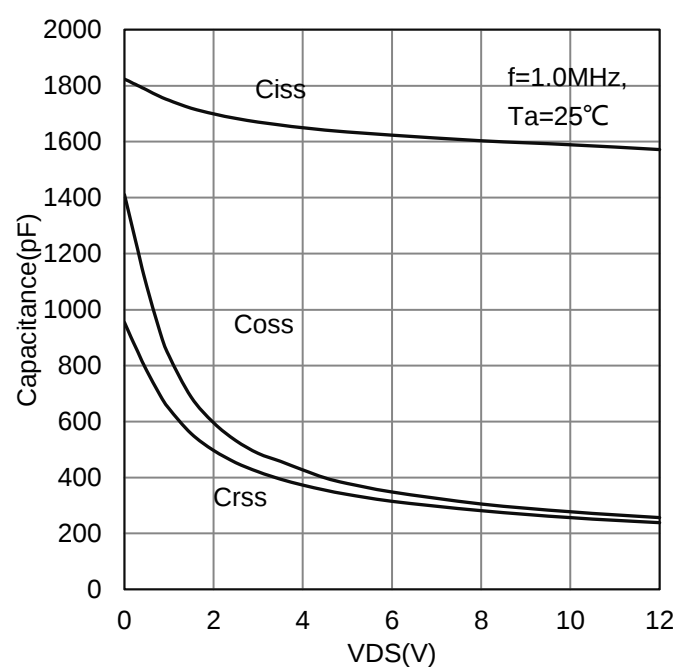
RDS(on) vs. VGS



RDS(on) vs. Tj



VGSth vs. Tj

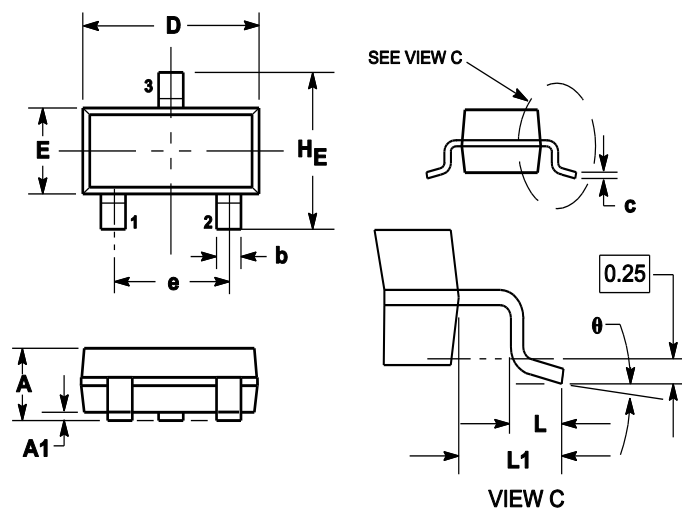


Capacitance

8.OUTLINE AND DIMENSIONS

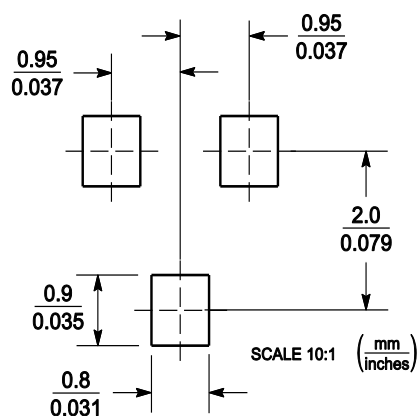
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H _E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9.SOLDERING FOOTPRINT



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