

S-LN2312LT1G

20V N-Channel Enhancement-Mode MOSFET

1. FEATURES

- $V_{DS} = 20V$
- $R_{DS(ON)}, V_{GS}@4.5V, I_{DS}@5A \leq 41m\Omega$
- $R_{DS(ON)}, V_{GS}@2.5V, I_{DS}@4.5A \leq 52m\Omega$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. APPLICATIONS

- High density cell design for ultra low on-resistance
- Advanced trench process technology

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
S-LN2312LT1G	N12	3000/Tape&Reel
S-LN2312LT3G	N12	10000/Tape&Reel

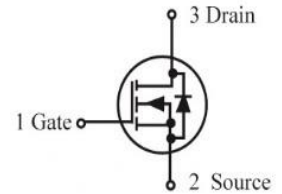
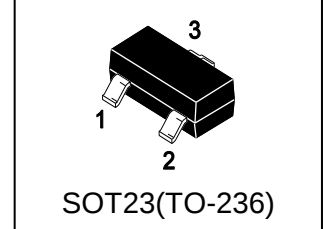
4. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 8	V
Drain Current			
– Continuous $T_a = 25^\circ C$	I_D	4.9	A
– Pulsed(Note 1)	I_{DM}	15	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	1.25	W
Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	120	$^\circ C/W$
Junction-to-Case	$R_{\theta JC}$	90	
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +175$	$^\circ C$

1. Repetitive Rating: Pulse width limited by the Maximum junction temperature.
2. 1-in² 2oz Cu PCB board.

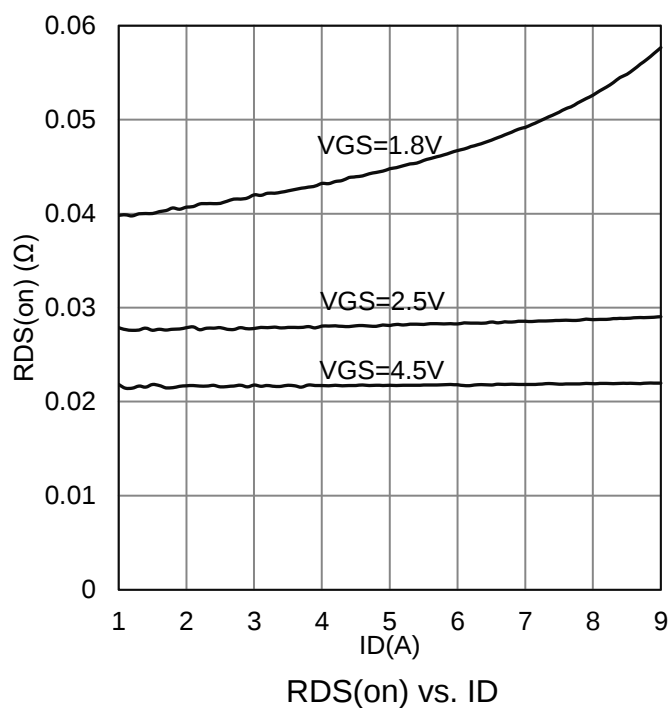
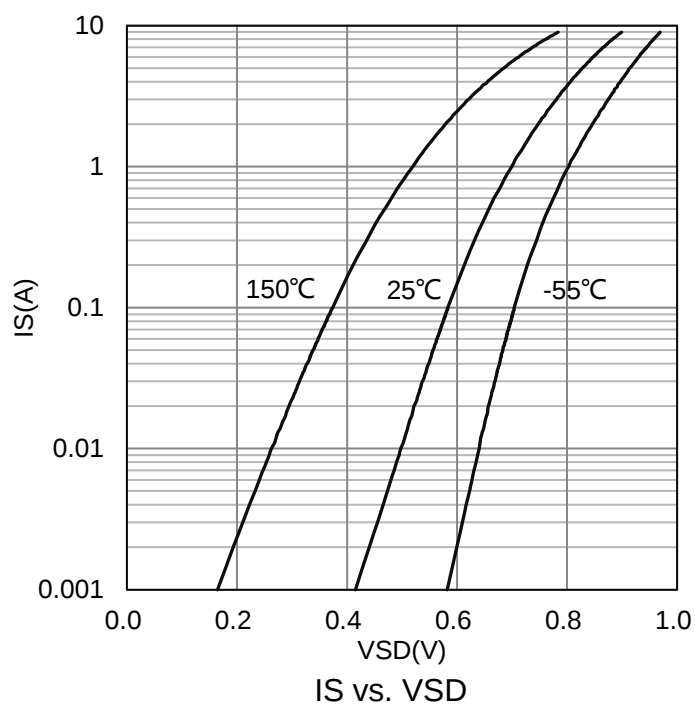
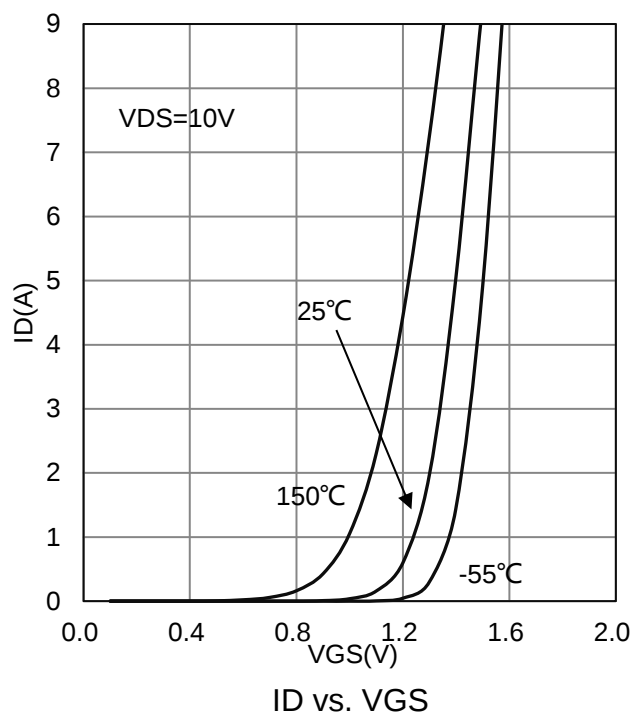
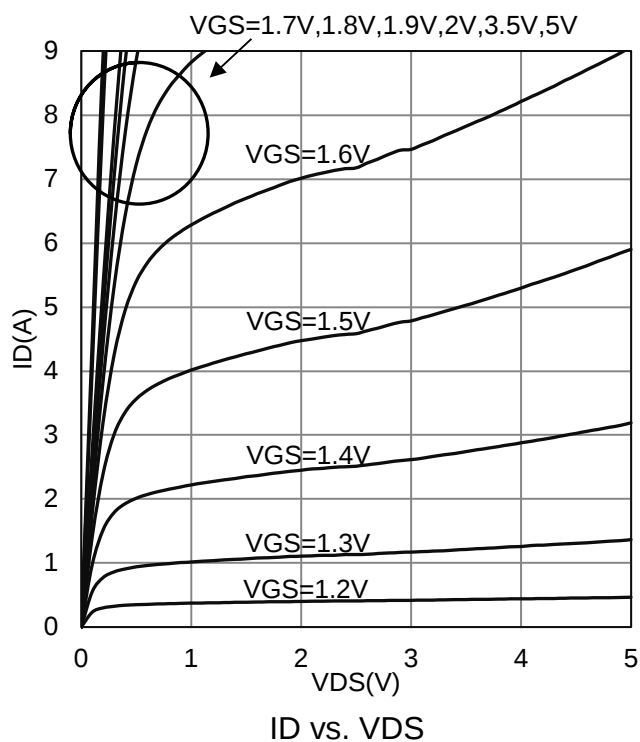


6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

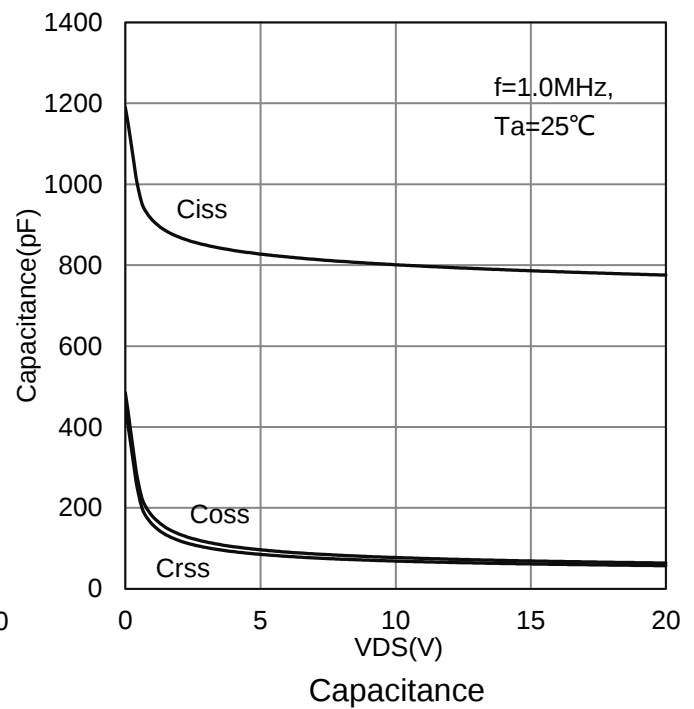
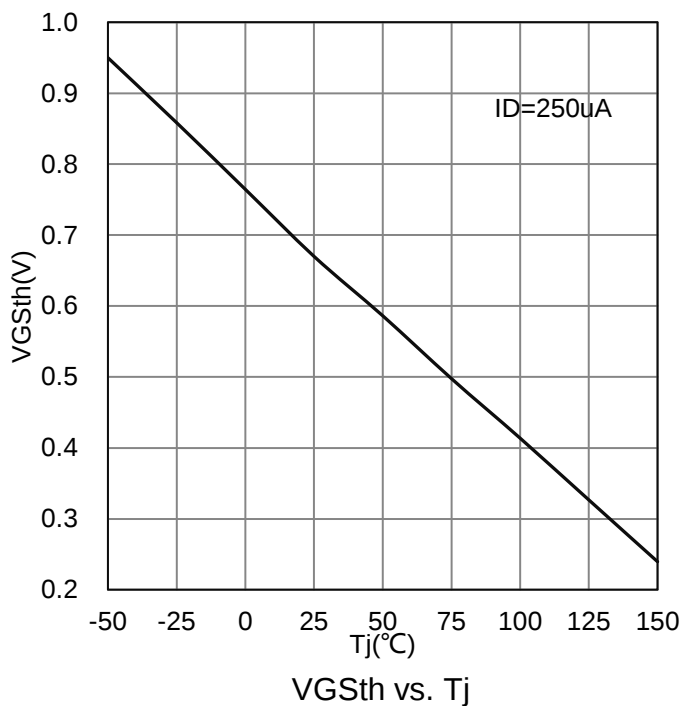
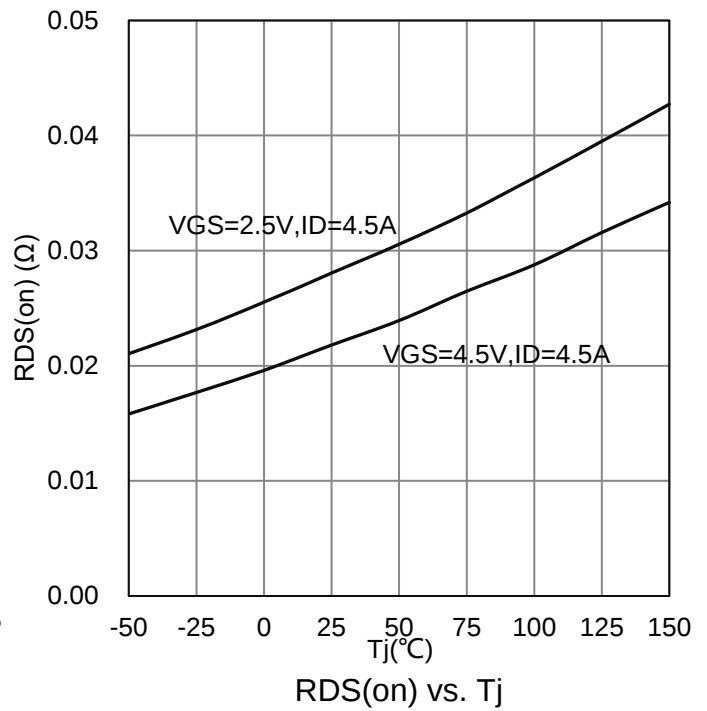
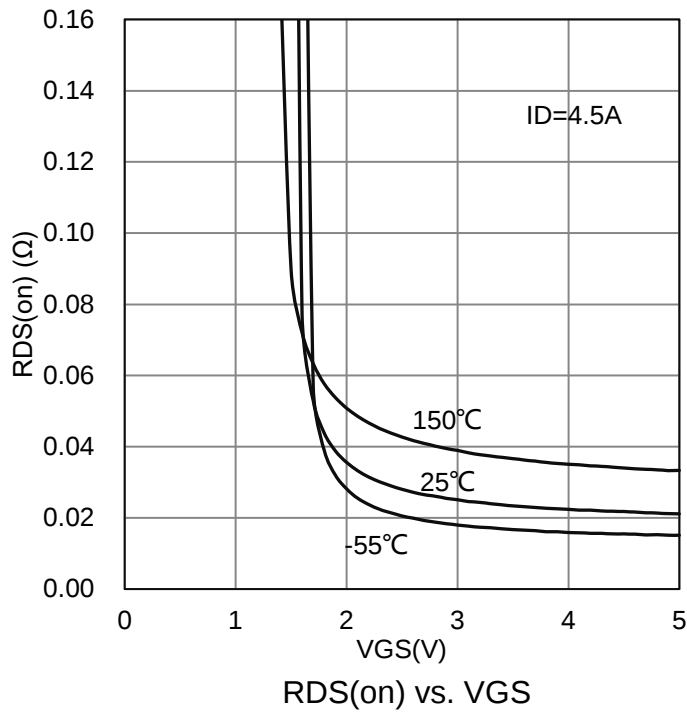
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Static					
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)	V(BR)DSS	20	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = 250μA)	VGS(th)	0.4	0.6	1.0	V
Zero Gate Voltage Drain Current (VDS=20V, VGS=0V)	IDSS	-	-	1	μA
Gate–Body Leakage Current, Forward (VDS = 0 V, VGS = 8 V)	IGSSF	-	-	100	nA
Gate–Body Leakage Current, Reverse (VDS = 0 V, VGS = -8 V)	IGSSR	-	-	-100	nA
Static Drain–Source On–State Resistance (VGS = 1.8 V, ID = 4 A) (VGS = 2.5 V, ID = 4.5 A) (VGS = 4.5 V, ID = 4.5 A)	RDS(on)	- - -	31 24 21	71 52 41	mΩ
Diode Forward Voltage (VGS = 0 V, ISD = 1.7 A)	VSD	-	-	1.2	V
Dynamic					
Total Gate Charge	(VDS = 10 V, VGS = 10 V, ID = 4 A)	Qg	-	18.4	nC
Gate to Source Charge		Qgs	-	1	
Gate to Drain Charge		Qgd	-	2.4	
Input capacitance	(VDS =10V, VGS =0V, f=1MHz)	Ciss	-	801	pF
Output Capacitance		Coss	-	78	
Reverse Transfer Capacitance		Crss	-	69	
Turn-On Delay Time	(VDD =10V, ID =1A, VGEN=4.5V, RG = 6Ω)	td(on)	-	7.8	ns
Rise Time		tr	-	13	
Turn-Off Delay Time		td(off)	-	40.7	
Fall Time		tf	-	15.3	

3.Pulse test; pulse width≤300μs, duty cycle≤2%.

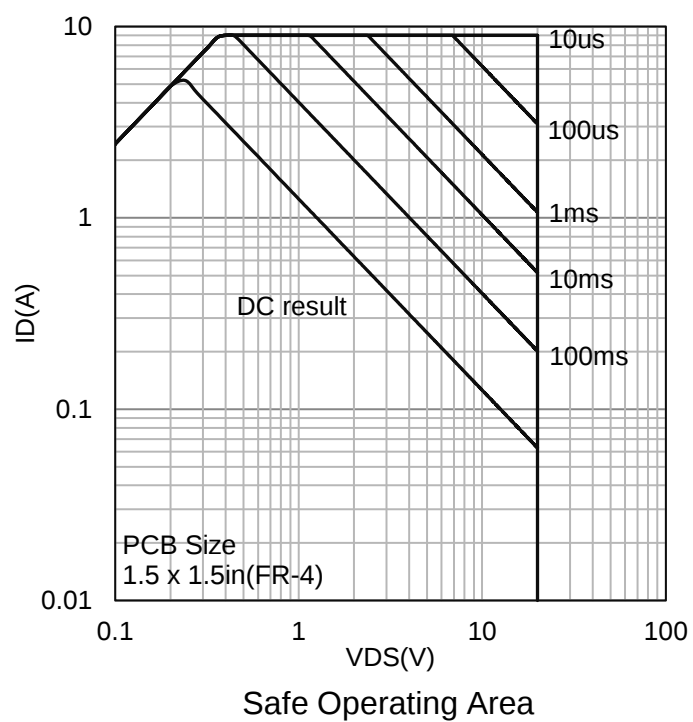
7. ELECTRICAL CHARACTERISTICS CURVES



7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



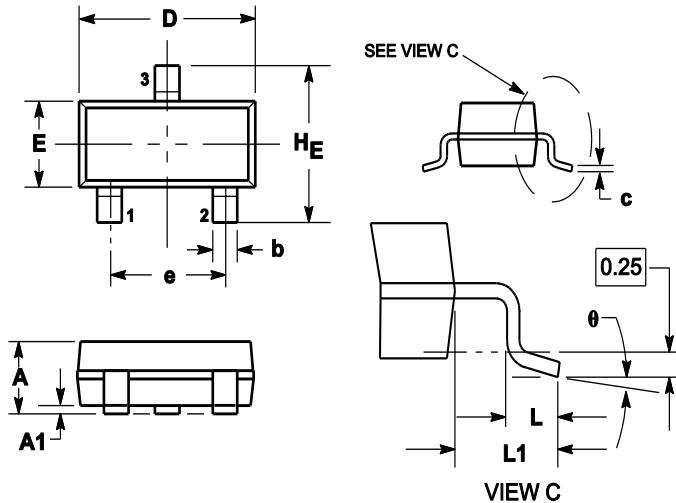
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8.OUTLINE AND DIMENSIONS

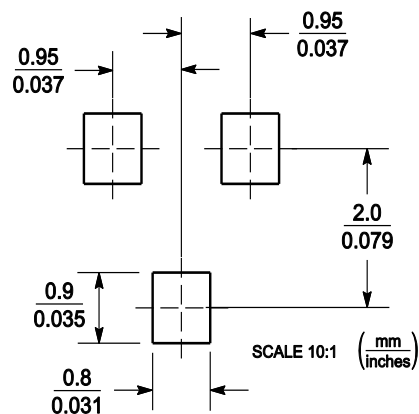
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H _E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9.SOLDERING FOOTPRINT



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