

- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

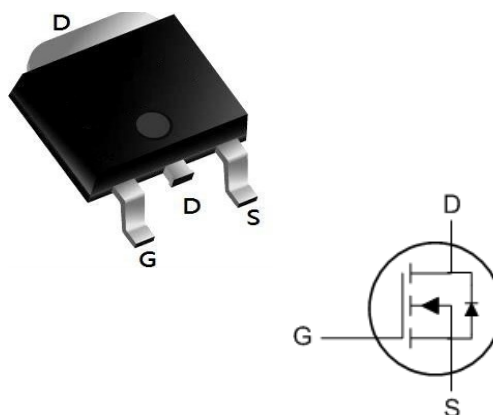
Product Summary

BVDSS	RDS(on)	ID
100V	85 mΩ	15A

Description

The SFT1443-TL-W is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The SFT1443-TL-W meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	15	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	7.7	A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	3	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	2.4	A
I _{DM}	Pulsed Drain Current ²	24	A
EAS	Single Pulse Avalanche Energy ³	6.1	mJ
I _{AS}	Avalanche Current	11	A
P _D @T _C =25°C	Total Power Dissipation ³	34.7	W
P _D @T _A =25°C	Total Power Dissipation ³	2	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	3.6	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.098	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=10A$	---	85	112	$m\Omega$
		$V_{GS}=4.5V$, $I_D=8A$	---	105	120	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.57	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=80V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=10A$	---	13	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	2	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=80V$, $V_{GS}=10V$, $I_D=10A$	---	26.2	---	nC
Q_{gs}	Gate-Source Charge		---	4.6	---	
Q_{gd}	Gate-Drain Charge		---	5.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V$, $V_{GS}=10V$, $R_G=3.3\Omega$ $I_D=10A$	---	4.2	---	ns
T_r	Rise Time		---	8.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	35.6	---	
T_f	Fall Time		---	9.6	---	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1MHz$	---	1535	---	pF
C_{oss}	Output Capacitance		---	60	---	
C_{rss}	Reverse Transfer Capacitance		---	37	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	15	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	24	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=10A$, $dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	37	---	nS
Q_{rr}	Reverse Recovery Charge		---	27.3	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=11A$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

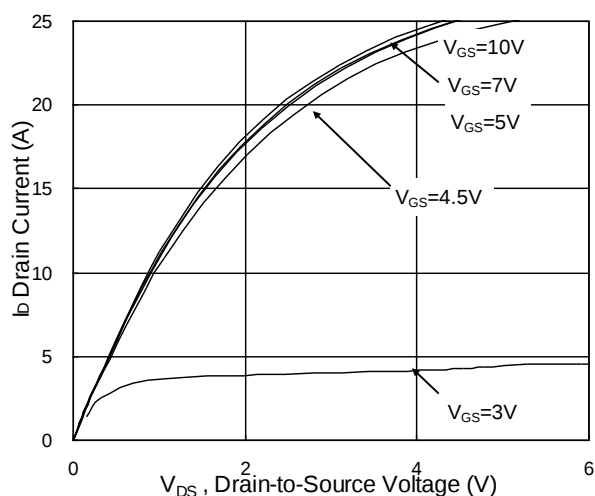


Fig.1 Typical Output Characteristics

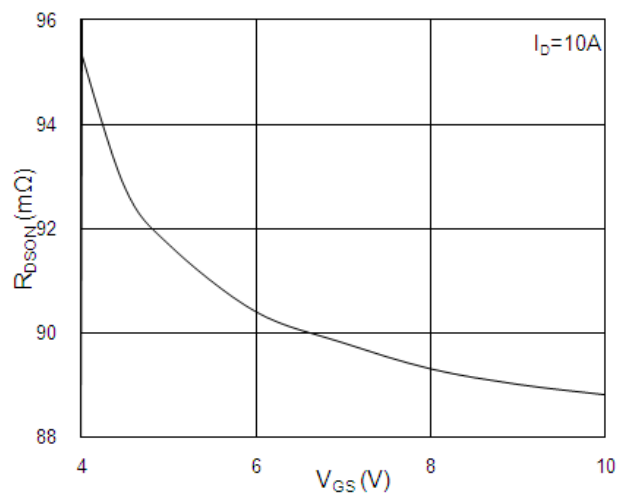


Fig.2 On-Resistance vs. Gate-Source

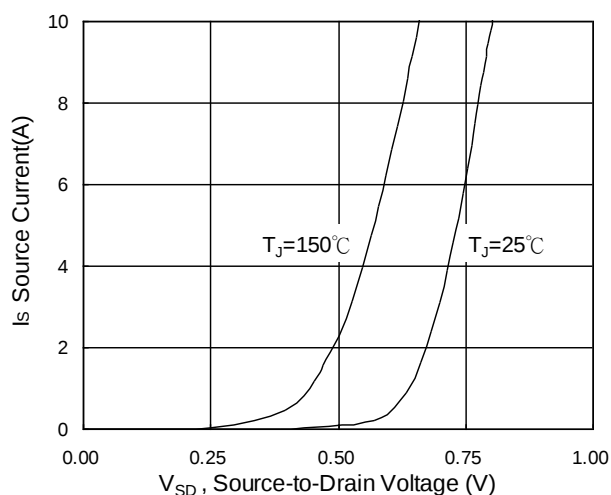


Fig.3 Forward Characteristics Of Reverse

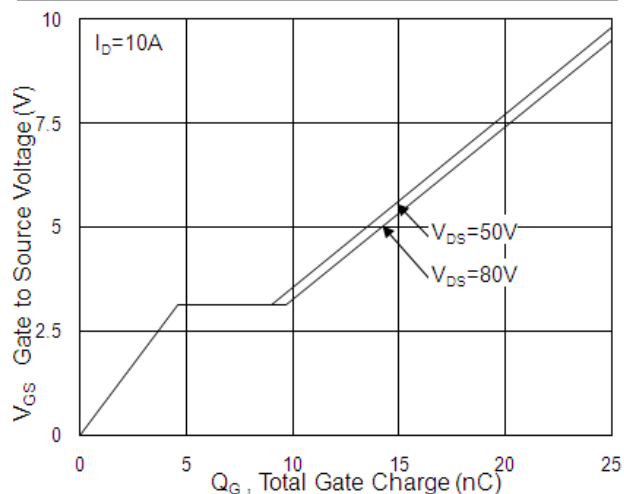


Fig.4 Gate-Charge Characteristics

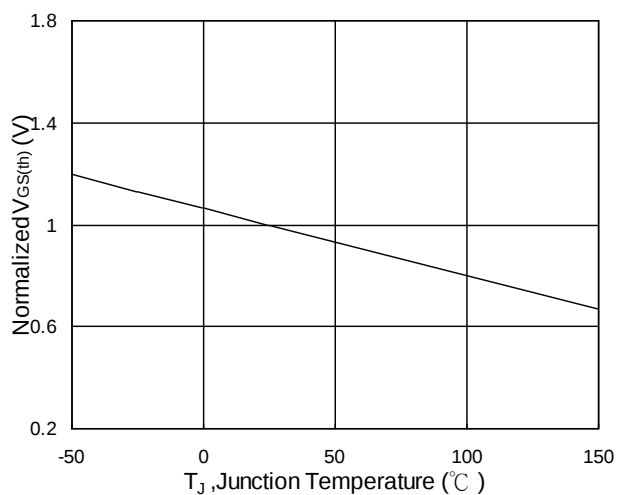


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

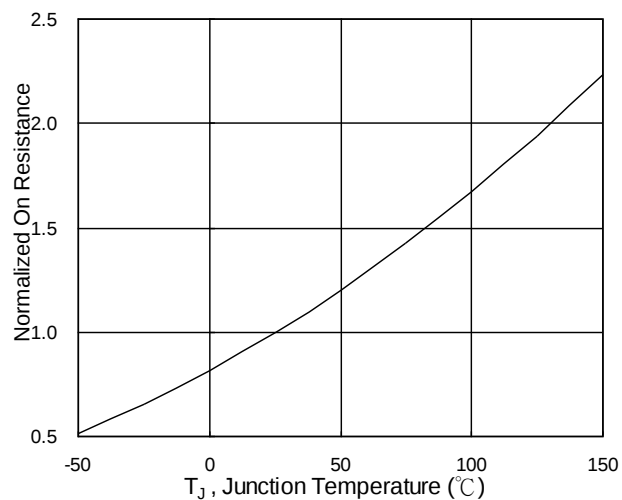


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

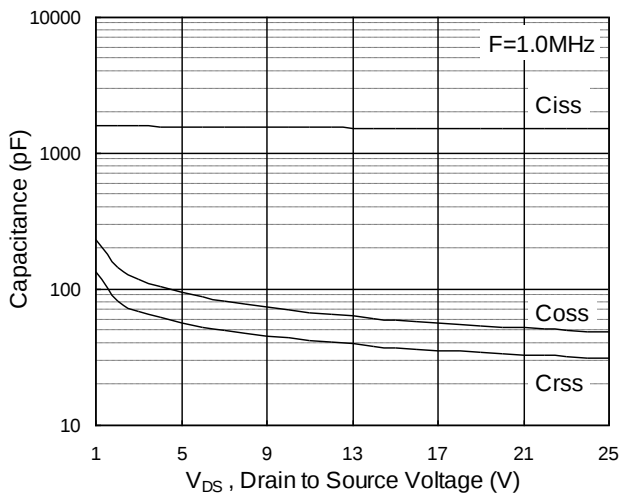


Fig.7 Capacitance

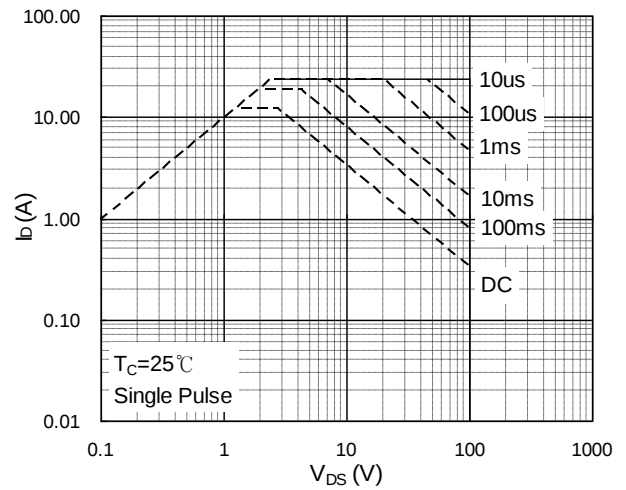


Fig.8 Safe Operating Area

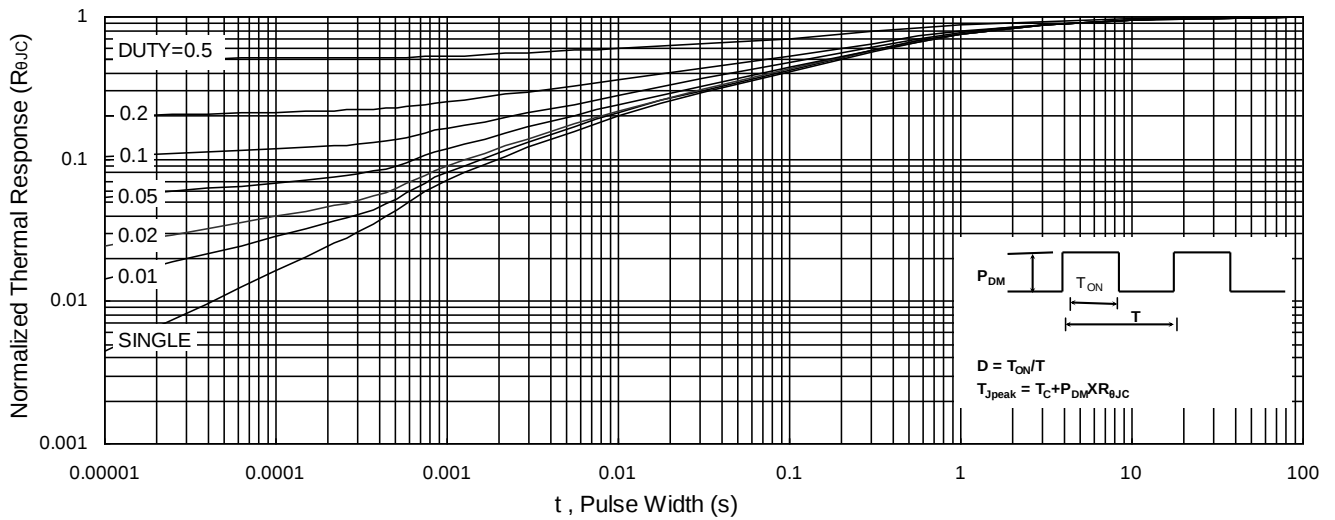


Fig.9 Normalized Maximum Transient Thermal Impedance

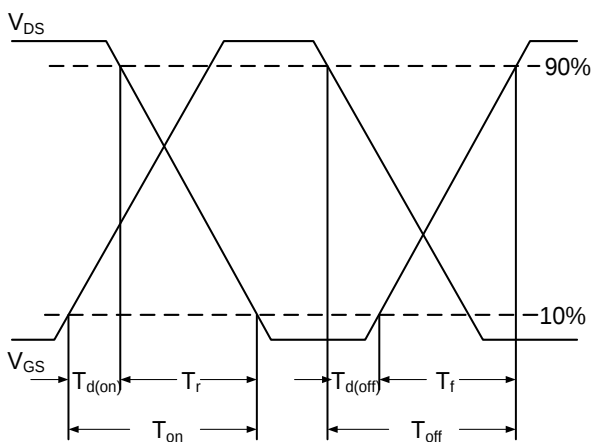


Fig.10 Switching Time Waveform

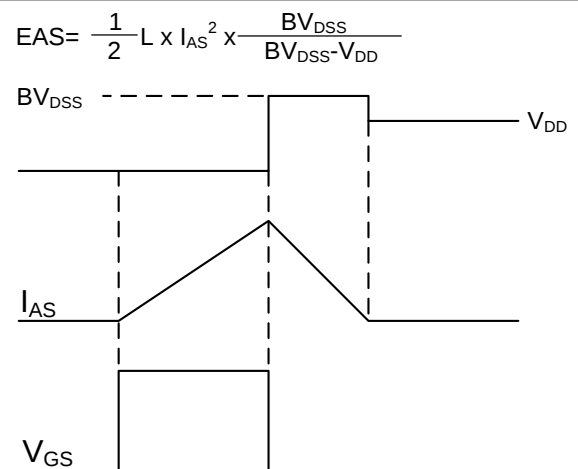


Fig.11 Unclamped Inductive Switching Waveform